

# LINEAR DESIGN SEMINAR



ANALOG  
DEVICES



# LINEAR DESIGN SEMINAR

## Introduction

In the last decade, substantial progress has been made in the design, processing, and volume manufacture of integrated circuits. Most of the attention has been focused on advances in digital circuitry—microprocessors, memories, gate arrays, and the like. However, the linear IC field has progressed at a rate which matches (and in many respects, exceeds) the achievements of digital ICs. New processes, refined existing processes, and new designs have made possible a wide variety of linear integrated circuits which permit more sophisticated analog measurement, control and signal conditioning functions.

This seminar examines not only the range of available products, but also the important aspects of applying these products successfully. Several appendices which the analog circuit designer will find useful are included at the end of the book for future reference.

Analog Devices is well established as a major supplier of precision analog integrated circuits and data converters. Design and process innovation combined with careful product planning underscore our commitment to serving the needs of instrumentation, process control, and avionics systems designers.

In addition, we have always been committed to providing the user with the highest level of technical support available as an aid in state-of-the-art system design and application of high performance components. This seminar is an example of the continuing support to that commitment; we hope it will be of help in understanding and applying the new monolithic amplifiers and analog computational ICs.



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# **OHM'S LAW AND OTHER NOVELTIES OF ANALOG DESIGN**

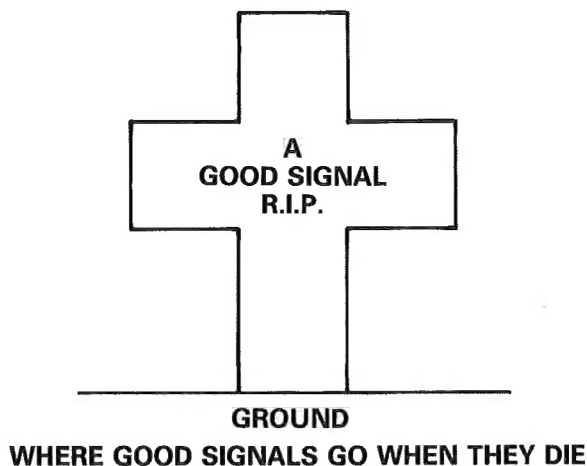




# OHM'S LAW & OTHER NOVELTIES OF ANALOG DESIGN

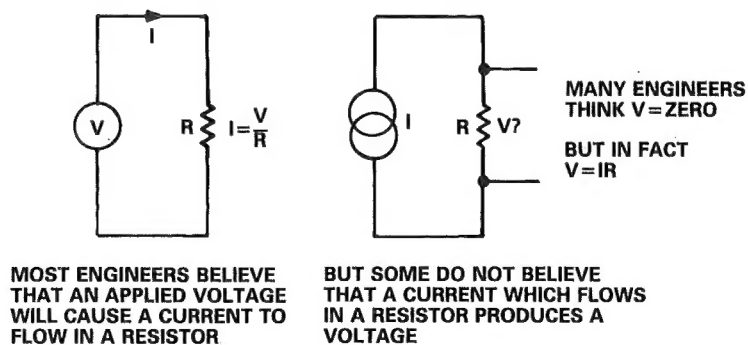
## INTRODUCTION

The most difficult part of the design of successful analog circuits is not the system design but making an entirely rational system perform correctly in real world. The commonest reasons for such failure are disregarding Ohm's and Kirchoff's Laws and the non-ideal performance of passive components, and treating ground as a place where good signals go when they die.



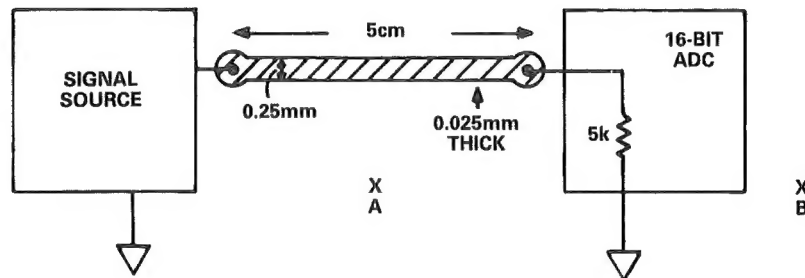
## OHM'S LAW

It is an uncomfortable fact that many electronic engineers do not actually believe Ohm's Law. They will claim to do so but in practice they accept that  $I = V/R$  but not that  $V = IR$ . In other words they have no difficulty in seeing that if a voltage is applied to a resistance a current will flow but they do not consider, in the design and layout of their circuits, that if a resistance is present when a current flows there will be a voltage across it. This can cause all sorts of difficulties.



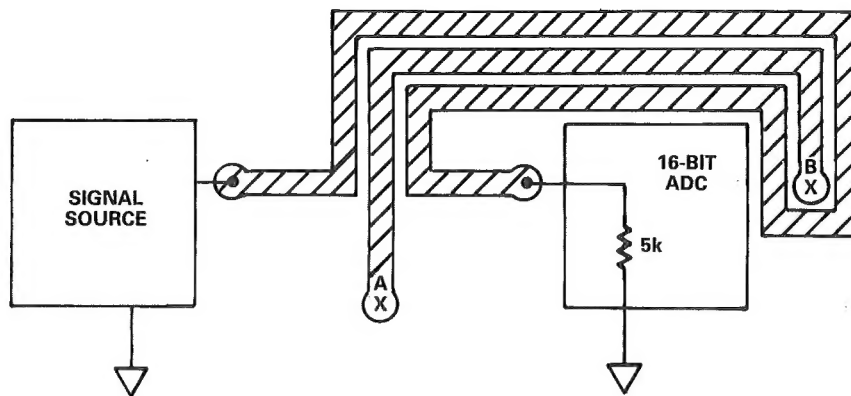
Consider, for instance, a 16-bit analog-digital converter (ADC) with an input resistance of 5K (such a low input resistance, though inconvenient, is not unusual in successive-approximation ADCs). At full scale there would be a voltage drop, and hence an error, of 1 LSB if the resistance of the printed-circuit track between the signal source and the ADC were only 75 milliohms—which is equivalent to only  $50 \times 0.25 \times 0.025\text{mm}$  copper, or 5cm of normal high-density PCB wiring.

### OHM'S LAW PREDICTS 1 LSB DROP IN 5cm OF STANDARD PCB TRACK— BUT WHO BELIEVES OHM'S LAW?



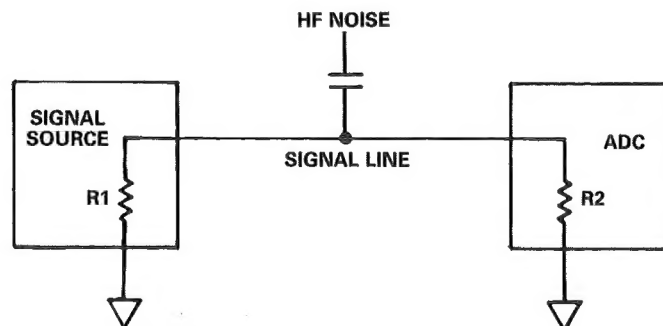
Most computers know even less than engineers about Ohm's law. Computer programs for the design of PCBs normally treat all points in the same metal track as being a "node" and assume that they are at the same potential. This is quite a reasonable assumption for logic circuitry where noise immunities are a volt or more but are unhelpful in precision analog applications. Consider the effect of a small change in the circuit in the previous diagram—points A and B must be joined. A CAD PCB program is quite likely to join the points with a link and then route the previous track around it—it is evident that in a precision analog (or high-frequency) environment such a solution is disastrous.

### AT THE DROP OF A NODE A COMPUTER CAN MAKE THINGS TEN TIMES WORSE



There are several solutions. The best is to ensure that signal leads are short and wide. Increasing the input impedance of sensitive circuitry will also help but this may increase its vulnerability to capacitively coupled interference.

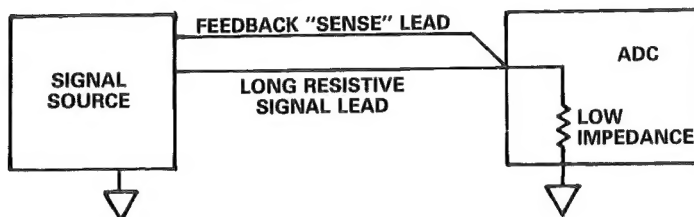
### CAPACITIVE COUPLING OF NOISE



**THE LARGER THE VALUES OF R1 AND R2 THE LESS  
ATTENUATION OF CAPACITIVELY-COUPLED NOISE**

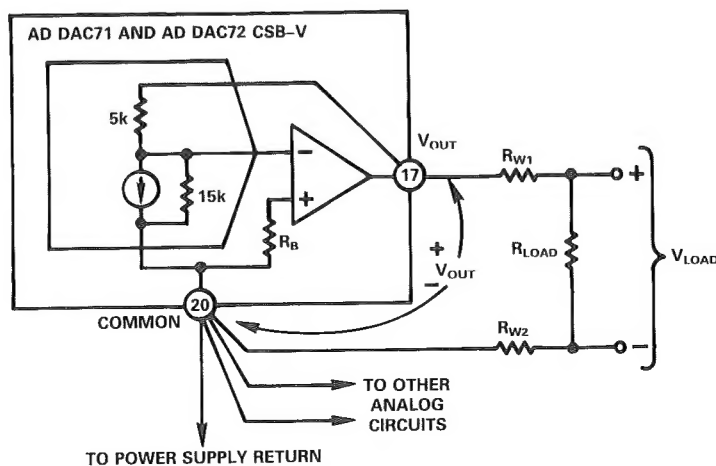
Separate "force" and "sense" leads from a signal source to its load will ensure that the signal source develops its precision at the load itself and not at some "output" pin far from where the precision is needed. In this case it is unlikely that capacitive coupling of interference will cause difficulty.

## USE OF A SENSE CONNECTION MOVES ACCURACY TO THE LOAD



The reason for "force" and "sense" connections becomes clear when we consider all the resistances involved in connecting a signal to a load. Using the DAC71 16-bit DAC as an example we have a load  $R_L$  and resistances  $R_{W1}$  and  $R_{W2}$  in the signal and ground paths respectively.

## PRECISION ANALOG SIGNAL HANDLING

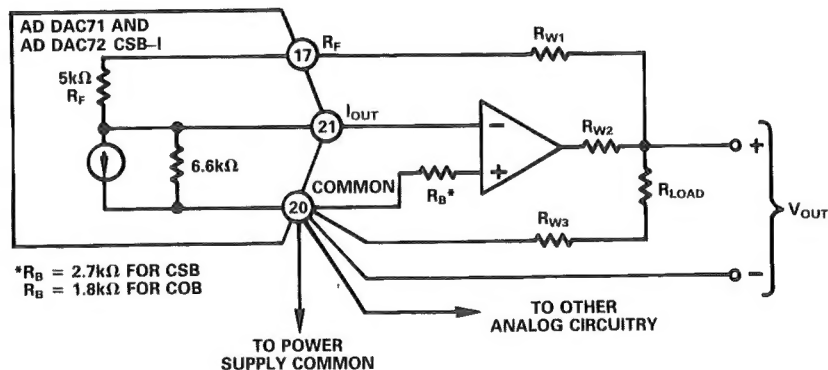


It is evident that the load voltage will be less than the DAC output voltage by the voltage drop in  $R_{W1}$  and  $R_{W2}$  and that if the error is to be less than 1 LSB,

$$\frac{R_{W1} + R_{W2}}{R_{LOAD}} < \frac{1}{2^{16}}$$

At 16 bits even the voltage drop in the sense lead itself may need to be considered in cases where the impedance of the sense terminal is not very high. This can be seen in the connection of the current output version of the DAC71 where  $R_{W1}$  appears in the feedback path and can still have serious consequences.

## PRECISION ANALOG SIGNAL HANDLING



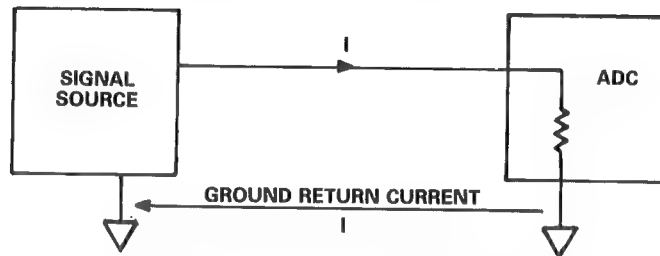
From considering these cases we can derive a general rule: at some stage of the design of any precision analog system all lead resistances should be added to the circuit diagram and their effects on system accuracy computed. In most cases it will be clear that they can be disregarded—in a few cases they will be seen to be critically important to system accuracy.



## KIRCHHOFF'S LAW

Disregarding Kirchoff's Law is equally dangerous. Kirchoff's law is generally preceived as being relevant only to the analysis of current flowing in networks having several nodes but it is equally relevant in the analysis of a signal source driving a single load.

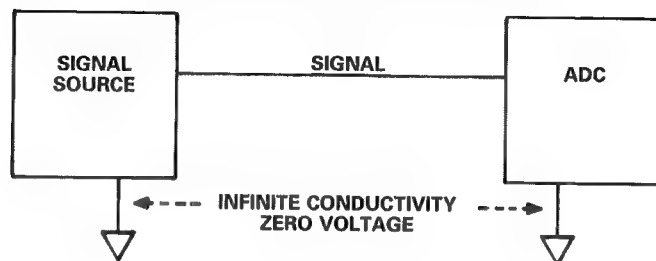
### KIRCHHOFF'S LAW



**AT ANY POINT IN A CIRCUIT  
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO  
OR  
WHAT GOES OUT MUST COME BACK  
WHICH LEADS TO THE CONCLUSION THAT  
ALL SIGNALS ARE DIFFERENTIAL  
(EVEN IF THEY'RE GROUNDED)**

Kirchoff's Law states that the net current at any point in a circuit is zero and therefore implies that the current which goes from a source to a load must return to its source—i.e., that all signals are differential. The signal return is just as important to system accuracy as the so-called “signal path”—and is much more likely to be disregarded during the system design. Far too many designers assume that the return path is “ground” and consider the matter no further. Treating all ground connections as being at exactly the same potential is very dangerous. (A point is a mathematical abstraction—does this tell us anything about “common grounding point”?) The concept of “ground” as a connection to a point of zero potential and infinite conductivity is attractive in theory and may be useful during preliminary system design but it can lead to major errors in real systems.

### THE IDEAL GROUND

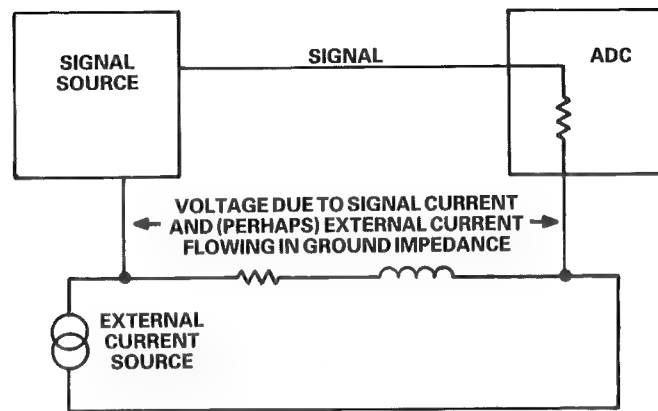


## GROUNDS

In real life, ground conductors have both resistance and inductance and may also be carrying unpredictable currents which will give rise to voltage drops when they flow in the ground impedances. CAD PCB programs are particularly bad at ground design because they tend to keep all conductors as thin as possible to conserve copper and board area and this, of course, results in high ground resistance.

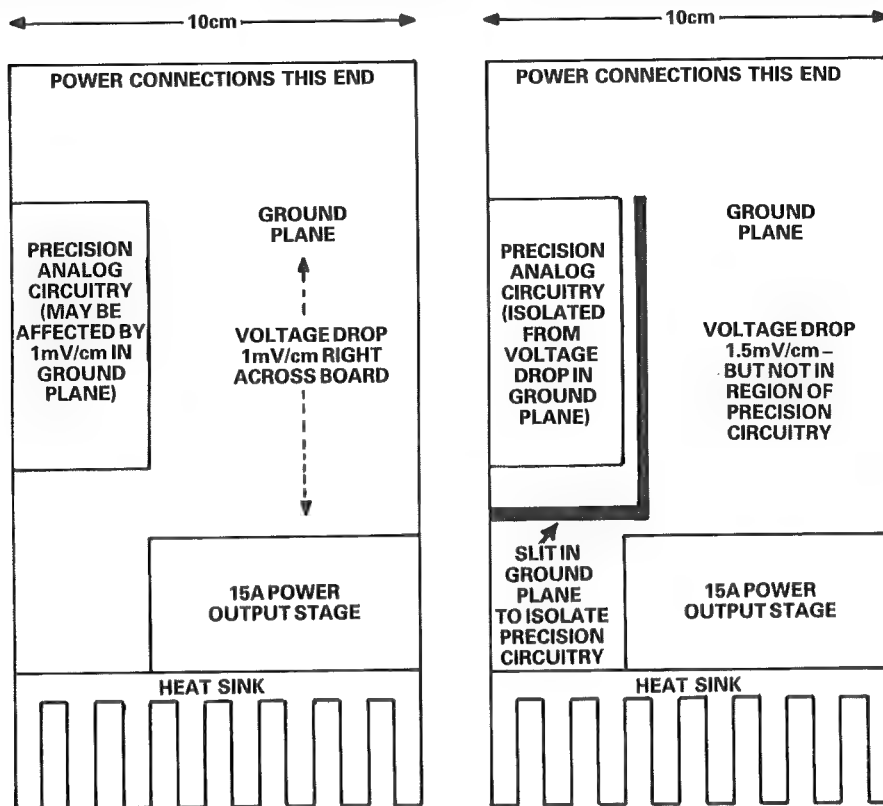
As a general principle the design of PCBs for precision analog applications is far too important to be delegated to an apprentice, the drawing office or, worst of all, a computer but should be the direct responsibility of the project leader.

## A MORE REALISTIC GROUND



There is an obvious alternative to thin ground leads—a continuous “ground plane” of copper covering one side of a PCB to which all ground connections are made. The resistance of 0.001” (0.025mm) copper is approximately 0.67m $\Omega$ /square so this solution is frequently adequate—but not always.

## A SLIT IN A GROUND PLANE CAN RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

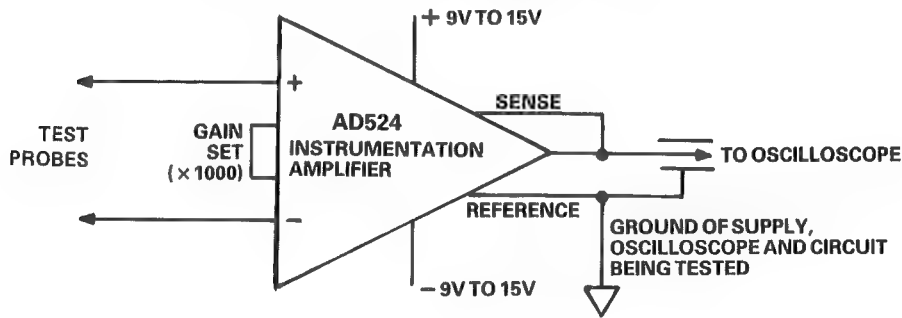


Consider a 15 × 10cm PCB with a ground connection at one end and a power amplifier at the other drawing 15A (it is not possible to mount the amplifier near to the ground bus-bar because it requires a heat-sink). If this current flows in a 0.001” ground plane on the PCB there will be a voltage drop of about 1mV/cm in the ground plane—which would cause quite serious problems to any high precision circuitry sharing the PCB. If we slit the ground plane so that the high current does not flow in the region of the precision circuitry the situation is greatly improved—even though the voltage drop will increase in the region where the current does flow.

Accuracy (and stability) problems in precision circuitry arising from the causes we have discussed can very often be avoided if the engineer is aware that such problems can occur and takes steps during the system and PCB design to ensure that they do not. When they arise during design changes in existing systems they can be very intractable, not least because it is so hard to measure microvolt potential differences in ground conductors.

There is a simple piece of testgear which can be used to find small (but significant) voltage drops in ground or signal conductors. It consists of a single instrumentation amplifier—such as the AD524—used as a fully differential input stage to an oscilloscope.

### AN INSTRUMENTATION AMPLIFIER CAN BE USED TO MEASURE DIFFERENTIAL VOLTAGES DOWN TO A FEW MICROVOLTS



Since the instrumentation amplifier has low noise, good common-mode rejection and gain of up to 1000 it may be used to measure voltage drops of a few microvolts at bandwidths of up to 50kHz. By moving the probes around ground or signal tracks the voltage drops in them may easily be observed and measured (the system is also very useful for finding short-circuits). The high input impedance and low bias current of the amplifier ensure that the measurement may be made with minimal loading of the circuit being measured (this is, of course, unimportant when making ground measurements). The instrumentation amplifier may be powered from the circuit under test or by a pair of 9V batteries—if batteries are used their centre-point must be connected to the circuitry being measured (generally to its ground) to provide a return path for the instrumentation amplifier bias currents.

When a precision analog system is built on a single PCB it is generally possible to overcome the difficulties that we have discussed and make it perform as required. The following steps should be followed:

### STEPS IN THE DESIGN OF PRECISION ANALOG CIRCUITS

1. Examine your circuit diagram and determine which voltage differences must be communicated accurately through the circuit and the currents which must flow in transmitting them.
2. Redraw the circuit diagram so that "Output" voltages (treated differentially) connect to the desired "Inputs" (also treated differentially). In plain English, hook up the main signal paths without using ground or common connections.
3. Identify signal paths which must be shared and eliminate those which are unnecessary.
4. Identify high current signal paths so that they can be made low impedance at signal frequencies.
5. Now add the power supplies to the diagram, identify and newly-formed signal connections and ensure that they are tolerable (it may be necessary to use isolated power or fully differential amplifiers [such as instrumentation or isolation amplifiers] to overcome problems arising at this point).
6. Tie up any loose ends (protection circuitry, location of any digital circuitry, reconfiguration of HF currents with capacitors, etc.) and again check their effect on the diagram in [2] and correct any abominations.
7. Build the circuit as you have designed it. Take two aspirins and try it. With luck the problems will be simple enough to find and fix without too much grief.

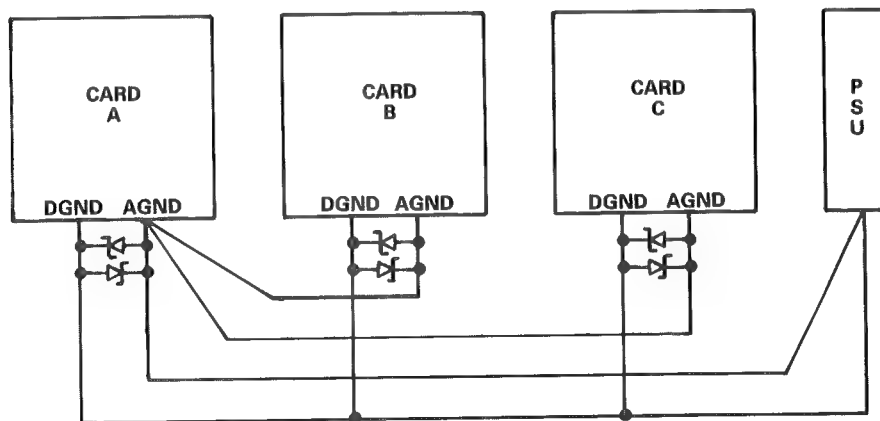
**NEVER OMIT STEP SEVEN!**



These steps are quite clear and easily understood and yet probably as many as 60% of the problems seen by the Applications Department of Analog Devices arise from not following them. In particular step 7 is ESSENTIAL. Any engineer who sends a design to production without first testing it thoroughly is unworthy of the title of engineer—but far too many do just that.

Where systems are built on more than one card or PCB (and where different systems may be made by using different configurations of a few standard cards) it is much harder to follow such a procedure because of the difficulties of separating signal and power return paths. Where it is possible the same principles should be applied (but additional precautions may have to be taken to ensure that unplugging a card does not damage adjacent cards by open-circuiting their ground—a few Schottky diodes will solve this in any application where the difference between the analog and digital ground is unlikely to exceed 250mV).

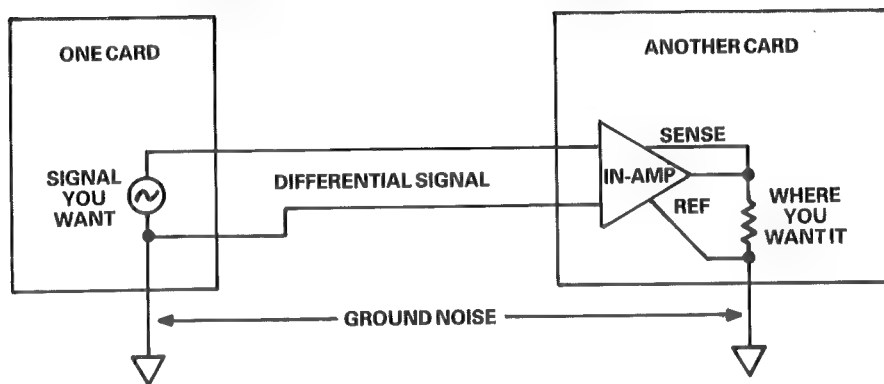
## GROUNDING OF A MULTIPLE CARD SYSTEM



**SCHOTTKY DIODES PROTECT CARDS IN THE EVENT OF  
LOSS OF ANALOG GROUND**  
(THIS GROUNDING SYSTEM MAY BE INADEQUATE AT  
HIGH RESOLUTION OR WHERE LARGE GROUND CURRENTS FLOW)

Where it is not possible to eliminate ground errors between cards fully differential transmission should be considered for all precision analog signal paths. This will involve the use of instrumentation or isolation amplifiers.

## DIFFERENTIAL AMPLIFIERS CAN ELIMINATE GROUND ERRORS



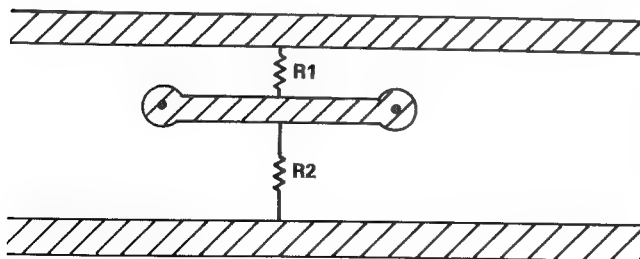
These are both differential amplifiers with high common-mode rejection. They differ in their common-mode ranges and bias requirements: an instrumentation amplifier has a common-mode range of less than its power supply and its bias current must flow to or from one of its supplies or some point between them, while an isolation amplifier has a common-mode range of many hundreds or thousands of volts and its bias current return is referred to its input stages rather than its power supplies. Instrumentation amplifiers, which today are usually monolithic, are less expensive than isolation amplifiers, which are manufactured using hybrid or modular techniques. In most applications instrumentation amplifiers are quite sufficient and cost only a few dollars.

## LEAKAGE CURRENTS

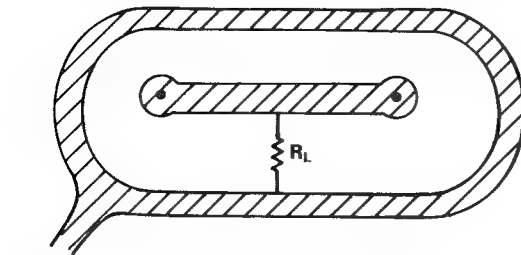
Disregard of Ohm's Law is not confined to overlooking the resistance of conductors—problems also arise from ignoring the conductivity of insulators. We have considered the difficulties we may encounter when comparatively large signal currents flow in small resistors—when using transducers with very small output currents stray leakage currents can be equally damaging.

When amplifying signals from photocells and electrochemical cells source impedances may be many millions or billions of ohms. If PCBs are inadequately cleaned after etching the residual electrolytes on the board surface may result in comparable resistances between nearby conductors and even with properly cleaned boards leakage resistances of no more than  $10^{12}$  ohms can be expected. These resistances, moreover, are unlikely to be isotropic so that the resistance between two adjacent tracks may be higher than that between two tracks separated by a much larger gap. For this reason the inputs to low-level I/V converters should be protected by guard rings ON BOTH SIDIES OF THE PCB connected to a point at the same potential as the summing junction. If this is done the exact value of the leakage resistance is unimportant since the potential difference across it will be small.

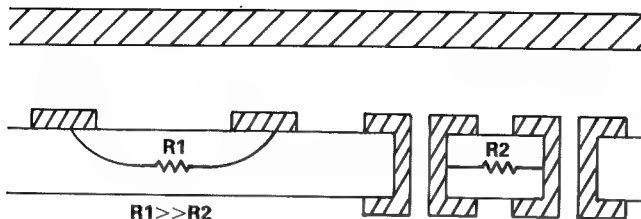
## LEAKAGE RESISTANCE ON PRINTED CIRCUIT BOARDS



**SURFACE LEAKAGE ON A PCB IS UNPREDICTABLE.  $R_1$  IS NOT NECESSARILY LESS THAN  $R_2$**



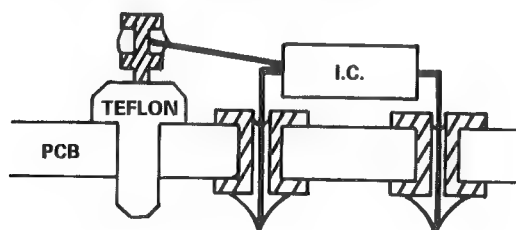
**IF A VULNERABLE CONDUCTOR IS SURROUNDED BY A GUARD RING (ON BOTH SIDIES OF THE BOARD) WHICH IS AT THE SAME POTENTIAL AS THE CONDUCTOR IT IS GUARDING THE EFFECTS OF LEAKAGE RESISTANCE WILL BE MINIMIZED**



**LEAKAGE RESISTANCE BETWEEN SURFACE TRACKS ON A PCB IS GENERALLY MUCH LARGER THAN BETWEEN PLATED HOLES**

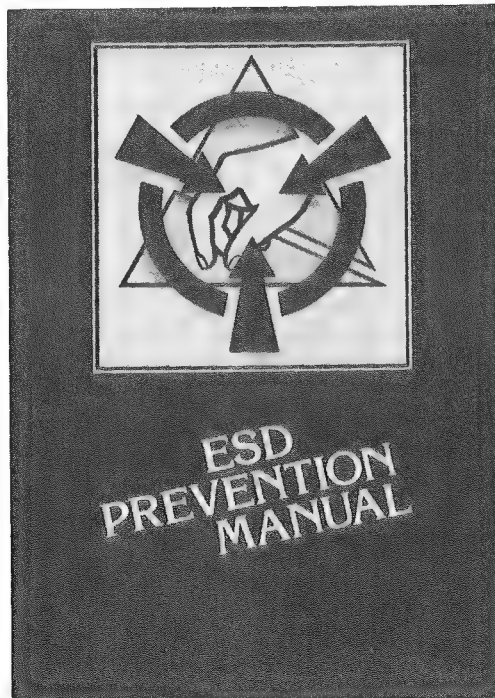
In applications of this type the use of plated-through holes (PTH) is inadvisable. The bulk resistivity of PCB material is much lower than the sheet resistivity of its surface and it is very difficult to fabricate a guard ring in the bulk of a board. The best approach of all is to connect such high impedance amplifier terminals to a virgin teflon stand-off insulator rather than a PCB track. (A virgin teflon insulator is made from a solid piece of new teflon which has not been welded together from powder or grains.)

## A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK



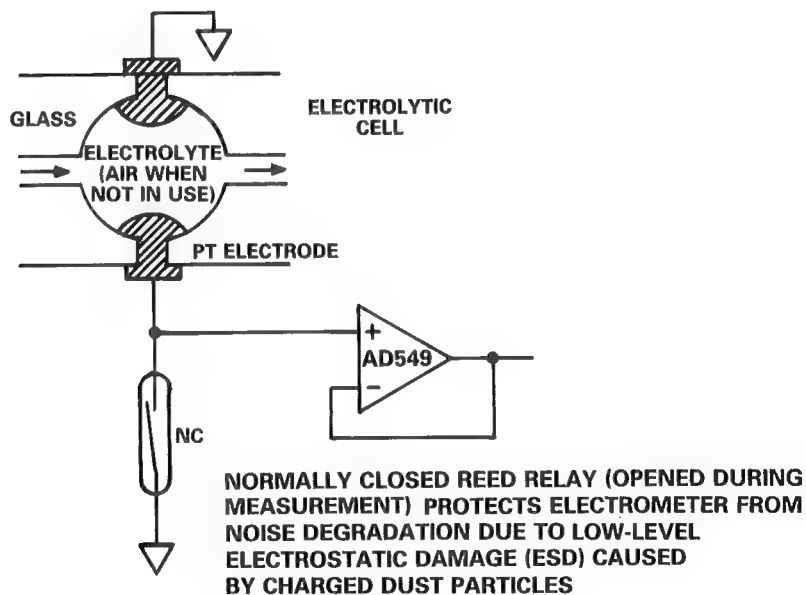
## ELECTROSTATIC DAMAGE (ESD)

Where resistance is very high there is often the possibility of electrostatic charge—and electrostatic damage. A full discussion of electrostatic damage (ESD) is given in the Analog Devices' Application Note on the subject which is available free of charge from any Analog Devices office or agent.



At this juncture it is sufficient to point out that all integrated circuit structures are vulnerable to damage from the high voltages and high peak currents involved in even small electrostatic discharges but that precision analog circuits suffer from a special disadvantage—the circuitry used to protect integrated circuit structures from ESD can often degrade the analog accuracy of the circuit where it is employed. Thus we have the choice of high performance or a high degree of protection. Which we choose will depend on individual circumstances but it is essential to realize that the choice may have to be made—and if it is made in favour of accuracy then the circuit involved must not be exposed to electrostatic discharge.

An interesting example of an unobvious effect of ESD occurred in Finland, where the very cold Winters produce very low humidity and particularly severe electrostatic problems. A customer complained that a particular BIFET amplifier type had poor long-term reliability and this its noise performance degraded during a few years of use.





The amplifier was being used as a unity gain buffer with an electrochemical cell and the noninverting input was connected to a platinum electrode and to nothing else. In use this electrode was immersed in electrolyte but after use it was washed (automatically) in deionised water and air dried. It was then left unconnected until the machine was next used.

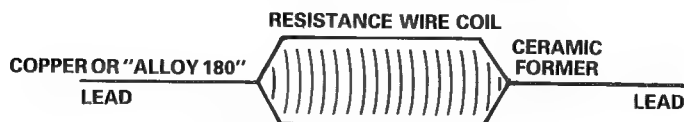
Although there is no possibility of the electrode being touched at this time (it was in the very centre of the machine) it could encounter random particles of electrostatically charged dust—and the pulse currents as these discharged were sufficient to cause slow degradation of the noise figure. As soon as arrangements were made to ground the electrode (with an NC reed relay for minimum leakage) the problem disappeared.

## RESISTORS

Between the low resistance of conductors and the high resistance of insulators there is yet another resistive source of inaccuracy in precision circuitry—resistors themselves. We normally assume that a resistor is a simple component which actually performs much as it might theoretically be expected to do. In fact it is necessary to consider a number of additional factors when designing high precision analog circuits incorporating resistors.

The most obvious imperfection is the inductance of a wirewound resistor. A wirewound resistor consists of a coil of resistance wire on a ceramic former—the coil, of course, has inductance as well as resistance which will affect the high frequency performance of any circuit using such a resistor (even a low frequency circuit built with an inductive resistor may suffer loss of accuracy if the inductance causes an oscillation—and such oscillation may be at too high a frequency to be observed on an LF oscilloscope). Some wirewound resistors have half their turns wound clockwise and the other half wound anticlockwise—this technique minimizes their reactance but rarely causes it to disappear altogether. Residual inductances of up to  $20\mu\text{H}$  are quite normal for resistance values below  $10\text{K}$  but the dominant reactance may actually take the form of shunt capacitance of the order of  $5\text{pF}$  for noninductively wound resistors above  $10\text{K}$ .

### WIREWOUND RESISTORS



WIREWOUND RESISTOR



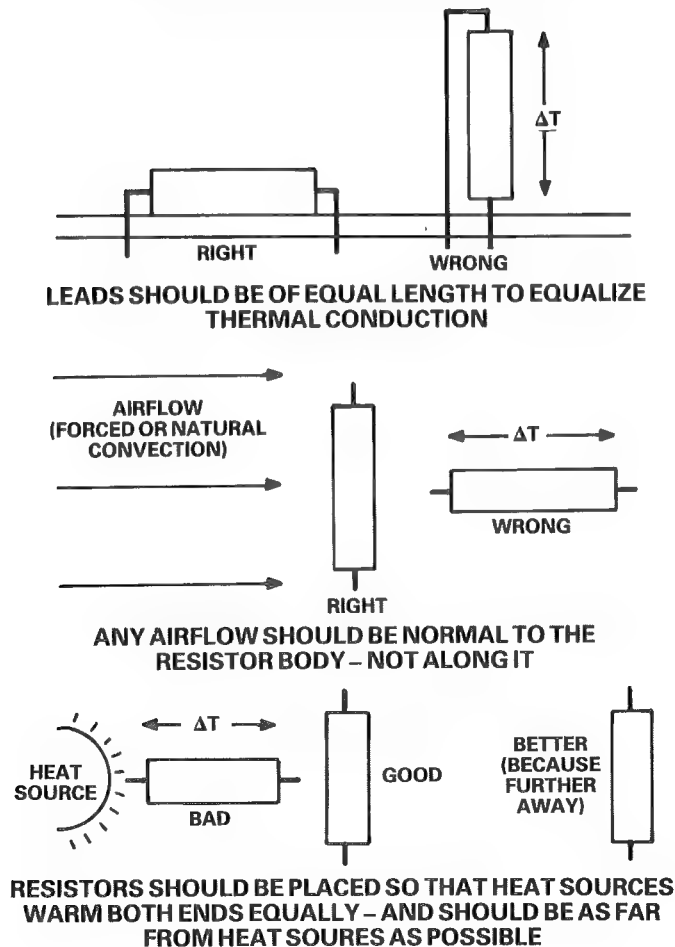
EQUIVALENT CIRCUIT

**THE INDUCTANCE OF WIREWOUND RESISTORS CAUSES ERRORS WHEN THEY ARE USED IN HF PRECISION CIRCUITRY AND MAY CAUSE UNSUSPECTED VHF INSTABILITY EVEN IN LF AND DC CIRCUITRY.**

**THE NET THERMOELECTRIC OUTPUT OF A WIREWOUND RESISTOR IS ZERO IF BOTH ENDS OF THE RESISTOR ARE AT THE SAME TEMPERATURE. IF THEY ARE NOT THE EMF MAY BE  $42\mu\text{V}/^\circ\text{C}$  TEMPERATURE DIFFERENCE.**

Wirewound resistors have another problem. The junction of the resistance wire and the lead forms a thermocouple which has a thermoelectric EMF of  $42\mu\text{V}/^\circ\text{C}$  for the standard "Alloy 180"/Nichrome junction of an ordinary wirewound resistor (if a resistor is chosen with the [more expensive] Copper/Nichrome junction the value is  $2.5\mu\text{V}/^\circ\text{C}$  ["Alloy 180" is an alloy of 77% copper & 23% nickel]). Such thermocouple effects are unimportant in ac circuitry or where a resistor is at a uniform temperature but if the dissipation in a resistor, or its location with respect to heat sources, can cause one of its ends to be warmer than the other then there will be a net thermoelectric EMF which will introduce a dc error into the circuit. With a normal wirewound resistor a temperature differential of only  $4^\circ\text{C}$  will introduce a dc error  $168\mu\text{V}$ —which is greater than 1 LSB in a  $10\text{V}/16\text{-bit}$  system.

## MINIMIZING THERMOCOUPLE EFFECTS IN WOREWOUND RESISTORS

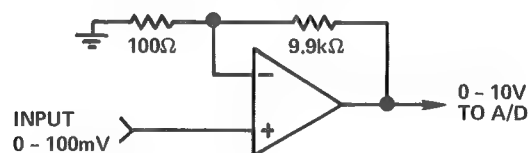


The problem may be minimized by mounting wirewound resistors to ensure that temperature differentials are minimized. This may be done by ensuring that both leads are of equal length to equalize thermal conduction through them, by making any airflow (whether forced or natural convection) normal to the resistor body, and by taking care that both ends of the resistor are the same distance from any heat source on the PCB, and that, notwithstanding the above precautions, all precision resistors are located as far as possible from any sources of heat. Even after these precautions have been taken it is still wise to use resistors with copper, rather than "Alloy 180", leads.

The best discrete resistors for most precision applications are metal film or carbon film types. These are stable, accurate and low noise and are available with low temperature coefficients. Carbon composition resistors should be avoided in precision circuitry because they are noisy and have poor temperature coefficients and worse long-term stability.

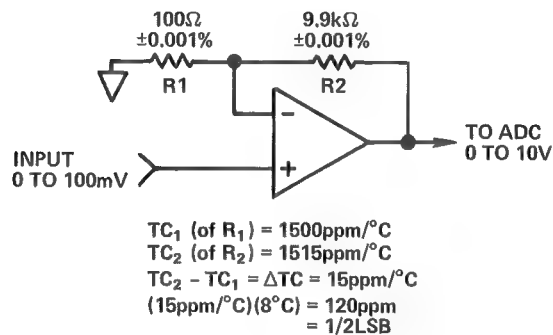
But all discrete resistors have problems. Consider a simple circuit comprising an operational amplifier and two resistors configured to make a precision amplifier with a gain of 100.

### GAIN OF 100 STAGE



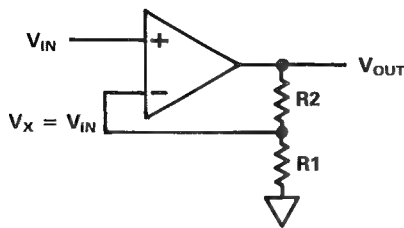
Let us assume that the amplifier is made with a perfect op-amp and that the two resistors are perfectly accurate at 25°C. If the temperature coefficients of the two resistors are 1500 and 1515ppm/°C (i.e., they differ by only 1%) then a temperature change of only 8°C would cause a change in resistor matching of 120ppm which would represent a full-scale gain error of 0.5LSB in a 12-bit system. This is obviously unacceptable.

## TEMPERATURE EFFECTS × 100 AMPLIFIER



It would seem, therefore, that we require our precision resistors to have both their resistance values and temperature coefficients well-matched—but even this is not enough.

## EFFECTS OF RESISTOR SELF-HEATING



$R_1 = 100\Omega$  BOTH ABSOLUTELY ACCURATE @ 25°C  
 $R_2 = 9.9k\Omega$  0.125W (125°C/W) & 100ppm/°C

$V_{IN} = 0$  THEREFORE  $V_{OUT} = 0$  THEREFORE DISSIPATION IS ZERO.  
 $V_{IN} = 0.1V$  THEREFORE  $V_{OUT} = 10V$

	THEREFORE DISSIPATION	TEMPERATURE RISE	DELTA R
R1:	$\frac{(0.1)^2}{100} = 0.025\text{mW}$	0.0125°C	1.25ppm
R2:	$\frac{(9.9)^2}{9900} = 9.9\text{mW}$	1.24°C	124ppm

GAIN ERROR = 123ppm = 1/2LSB (12-BIT)

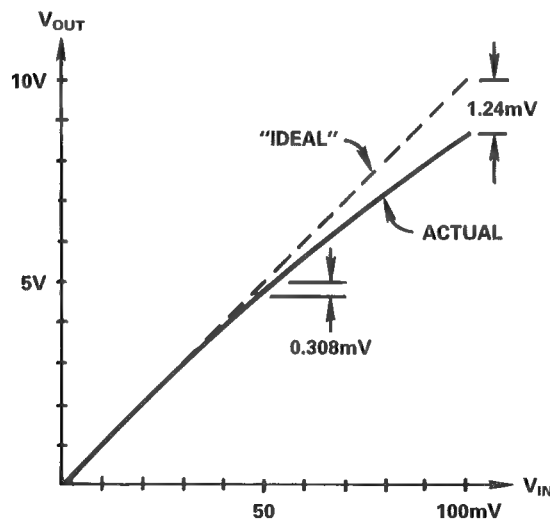
BUT THE EFFECT IS NONLINEAR

$V_{IN} = 0.05V$  THEREFORE  $V_{OUT} = 5V$

R1:	$\frac{(0.05)^2}{100} = 0.025\text{mW}$	0.003°C	0.4ppm
R2:	$\frac{(4.95)^2}{9900} = 2.48\text{mW}$	0.3°C	30.8ppm

GAIN ERROR = 30ppm = 1/4LSB (12-BIT)

## AMPLIFIER CIRCUIT TRANSFER FUNCTION



Consider the same amplifier built with a perfect op-amp and perfectly matched 0.125W metal film resistors which are matched not only for resistance but for their temperature coefficient of 100ppm/°C. When the input voltage is zero the output is also zero and neither resistor dissipates any power—the amplifier gain is accurate. If, on the other hand, an input of 100mV is applied to the amplifier the output is 10V and a current flows in both R1 and R2.

The voltage across R2 is 9.9V and the dissipation is 9.9mW, which causes the temperature of R2 to increase by 1.24°C. The dissipation in R1, on the other hand, is only 0.1mW and the temperature rise only 0.0125°C. The change of temperature difference due to resistor self-heating is therefore approximately 1.24°C and as a result the resistor match will be degraded by  $1.24 \times 100 = 124\text{ppm}$ —which is 0.5 LSB at 12-bits.

Worse—the effect is nonlinear. At half scale the heating (which is, of course, proportional to the square of the voltage) is only one quarter as great and the error is only 0.125 LSB. Thus self-heating makes the circuit nonlinear as well as inaccurate.

## **RESISTOR SELF-HEATING PRODUCES GAIN AND LINEARITY ERRORS**

**Thermal Time Constants Make the Error Dependant Not On the Current Resistor  
Dissipation But On the rms Voltage On the Resistor During the Previous Few Seconds –**

**Which Makes Compensation Virtually Impossible**

**The Problem May Be Prevented By Ensuring that Resistors Used Have:**

- **Closely Matched TCs**
- **Low Absolute TCs**
- **Low Thermal Resistance**
- **Tight Thermal Coupling Between Resistors Whose Matching is Critical**

**BEST SOLUTION IS TO USE A MONOLITHIC CHIP CONTAINING BOTH THE AMPLIFIER  
AND THE RESISTOR NETWORK OVERALL PERFORMANCE IS THEN GUARANTEED  
BY THE INTEGRATED CIRCUIT MANUFACTURER.**

**WHERE THIS IS NOT POSSIBLE A SINGLE THIN-FILM RESISTOR NETWORK SHOULD  
CONTAIN ALL THOSE RESISTORS WHOSE MATCHING IS CRITICAL**

There is yet another effect. Since the heating is not instantaneous the error in the gain of the amplifier will depend, not on the present input, but on the rms input during the previous few seconds. This is obviously most unsatisfactory and is best solved by not using discrete resistors.

If several thin-film resistors are manufactured on a single substrate from a single resistive film then we can reasonably expect that their temperature coefficients will be very well matched. Also if they are on the same substrate dissipation in one resistor will heat them all so that there will be no differential temperature to cause errors. Thus it is evident that if the matching of several resistors is critical for the performance of a precision analog circuit than all the resistors should be fabricated on a single substrate.

Such resistor networks are readily available on ceramic substrates and may be used wherever precision resistor matching is required. There is an even better solution, however,—the use of monolithic integrated circuits which contain laser-trimmed resistor networks in addition to such active circuit elements as amplifiers or digital-analog converters (DACs). Such devices are not yet available for all applications but where they are available they are undoubtedly the best solution to the problem because the integrated circuit manufacturer has guaranteed the overall performance of both the amplifier and resistors supplied with it (he may even have arranged for nonlinearities in one to be compensated in the other).

Precision applications involving very high value resistors cannot use resistors on a monolithic chip or a thin-film network, which are limited to values between a few tens of ohms and a few megohms. In this case there is no alternative to carbon film or cermet resistors. Some high value resistors suffer quite badly from voltage variable resistance and devices whose data sheets indicate that they are liable to this problem should not be used in precision applications. The best high megohm resistors are packaged in glass and treated with silicone varnish to minimize the effects of humidity. The resistor bodies should never be touched with ungloved hands as surface contamination of the glass can cause leakage currents larger than the currents in the resistor—ruining the accuracy.

# RESISTOR COMPARISON CHART

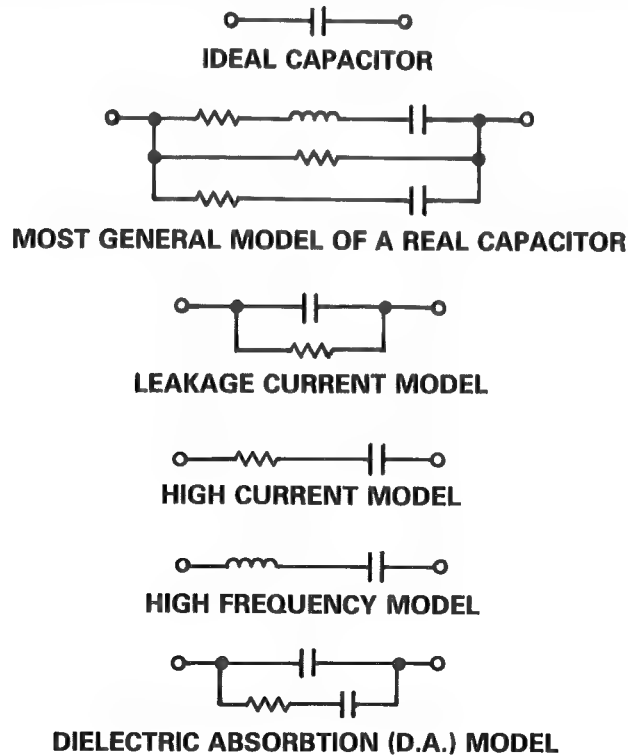
TYPE		ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size	Poor Tolerance (5%) Poor Temperature Coefficient (1500ppm/°C)
	Wire-Wound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance May be a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance	Low Power Very Expensive
	High Megohm	Very High Values ( $10^8 - 10^{14} \Omega$ ) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film on Glass	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimable Low Capacitance	Delicate Often Large Geometry Low Power
	Thin Film on Ceramic	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry
NETWORKS	Thin Film on Silicon	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimable Suitable for Monolithic IC Construction	Some Capacitance to Substrate Low Power
	Thin Film on Sapphire	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Laser-Trimable Low Capacitance	Higher Cost Low Power



## CAPACITORS

Capacitors can also behave in ways which are inconsistent with their simple model and thus introduce errors into precision circuitry. An ideal capacitor is a simple device—real capacitors suffer from a number of different problems which cause difficulties in different applications. While it would be possible to make a general model of nonideal capacitor and use it in all circuit analyses it would be unprofitable to do so since different features are important in different applications.

### EQUIVALENT CIRCUITS OF A REAL CAPACITOR



Capacitors are used for coupling (passing ac signals while blocking dc), for decoupling (removing ac superimposed on dc in both power and signal circuitry), for building filters or frequency-selective networks, and for storing charge in “sample and hold” circuits (also known as “track and hold” circuits or SHAs, SAHs or THAs).

In coupling and SHA applications the leakage of the capacitor can be important. Electrolytic capacitors, where the dielectric is formed by an electrochemical reaction, have relatively high leakage currents of microamperes or even more and so are not used in applications where leakage matters. The leakage of electrolytic capacitors is greater during the first few minutes of operation after a period of storage (the leakage current while the capacitor is in use keeps the dielectric in good condition and it may deteriorate slightly in storage)—this feature can be important in equipment which must perform correctly after a long quiescent period.

The leakage of tantalum electrolytic capacitors is lower than that of aluminum ones and so in applications where capacitances of tens of microfarads or more (which can be achieved only with electrolytic capacitors) are required tantalum ones are used, despite their extra cost, if particularly low values of leakage current are necessary. At room temperature the leakage of aluminum electrolytic capacitors is of the order of  $20\text{nA}/\mu\text{F}$  and that of tantalum ones is  $5\text{nA}/\mu\text{F}$ .

Another feature of electrolytic capacitors, both aluminum and tantalum, is that most of them are polarized and require a dc bias for correct operation—a reverse bias may do damage and will certainly increase leakage.

Most other types of capacitor have leakage resistances in excess of hundreds of gigohms so that for most applications their leakage currents can be disregarded.

The series resistance of capacitors causes them to dissipate power when high ac currents are flowing in them. This can have serious consequences at RF and in high current supply decoupling capacitors but is unlikely to have much effect in precision analog circuitry. The series inductance, however, can have very inconvenient consequences.

The transistors used in precision analog circuits have transition frequencies ( $f_t$ ) of hundreds of MHz or even several GHz, even though the precision circuitry itself may be operating at dc or low frequencies. This makes it essential that the power supply terminals of such circuits should be decoupled properly at high frequency.

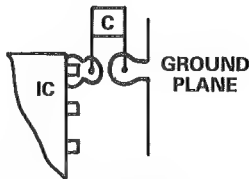
A common structure for capacitors is two sheets of metal foil separated by sheets of dielectric and formed into a roll. Such a structure has considerable inductance and behaves as an inductance at frequencies of more than a few MHz. It is therefore inadvisable to use electrolytic capacitors, paper capacitors or plastic film ones for decoupling at high frequencies.

Monolithic ceramic capacitors have very low series inductance (they are formed of a multilayer sandwich of metal films and ceramic dielectric and all the films are joined to a bus-bar rather than being connected in series). They are therefore ideal for high frequency decoupling. Disc ceramic capacitors, on the other hand, are sometime quite inductive, although less expensive.

The best way of ensuring that an analog circuit is adequately decoupled at both high and low frequencies is to use a tantalum bead capacitor in parallel with a monolithic ceramic one. The combination will have high capacitance but will remain capacitive at VHF frequencies.

There is little point in taking great care in the choice of a noninductive capacitor if it is then unsuitably mounted. As quite short lengths of wire have appreciable inductance HF decoupling capacitors must be mounted on short leads as close as possible to the points that they are decoupling—and their PCB tracks must also be as short and wide as possible. It is also important to understand where HF decoupling currents should flow and why HF decoupling is more important at some points than at others—there are additional comments on this in the operational amplifier section of the seminar.

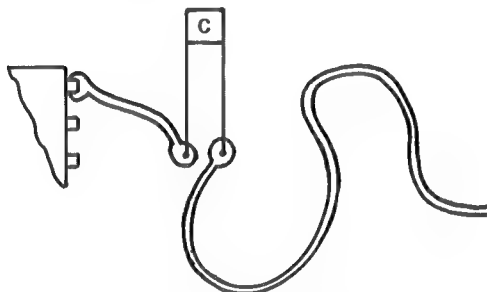
## HIGH FREQUENCY DECOUPLING (REQUIRED EVEN BY LF ANALOG CIRCUITS)



### IDEAL HF DECOUPLING HAS

1. LOW INDUCTANCE CAPACITOR (MONOLITHIC CERAMIC)
2. MOUNTED VERY CLOSE TO THE IC
3. WITH SHORT LEADS
4. AND SHORT, WIDE PC TRACKS

IT MAY BE SHUNTED WITH A TANTALUM BEAD ELECTROLYTIC TO PROVIDE GOOD LF DECOUPLING AS WELL.

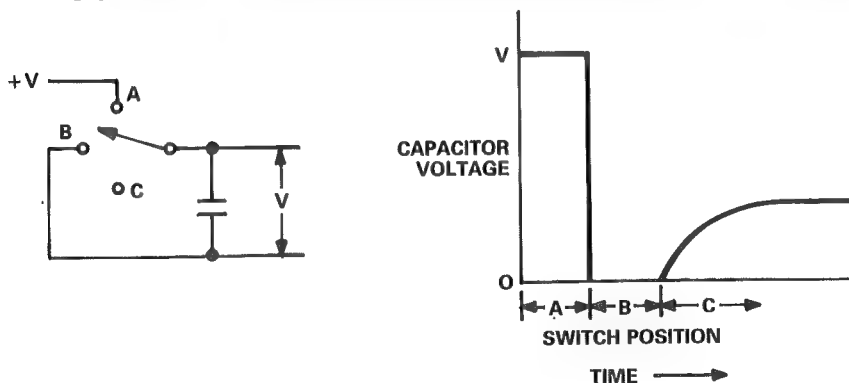


THIS SORT OF THING IS USELESS!

HF instability in analog circuits is commoner than is realized. Oscillation at hundreds of MHz will cause serious malfunction of precision circuitry but may not affect an oscilloscope (indeed the presence of an oscilloscope probe may damp the oscillation). It is quite good practice to use a broadband spectrum analyzer (say 1–1500MHz) and a low capacity FET probe to check for parasitic oscillation any analog circuit which is malfunctioning for no obvious reason. This test will also show if the malfunction is due to the presence of a strong RF field from an external source.

Monolithic ceramic capacitors are excellent for HF decoupling but they have considerable dielectric absorption, which makes them unsuitable for use as the hold capacitor of an SHA. Dielectric absorption causes a capacitor which is quickly discharged and then open-circuited to recover some of its charge. Since the amount of charge recovered is a function of its previous charge this is, in effect, a charge memory and will cause errors in any SHA where dielectric absorption is present in the hold capacitor.

## CAPACITORS HAVING SIGNIFICANT D.A. ARE USELESS FOR SAMPLE AND HOLD APPLICATIONS



**DIELECTRIC ABSORPTION CAUSES A BRIEFLY DISCHARGED CAPACITOR TO RECOVER A PERCENTAGE OF ITS PREVIOUS CHARGE ON BEING OPEN CIRCUITED.**

Capacitors for this application should therefore be selected to have minimal dielectric absorption. The best strategy is to use a SHA which is supplied with an internal capacitor or where the SHA manufacturer supplies the capacitor with the SHA. If this is not possible (sometimes one may require a longer hold time—and hence extra capacity) a capacitor should be chosen which has its low dielectric absorption (DA) specified on its data sheet.

Such capacitors are normally plastic dielectric types (polystyrene, polypropylene or teflon) but it is not safe to use just any plastic dielectric capacitor with a SHA as special processing and testing is necessary to ensure that it has low DA. For use with a SHA a capacitor should be chosen which is specified for use in SHAs.

## FEATURES OF COMMON CAPACITORS

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	0.1%	Small Case Size Inexpensive Good Stability Wide Range of Values Many Vendors Low Inductance	DA too High for More than 8-Bit Applications
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Destroyed by Temperature $> +85^{\circ}\text{C}$ Large Case Size High Inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Destroyed by Temperature $> +105^{\circ}\text{C}$ Large Case Size High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational Above $+125^{\circ}\text{C}$ Wide Range of Values	Relatively Expensive Large High Inductance

## FEATURES OF COMMON CAPACITORS

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
MOS	0.01%	Good DA Small Operational Above + 125°C Low Inductance	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Polysulfone	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-Bit Applications High Inductance
Monolithic Ceramic	>0.2%	Low Inductance Wide Range of Values	Poor Stability Poor DA
Mica	>0.003%	Low Loss at HF Low Inductance Very Stable Available in 1% Values or Better	Quite Large Low Values (<10nF) Expensive
Aluminium Electrolytic	High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability Poor Accuracy Inductive
Tantalum Electrolytic	High	Small Size Large Values Medium Inductance Reliable	Quite High Leakage Usually Polarized Expensive Poor Stability Poor Accuracy

### HORRIBLE EXAMPLES

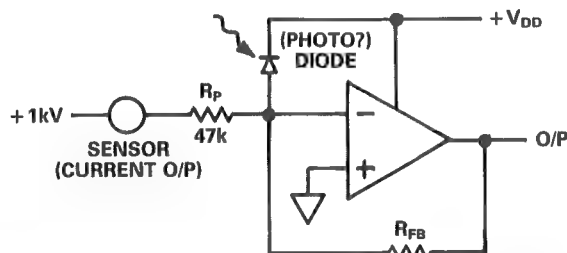
This section of our seminar has demonstrated how unconsidered aspects of well-known physical laws, especially Ohm's and Kirchoff's Laws, and the nonideal behaviour of passive components, can damage the performance of precision analog circuitry. We have also shown how circuit techniques which are appropriate for digital circuitry with noise immunities of hundreds or thousands of millivolts may be totally unsuited to precision analog systems where even millivolts of error may be too much.

This section could be extended almost indefinitely, particularly if we included case studies from Analog Devices' Application Department. They have some real horror stories to tell and it might be instructive to complete the section with two examples of how the laws of physics go on working even when one would rather that they didn't—and in the process can foul up quite well-considered designs. We shall call our studies "The Case of the Hum from Nowhere" and "The Case of the Two-Coloured Wire".

## THE CASE OF THE HUM FROM NOWHERE

When the signal source of an op amp contains an energizing voltage which is much higher than the op-amp supply it is common to use a diode and a current limiting resistor to protect the op amp in the event of a sensor short-circuit. In normal operation the diode is reverse biased and contributes only its (low) leakage current to the circuit but should the sensor be short-circuited the resulting current will flow through the diode to the op-amp supply rather than destroy the op amp. It is, of course, important to choose the resistor so that it neither degrades the noise performance of the system nor allows too much current to pass under fault conditions.

## THE CASE OF THE HUM FROM NOWHERE



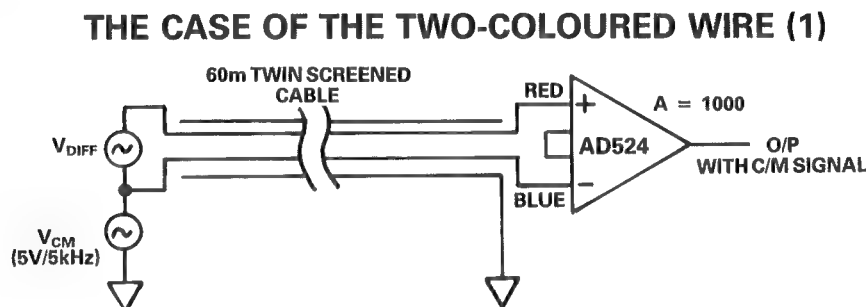
THE DIODE PROTECTS THE OP AMP UNDER FAULT CONDITIONS BY DIVERTING FAULT CURRENT (LIMITED BY  $R_P$ ) TO THE SUPPLY RAIL. THE DIODE SHOULD NOT BE PHOTO-RESPONSIVE, OTHERWISE FLUORESCENT LIGHTING MAY MODULATE ITS LEAKAGE CURRENT AT 100/120Hz AND CAUSE HUM. USE A PLASTIC DIODE – NOT A GLASS ONE.

We encountered such a system where about 10% of all the amplifiers built suffered from severe hum at twice the power line frequency. The customer, of course, blamed the op amp for poor supply rejection but analysis showed that even when the circuit was powered from batteries the problem persisted. The cause eventually turned out to be the protective diode—a 1N914 in a glass case.

About 10% of diodes from the particular manufacturer were quite active as photodiodes and when illuminated by fluorescent lights their leakage current was modulated at 120Hz—and the 120Hz was, of course, amplified with the sensor signal. Use of a black epoxy packaged diode provided a complete cure.

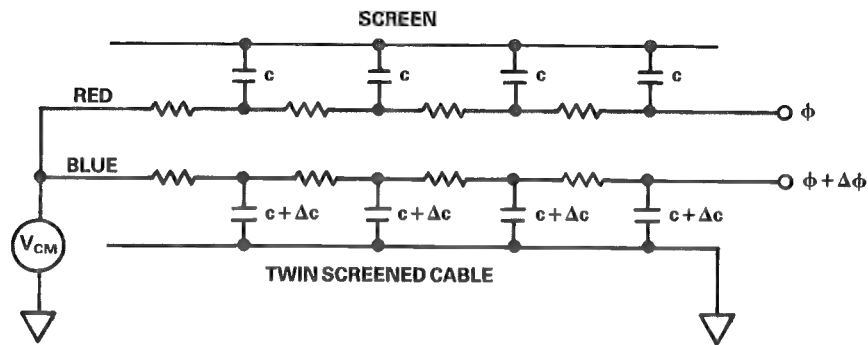
### The Case of the Two-Coloured Wire

Another customer complained that one of our instrumentation amplifiers did not have the common-mode rejection that we advertised. He was using the AD524 to amplify a small differential signal in the presence of several volts of 5kHz common mode and the signal was applied to it via about sixty metres of twin screened cable.



The problem was the result of differential phase shift in the cable. The red conductor has slightly thicker insulation than the blue, which accordingly has slightly more capacitance and therefore produced slightly greater phase shift to ac signals. A common mode 5kHz signal applied to one end of the 60 metre cable underwent a differential phase shift of a fraction of a degree in transit—this phase shift caused a small DIFFERENTIAL 5kHz signal at the instrumentation amplifier input in addition to the large common-mode signal. Unfortunately the differential 5kHz was about the same amplitude as the original wanted signal.

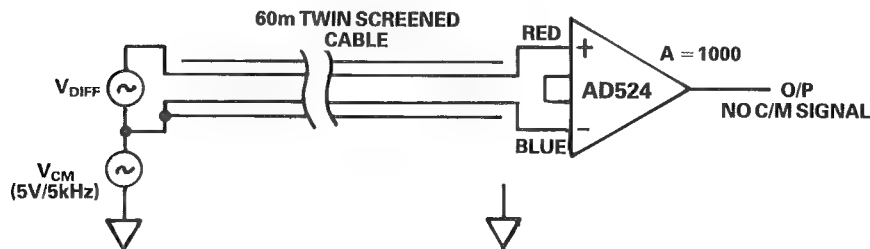
## THE CASE OF THE TWO-COLOUR WIRE (2)



DIFFERENTIAL PHASE SHIFT DUE TO DIFFERENCES IN CORE CAPACITANCE

The cure is to drive the screen of the cable with the common-mode signal (bootstrap it). Common-mode phase shift does not then take place and the instrumentation amplifier input contains only common-mode signals at 5kHz—which it rejects.

## THE CASE OF THE TWO-COLOUR WIRE (3)



The bootstrapping is most simply done (as in this case) by connecting the cable screen to the common-mode signal at the signal end of the cable. In some cases this is not possible and the shield must be driven by an additional buffer amplifier (known as a "shield driver") which is fed with common-mode signal, which can be obtained from the AD524.

## CONCLUSION

Such examples might be continued *ad infinitum* but the important message of this part of our seminar is that the design of precision analog circuits and systems follows the same physical laws as the design of any other electronic apparatus but that the priorities during such design depend on the high performance that we wish to achieve. The fundamental rules are:

### GROUND IS A DIRTY WORD ALL VOLTAGES ARE DIFFERENTIAL

ALL COMPONENTS HAVE EXTRAS  
(EXTRA INDUCTANCE, EXTRA CAPACITANCE, ETC.)  
BE GRATEFUL YOU ARE NOT CHARGES FOR THEM  
(IT'S ALL YOU HAVE TO BE GRATEFUL FOR)

NEVER BELIEVE DATA SHEETS

ALL THE LAWS OF PHYSICS ALWAYS WORK  
(THAT'S WHY THEY'RE CALLED LAWS)

ANY EFFECT YOU THINK CAN BE DISREGARDED – CAN'T

AN UNTESTED PAPER DESIGN IS WORTH LESS THAN ITS MATERIALS

AND FINALLY – MURPHY DIDN'T KNOW HALF OF IT

# **FABRICATION TECHNIQUES FOR PRECISION CIRCUITS**





Throughout the history of electronics system designers have used "integrated" circuits, that is to say functional blocks performing a particular task which are not redesigned for each occasion but reused repeatedly. The practice of naming circuits demonstrates this: "Colpitt's Oscillator", "Schmitt Trigger", and "Eccles-Jordan Multivibrator" being just a few examples. In the beginning people built these units for themselves, but very early on it became possible to buy ready-made circuit functions, packaged and tested, for assembly into larger systems.



The practice has continued to the present, but the functionality, complexity, and reliability of individual blocks has become steadily greater while their size, cost, and power consumption has steadily diminished. The invention in the early 1960s of the monolithic integrated circuit, where a number – today a very large number – of individual circuit elements and their interconnections are fabricated in a single minute piece of a semiconductor, accelerated the process enormously but was by no means the start of it. This section of our Seminar considers the different techniques used to manufacture precision analog circuit blocks today.

Prepackaged circuit elements are commonly grouped in four categories: boards, modules, hybrid integrated circuits, and monolithic integrated circuits. Why the term "integrated circuit" should be reserved for the last two is by no means clear, but the practice is too widespread to change.

## COMMON TYPES OF INTEGRATED CIRCUIT ELEMENT

<b>BOARD</b>	Function is sold, ready assembled & tested on a printed circuit board.
<b>MODULE</b>	Discrete components and encapsulated ICs are built into a circuit element using normal macro electronic assembly techniques – and then tested and encapsulated.
<b>HYBRID IC</b>	Unencapsulated chip components are assembled on a substrate or header (which may also carry thick- or thin-film circuitry), bonded to the package, substrate, and each other by standard integrated circuit bonding techniques, and then tested and packaged.
<b>MONOLITHIC IC</b>	Standard integrated circuit chip.

### BOARDS & MODULES

There is little difference between boards and modules, other than the obvious fact that you can see the components on a board, and we shall consider them together. Unencapsulated boards are preferred to modules in situations where there is high-power dissipation and free air flow minimizes temperature rises, and where the circuit element is intended to be mounted in a "card-mount" system.

## BOARDS & MODULES

### USE THE SAME CONSTRUCTION TECHNIQUES

### AND OFFER THE SAME ADVANTAGES & DISADVANTAGES

They differ only in their packaging or lack of it.

When prepackaged circuit elements first became available, they were all boards or modules. Today boards and modules are a minute percentage of the total market. Nevertheless, the absolute quantity and the value of the total number sold continues to rise – it is only their market share that has fallen. They continue to be used because they offer the ultimate in performance, they are easily customized, and they are often preferable to "home-brew" designs in having a guaranteed performance level.

## BOARDS & MODULES

### ADVANTAGES

- Highest Possible Performance
- Lowest Tooling/Development Cost
- Relatively Easily Customized
- Greatest Variety of Possible Components
- Greatest Opportunities for Adjustment
- Specified & Tested as a Complete Function

### DISADVANTAGES

- High Unit Cost
- Large Physical Size
- Slightly Lower Reliability

Boards and modules may use any type of component, even ones such as transformers and variable capacitors which are difficult or impossible to fabricate in hybrid or monolithic form. Their performance may be optimized during manufacture by component selection and adjustment, they may be reworked without difficulty during manufacture so their yields are very high, and they have relatively low tooling costs so they may quite easily be customized, even for short production runs.

On the other hand they are individually constructed, so their unit cost is high and large production batches offer few economies of scale. They are also relatively large and, because of their method of construction, slightly less reliable than a hybrid or monolithic circuit with the same functionality.

They are therefore used where their outstanding performance or the ease with which they can be customized in small quantities outweigh their disadvantages of cost and size.

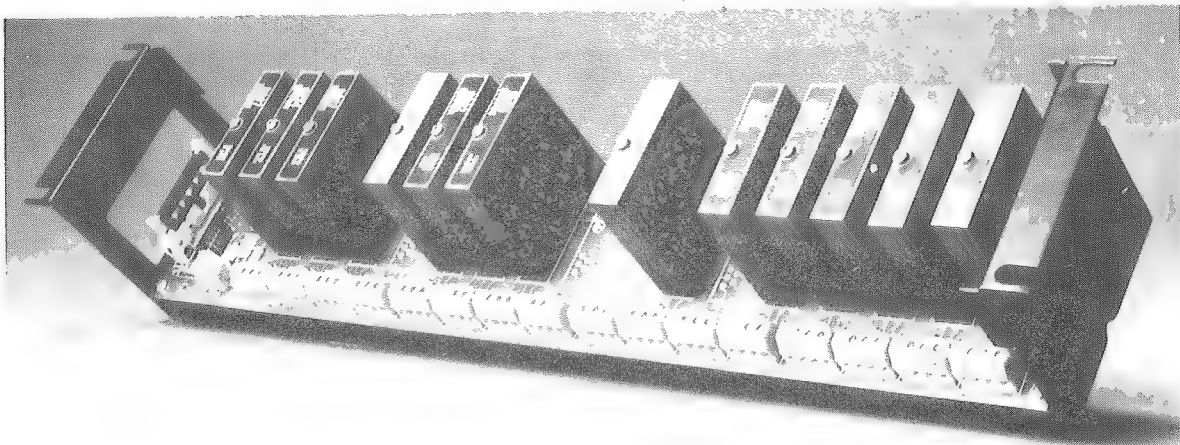
## **TYPICAL BOARD PRODUCTS**

**Very Fast High-Resolution Converters.**

## **TYPICAL MODULES**

**Electrometer Op-Amps  
Very High-Resolution Converters  
Isolated Functions (Large Voltages Possible  
Between Input & Output)  
Industrial Measurement & Control**

There is one area where the larger size of modules is an advantage, for instance, in industrial measurement and control where systems are assembled and serviced by electricians rather than electronic technicians. Modules are large enough and robust enough to be handled with normal tools and be installed with clamps and screw terminals and will survive in an industrial environment. ICs, on the other hand, must be handled and mounted with great care and are vulnerable to blows and corrosion. Thus, many manufacturers make ranges of modules for industrial applications which can easily be installed in the field. Some of them are very sophisticated, but others could easily be replaced with a single IC save for the advantages of robustness and ease of installation.



## **SURFACE MOUNT MODULES**

### **ADVANTAGES**

**Lower Cost than Conventional Modules  
Wider Component Range than Hybrids or Monolithic  
Automatic Assembly for Lower Unit Cost**

### **DISADVANTAGES**

**Economically Viable Only when Manufactured in Large  
Quantities Due to Higher Tooling Costs**

### **TYPICAL PRODUCTS**

**Isolation Amplifiers  
Industrial Modules  
Data Converters with Integral Computation**

**NOTE: These modules are fabricated using surface mount techniques – they are not necessarily mounted in this manner themselves.**

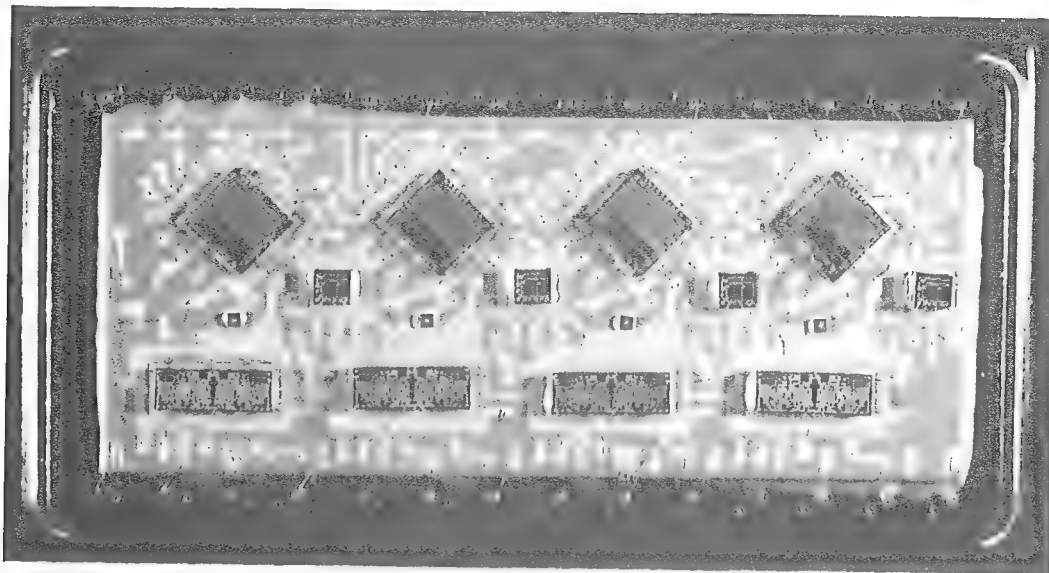
Within the last few years the introduction of electronic components in surface mount packages has revolutionized the automatic assembly of printed circuit boards and has created a new type of modular component – one which is manufactured in large quantities by these automated assembly methods and which contains components which are difficult or impossible to incorporate in hybrid or monolithic ICs. These modules, which are generally smaller than traditional modules, are often not trimmed or adjusted during manufacture and are therefore less expensive. Because of the greater tooling cost of such automated assembly, they must be manufactured in larger quantities to be viable. The first example of such modules was the AD202, an isolation amplifier of medium performance and very small size which costs about one third as much as an isolation amplifier of comparable performance built using conventional module assembly techniques.

## AD202 FEATURES

**Small Size: 4 Channels/Inch**  
**High Accuracy:  $\pm 0.05\%$  max Nonlinearity**  
**High CMRR: 150dB**  
**Wide Bandwidth: 5kHz Full Power**  
**High CMV Isolation:  $\pm 1000V$  pk Continuous**  
**Isolated Power Outputs**

## HYBRID INTEGRATED CIRCUITS

Hybrid integrated circuits are circuits built using the same assembly and handling techniques as monolithic ICs but containing more than one chip. They may vary in complexity from such circuits as the AD515 or the hybrid AD574, which contain just two monolithic chips, mounted in a package similar to that of a monolithic IC, and connected to each other and to the package pins, to the hybrids used in the most complex systems which contain hundreds of monolithic chips, capacitors, and other components, mounted on multilayer thick or thin film ceramic substrates carrying both precision and nonprecision resistors.



Hybrid circuits are smaller than modules (which means that they may have lower power ratings) and somewhat more reliable. They are assembled using microelectronic techniques of mounting and bonding rather than simpler, larger scale methods – which prevents the use of some types of component (large transformers, thermionic tubes and large variable capacitors come to mind – though Analog Devices' Memory Devices Division does manufacture hybrids containing several small 400Hz signal transformers per hybrid). Their main advantages from the manufacturer's viewpoint are that they allow the use of several different IC technologies in a single device to produce devices which would not be possible in monolithic technology, they may be reworked (to a certain extent) during manufacture, and they tend to have shorter development times and lower development costs than monolithic circuits and so may get to market sooner and for less development cost. To counter these advantages they are more expensive to manufacture (since they can rarely be assembled automatically and are more complex in structure than monolithic circuits).

# HYBRID INTEGRATED CIRCUITS

## ADVANTAGES

**Small Size**  
**High Performance**  
**Shorter Development Times**  
**Can Use Several Technologies at Once**

## DISADVANTAGES

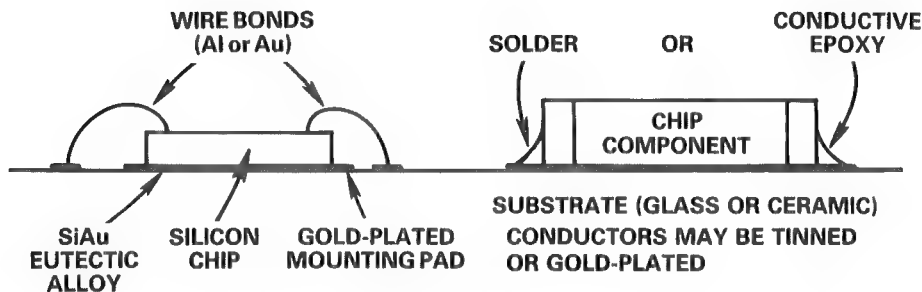
**Higher Price than Monolithic ICs**  
**Very Slightly Lower Reliability**

From the user's point of view, though, the manufacturer's problems are irrelevant. In a hybrid IC, the user finds high performance of a complex function in less space (generally no larger than the package of a monolithic IC), at a lower price, and with higher reliability than a module. The user does not usually care whether a particular function is performed by a monolithic or a hybrid circuit – provided it is performed well at an economic price. It is quite common for circuits to start their production life as hybrids and be integrated on a single monolithic chip after a few years – either because the technology to do so has only just become available or because the volume required by the market has made economic the development of a monolithic version.

The components used in hybrid ICs are monolithic semiconductor chips (mounted and unmounted and both ICs and discrete devices), chip capacitors, chip resistors, and thick- and thin-film resistors. There are also less common components such as inductors and miniature transformers. These components may be mounted directly onto the metal or ceramic header of the device package or onto a glass or ceramic substrate carrying single- or multi-layer conductors and thick-film resistors, thin-film resistors, or both (thin-film resistors are made of metal film deposited on the substrate by chemical means such as evaporation, sputtering, or electroplating and have high stability and high accuracy, while thick film resistors, which are slightly less stable and accurate but available in a wider range of values, are made from a conductive paint or paste [made from metal powders or metal oxides and sometimes, but not always, fired after application to produce a conducting ceramic] which is painted, sprayed, or silk-screened onto the substrate – both types can be trimmed to improve accuracy and matching).

The components may be mounted by solder, adhesive, or conventional chip bonding (where a low melting-point silicon-gold alloy is formed by scrubbing the silicon chip on a heated gold-plated area where it is to be mounted – this eutectic alloy solders the chip to the substrate or header). Electrical connections are made to unencapsulated silicon chips by standard wire-bonding techniques and to other components by solder or, occasionally, conductive adhesives or paints – normally components other than unencapsulated chips have their electrical connection made by their mounting material.

## MOUNTING COMPONENTS IN HYBRID ICs



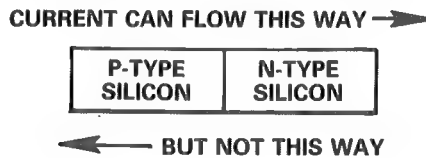
After assembly hybrid circuits may be tested before the package is closed – and components replaced if necessary. The package is filled with dry air or dry nitrogen before being sealed. The caps of hybrid packages are generally attached by soldering, resistance welding, or, occasionally, with adhesives.

## MONOLITHIC INTEGRATED CIRCUITS

The silicon monolithic integrated circuit has revolutionized electronics, and society, over the last quarter century. By using essentially simple physical/chemical processes of epitaxial growth, diffusion, and selective etching, it has been possible to build and interconnect millions of electronic circuit elements in a single small "chip" of silicon.

The processes involved are, by now, well known. If we have ultra-pure monocrystalline silicon and add controlled, and very small, amounts of group III (boron) or group V (phosphorus or arsenic) elements as impurities the conductivity of the silicon is increased and the "doped" silicon is said to be P-type or N-type respectively. If two adjacent regions in a silicon crystal are P-type and N-type, their interface is known as a "junction" and has useful electrical properties – the most obvious being that it is a diode and allows current to flow from P to N but not the other way. By controlling the doping and the geometry of the doped regions it is possible to fabricate various different electronic components in the silicon.

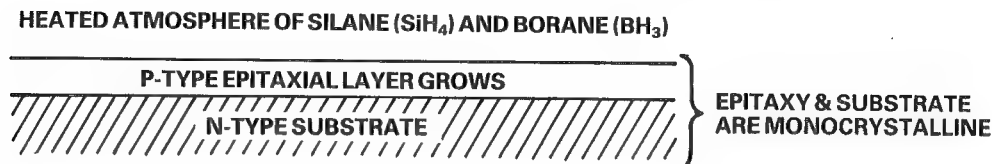
## BASIC SILICON JUNCTION (DIODE)



There are two common ways of forming junctions, epitaxy and diffusion. Epitaxy consists of growing silicon of one type on a substrate of another type. This is done by heating the substrate in an atmosphere of silane ( $\text{SiH}_4$  – the silicon analog of methane) containing a little phosphine, arsine, or borane to provide the dopant. If this is done correctly an "epitaxial layer" of new silicon grows on the existing silicon and the whole structure, new and old, is monocrystalline. If the correct dopant is used the new silicon will be of the opposite type to the old and a junction occurs at their interface.

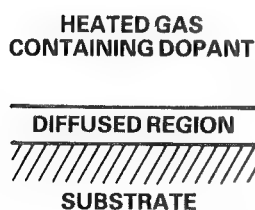
## EPITAXIAL GROWTH

(P ON N IS SHOWN – N ON P IS EQUALLY POSSIBLE)

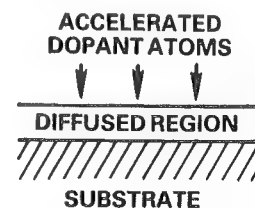
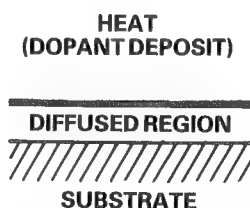


A diffused junction is formed by heating silicon of one type in the presence of the material producing the other type (N-type silicon is heated with boron or borane, P-type with arsenic, phosphorus, arsine or phosphine). Dopant atoms migrate into the silicon to produce a region of the other type. Diffusion may also be accomplished by "ion implantation" where atoms of the dopant are accelerated in a particle accelerator and allowed to strike, and penetrate, the surface of the silicon – ion implantation can give better control of both diffusion depth and density profiles and makes possible better devices than can be achieved by older methods of diffusion.

## METHODS OF DIFFUSION



TRADITIONAL DIFFUSION METHODS

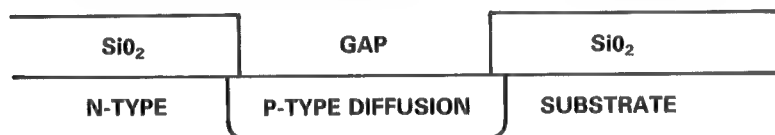


ION IMPLANTATION



The critical feature which makes silicon integrated circuits so complex is the ability to mask the surface of the silicon so that diffusion occurs only in certain areas. If silicon is heated in oxygen or steam it oxidizes and forms a thin coherent layer of silicon dioxide ( $\text{SiO}_2$  or silica) over its surface. If this layer is etched away in places before diffusion takes place, then the dopant will only reach the silicon where the oxide has been removed – which allows us to determine where diffusion will occur. This layer of silica also insulates any conductors deposited on it from the underlying silicon.

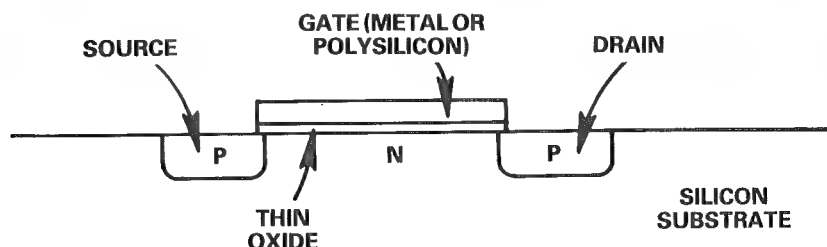
## MASKING THE CHIP WITH SILICA ALLOWS DIFFUSION TO BE SELECTIVE



Very thin layers of this silicon dioxide also form the “gates” of a particular type of field-effect transistor called a “metal-oxide-silicon” field-effect transistor or MOSFET.

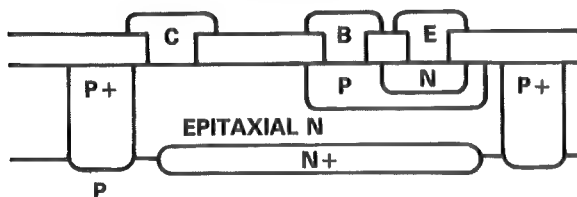
## MOS (METAL OXIDE SILICON) TRANSISTOR

This is a P-Channel One – N-Channel Types are Equally Possible

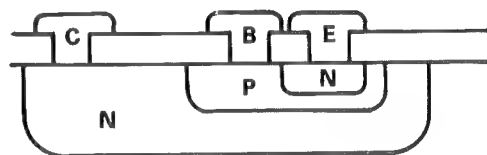


Using only diffusions and thin oxides we can produce a variety of different electronic devices in the surface of a chip of silicon. These include transistors (junction, field effect, and MOS), diodes, zener diodes, resistors (long thin strips of diffusion), and small capacitors (which may be formed either from the capacity of reverse-biased junctions or as parallel plate capacitors with thin oxide as the dielectric).

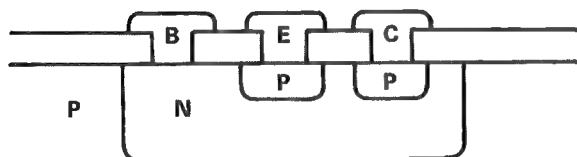
## SOME STRUCTURES USED IN MONOLITHIC ICs



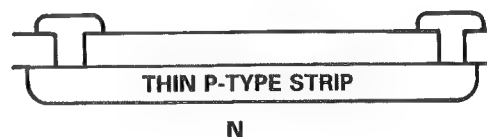
**NPN EPITAXIAL TRANSISTOR**



**NPN DIFFUSED TRANSISTOR**



**PNP LATERAL TRANSISTOR**



**RESISTOR**

These devices are connected together by aluminum conductors formed by coating the whole chip with aluminum and then etching it to the required pattern. Chips are manufactured hundreds or thousands at a time on a “wafer” of silicon which is cut up into individual chips after all the manufacturing processes are complete.

There are many different kinds of monolithic integrated circuit processes. Each has its own advantages and disadvantages and it is virtually impossible to make all types of integrated circuit components on a single chip. We are not concerned in this seminar with purely digital techniques but it is worth noting that the development of digital integrated circuits has involved increases of packing density from tens of devices per chip in the mid-sixties, when the first commercial ICs became available, to around ten million devices per chip today. Analog chips have developed differently.

The purpose of a precision analog IC is to perform with high analog accuracy. In the quarter century since the first analog ICs were sold, the improvement in accuracy and functionality has matched that of digital circuits but this has not involved comparable increases in component density. Today’s most complex analog chips rarely contain more than ten thousand devices and frequently no more than a few hundred – but their performance would have appeared impossible a decade ago.

Developments in circuit technology for precision analog applications concentrate on precision, accuracy and stability rather than packing density. It is well known that if two transistors have identical geometry and are fabricated close together on the same chip they are likely to be well matched – but to improve that match has taken years of study and experiment in processing, device geometry, and material sciences.

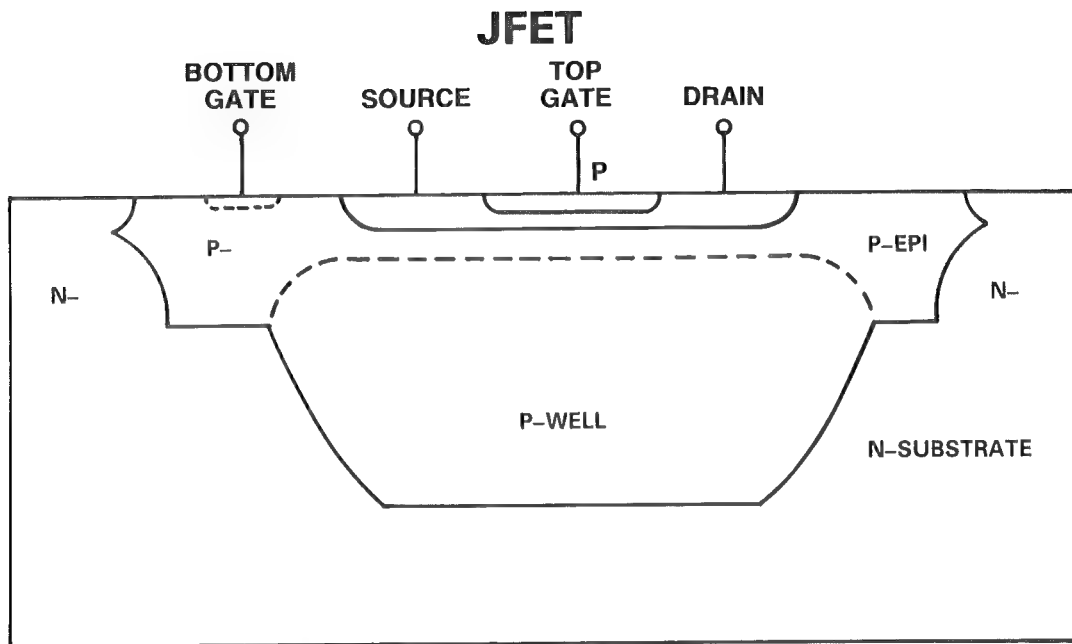
At Analog Devices we started our precision analog circuit manufacture with two processes: an epitaxial bipolar process and a CMOS process. The bipolar process makes good NPN transistors and resistors, and fairly good PNP transistors and is therefore excellent for low-frequency amplifiers and computational circuits but does not make particularly good logic.

CMOS, on the other hand, makes only P-channel and N-channel MOS devices. CMOS is excellent for logic and switches with high speed and low dissipation but is unsuitable for amplifiers since it is noisy and has poor offset matching.

	<b><u>BIPOLAR</u></b>	<b><u>CMOS</u></b>
<b><u>Devices</u></b>	NPN & PNP transistors Zener Diodes Resistors	N- & P-Channel MOS (Sometimes) NPN Transistors Resistors
<b><u>Advantages</u></b>	Low Noise Low Amplifier Offsets Good References	High Speed, Low Power Logic High Density Low Ron Switches Bidirectional Switches
<b><u>Disadvantages</u></b>	Poor, Low Density Logic High Amplifier $I_b$ Unidirectional Switches	Poor Noise Performance Poor Offsets No References

The disadvantages of each process led to our process engineers working to overcome them. The first improvement to the bipolar process was to allow it to produce junction field-effect transistors (FETs). Unlike a bipolar transistor an FET does not have a base current proportional to its collector current but only a small gate current resulting from reverse leakage in the gate diode. Amplifiers made with this BiFET process could therefore have much lower bias currents – but at the cost of poorer offsets and bias currents which doubled for every 10°C temperature rise. Because the collector (drain) currents of the input devices are no longer proportional to their bias currents it is unnecessary in FET input amplifiers to limit the current (and hence the frequency response) of the input stages in order to limit the bias current – BiFET amplifiers, therefore, are frequently faster than bipolar ones.

	<b><u>BiFET</u></b>
<b><u>Devices</u></b>	JFETs NPN & PNP Transistors Zener Diodes Resistors
<b><u>Advantages</u></b>	Low Noise Low Bias Current High Frequency Operation Good References
<b><u>Disadvantages</u></b>	Offset Voltages Worse than Bipolar (But Much Better than CMOS) Bias Currents Double Every °10°C Bias Currents Ill-Matched Worse Offset TC



JFETs do little for logic circuitry. The next development was to create a bipolar process which could also make MOS devices of both polarities – a bipolar plus CMOS process. This process, called BiMOS II (since it is now in its second generation), is a non-epitaxial process which will make a wide range of components and is as good a logic process as it is an analog one.

## BiMOS II

### Devices

N-MOS & P-MOS FETs  
JFETs  
NPN & PNP Transistors  
Resistors

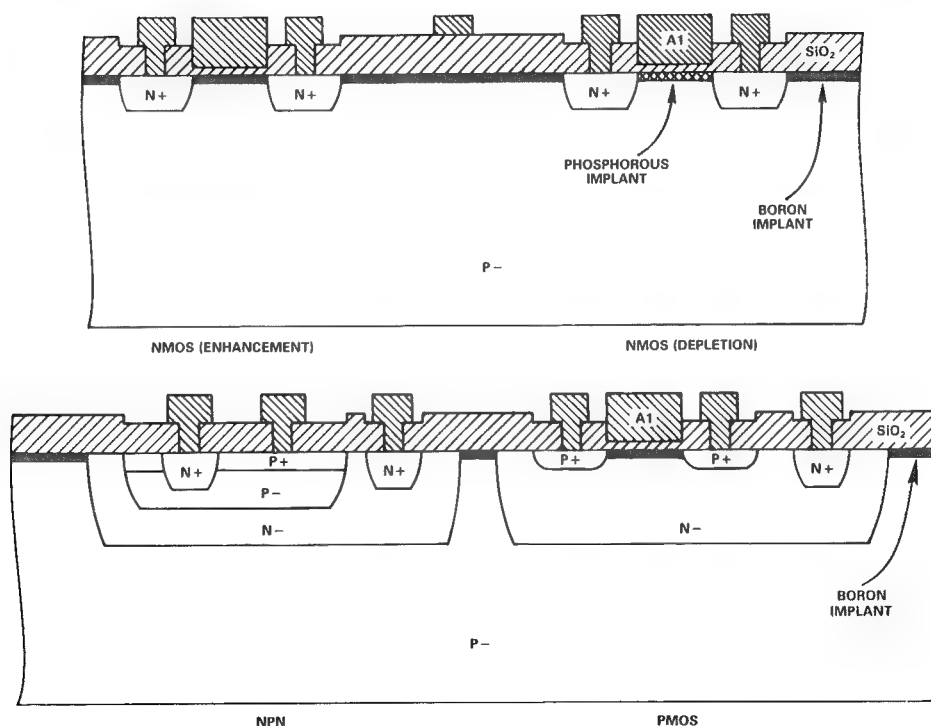
### Advantages

Excellent Amplifiers  
Excellent Logic

### Disadvantages

Greater Process Complexity  
No Buried Zener Diodes  
Limited Voltage Ratings

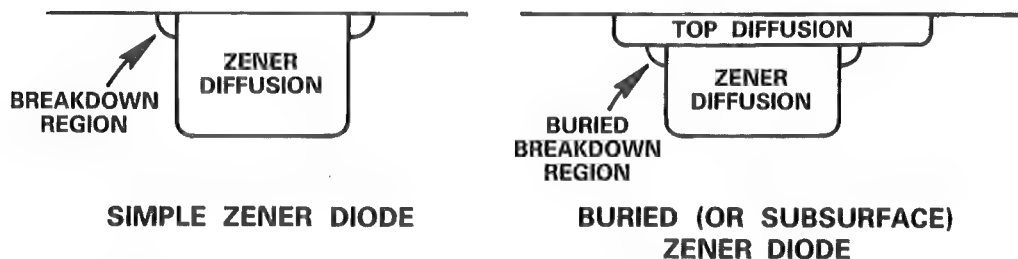
## CROSS SECTIONAL VIEW OF BIMOS II PROCESS



Two minor drawbacks of BiMOS II are its lower breakdown voltages (which prevent it from being used with  $\pm 15V$  supplies without special circuit techniques) and its inability to make a buried zener diode.

Buried zener diodes make a major contribution to the accuracy and stability of precision analog circuitry. A zener diode is a diode which is fabricated to have a reverse breakdown voltage which is quite accurately defined and is used as a reference. Zener diodes are frequently noisy and unstable. If we consider the structure of a simple zener diode we can see why this should be so.

## ZENER DIODE STRUCTURES



**Impurities, Mechanical Stress and Crystal Lattice Dislocations Near the Surface of the Silicon Cause a Zener Diode There to Be Noisy and Unstable. If the Diode is Buried Below the Surface Region, Its Performance Will Greatly Improve.**

The breakdown of a simple zener diode takes place at the surface of the silicon. Near the surface there are more impurities, mechanical stresses, and crystal lattice dislocations – all of which contribute to noise and long-term instability. (It is interesting to look at an operating planar zener diode in the dark. It is sometimes possible to see a point electroluminescence at the zener breakdown point – this often jumps around the periphery of the diffusion in an unpredictable way, indicating noisy operation of the device.) If we place a diffusion over the zener diode diffusion it is possible to cause the zener breakdown to occur below the surface of the silicon in a region with far fewer impurities, stresses and lattice dislocations. The resulting zener diode is less noisy and has far better long-term stability. The diffusion used to bury the zener may be of the same or the opposite type to the one it is burying, depending on the process.

The AD588 monolithic reference, which uses a buried zener diode as its primary reference, has an absolute accuracy of better than 100ppm and a temperature coefficient of under 1.5ppm/°C.

## AD588 FEATURES

### FEATURES

- Low Drift – 1.5ppm/°C
- Low Initial Error – 1mV
- Pin-Programmable Output
  - +10V, +5V,  $\pm 5V$  Tracking, -5V, -10V
- Flexible Output Force and Sense Terminals
- High Impedance Ground Sense
- Machine-Insertable DIP Packaging
- Guaranteed Long-Term Stability – 25ppm/1000 hours

The CMOS process engineers were not resting while the bipolar engineers were working towards BiMOS II. They started with a simple CMOS process which made excellent CMOS devices and laser-trimmed resistors (which we shall discuss later in this section) and nothing else – this makes for excellent logic, switches and MDACs, but lousy amplifiers and no references.

They therefore developed Linear Compatible CMOS (LCCMOS or LC<sup>2</sup>MOS) which added PNP and NPN bipolar transistors, buried zener diodes and N-channel JFETs to the basic P-channel and N-channel MOS FETs of the CMOS process. This has added the possibility of making amplifiers, comparators and references on CMOS chips and therefore greatly increased the range of practicable monolithic devices.

## LC<sup>2</sup>MOS

### Devices

NMOS, PMOS, JFET  
PNP & NPN Transistors  
Resistors  
Zener Diodes

### Advantages

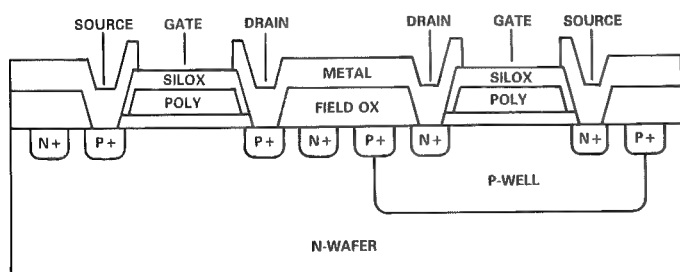
Excellent Logic & Switches  
Good Amplifiers & Comparators  
Quite Good References

### Disadvantages

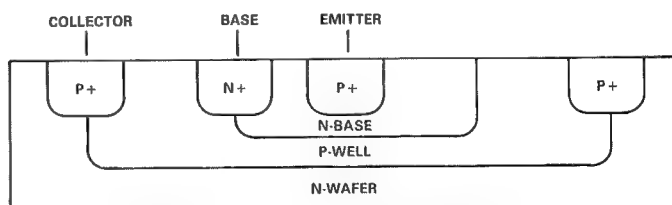
Greater Process Complexity  
Limited Analog Output Drive  
Limited Speed in Analog Structures

## LC<sup>2</sup>MOS PROCESS

### CMOS ELEMENTS

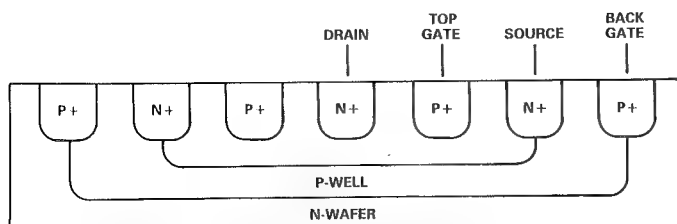


### PNP BIPOLAR TRANSISTOR



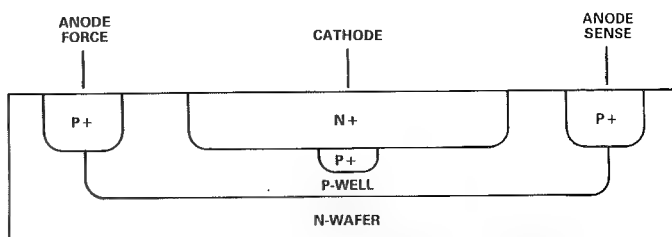
- Breakdown Voltage 10V
- Beta 130
- Ft 1GHz
- Noise 2nV/ $\sqrt{\text{Hz}}$  at 1kHz
- Match 100 $\mu\text{V}$

### N-CHANNEL JUNCTION FET



- Breakdown Voltage 8V
- Vp2V
- Match 20mV
- Noise 9nV/ $\sqrt{\text{Hz}}$  at 1kHz
- Leakage 1nA at 125°C

### BURIED ZENER DIODE



- Vz 6.1V
- TC +25mV/°C
- Noise 60nV/ $\sqrt{\text{Hz}}$  at 1kHz

It would seem as we consider these process developments that quite soon the BiMOS and the LC<sup>2</sup>MOS processes will converge and become identical and thereafter all precision analog circuits will be manufactured with this ultimate process. This is not about to happen.

For many circuits, the basic bipolar and CMOS processes are more than adequate. They do not require the extra features of the more complex processes – and they can be made more cheaply by not using the extra complexity (BiMOS has twice as many diffusion steps as the basic bipolar process – and therefore requires the generation of twice as many masks). Moreover, although both BiMOS II and LC<sup>2</sup>MOS have excellent analog and digital characteristics, they are still, respectively, primarily analog and primarily digital processes and the type of product for which each is best suited does differ markedly.

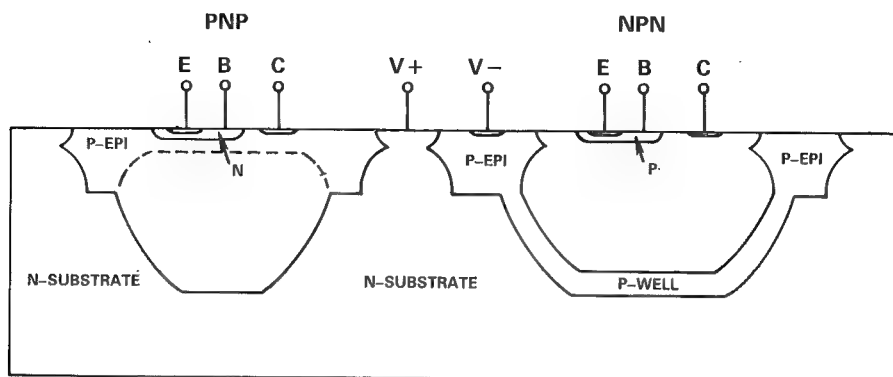
Therefore, while we can expect to see continual convergence of process parameters, two different lines of development will continue for the foreseeable future. We can also expect to see the older, simpler, cheaper processes continuing to be used in the many new designs which will not require the advanced features of the newer processes.

Meanwhile another development is taking place. A major limitation on the speed of monolithic circuits is the difficulty of fabricating PNP transistors which are as fast as the NPN ones on the same chip (or vice versa – but usually it is the NPNs which are fast). Level shifters and output stages, which perform best when manufactured with complementary transistors, are therefore much more difficult to design.

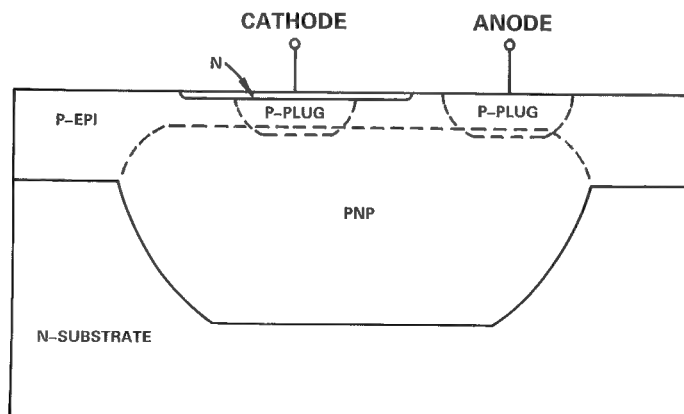
## DIELECTRIC ISOLATION



### CB COMPLEMENTARY TRANSISTOR PAIR



## CB BURIED ZENER



Although the CB process permits the manufacture of far faster complementary circuits than has hitherto been possible, the  $F_t$  of transistors made with it remains under 1GHz. Where even faster precision circuitry is required, another new process, using very small geometries and very precise ion implantation, allows the fabrication of NPN transistors with  $F_t$  of around 3GHz (PNP  $F_t$  in this process is only 25MHz) while still retaining the features required for precision circuitry: precise offset and beta matching and the ability to fabricate laser-trimmed SiCr resistors on the chip without compromising its other features. This is known as the “Flash” process.

## FLASH PROCESS

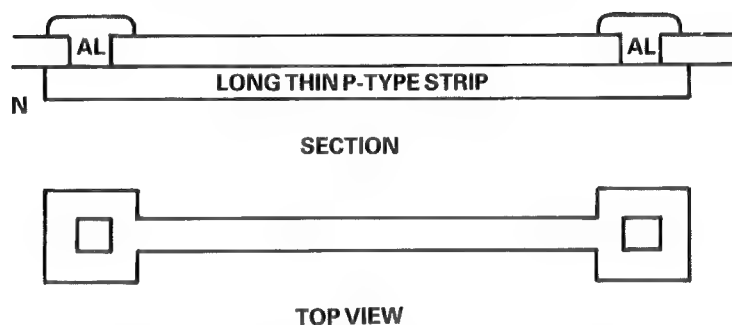
<b><u>Devices</u></b>	<b>3GHz NPN Transistors 25MHz PNP Transistors Laser-Trimmed Resistors</b>
<b><u>Advantages</u></b>	<b>Very High Speed High Precision Low Noise</b>
<b><u>Disadvantages</u></b>	<b>Limited Voltage Rating Relatively Slow PNPs</b>

In addition to its slow PNP transistors, the small geometry of the flash process limits its breakdown voltage but these disadvantages are trivial beside its blinding speed and analog precision. It is being used to design a range of amplifiers and multipliers whose performance will greatly exceed anything which has hitherto been possible, either in hybrid or monolithic form.

There are other details of the design and manufacture of precision analog integrated circuits which we do not have time to discuss in this brief summary (device geometries are optimized for analog performance, not minimum size, – which is why one sees so many round transistors in amplifiers and so few in microprocessors; transistors only match if they really are at the same temperature – so temperature gradients on a chip are sometimes of critical importance, which causes analog designers to lay out for minimum temperature gradient in critical areas rather than for minimum chip size; and voltage drops of millivolts in current-carrying conductors MATTER). There remains one feature of precision analog integrated circuits which must be discussed as it is critical to their performance: precise stable resistors.

Traditionally, resistors on integrated circuits have consisted of a long thin strip of diffusion biased so that it is isolated from the silicon in which it lies.

## DIFFUSED RESISTOR



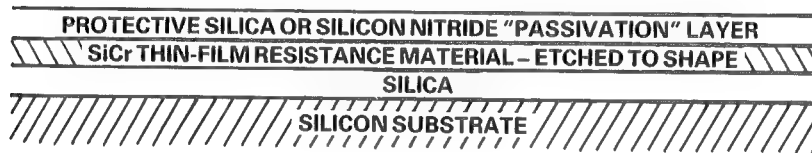
**If the N-Type Material is More Positive Than the Resistor, it Will Obviously Be Isolated From It.**

The accuracy of such resistors is pretty poor and they have large temperature coefficients. The matching of two adjacent and similar resistors can be around 1% but on the whole they cannot be considered precision parts. Nevertheless, with the greatest care in both design and processes it is possible to make a DAC with diffused resistors which has a DNL of 12-bits and an INL of 11-bits. To do better requires different techniques.



Analog Devices uses thin-film resistors deposited on the silica layer of the chip. These resistors are evaporated onto the silica and then photo-engraved to shape just like the aluminum conductors on the chip. They are made with an alloy of Silicon (Si) and Chromium (Cr) and are known as SiCr resistors. They have a temperature coefficient of well under 50ppm/°C and matching accuracy of 0.1% (their overall accuracy is only about 15% – this is because they are manufactured for minimum TC rather than maximum accuracy and the two requirements may conflict).

## THIN-FILM RESISTOR ON A CHIP



Accuracy	15%
Matching	0.1%
(May Be Laser-Trimmed to	<0.01%)
TC	<50ppm/°C
TC Matching	<0.25ppm/°C

Using such precise resistors it is possible to manufacture 8-bit and 10-bit ladder networks and even DACs with 16-bit DNL (but only 13-bit INL). But these resistors have another feature which enables us to make far more accurate components, and to use them to make very precise amplifiers and computational circuits: they can be trimmed to better than 0.01% during manufacture.

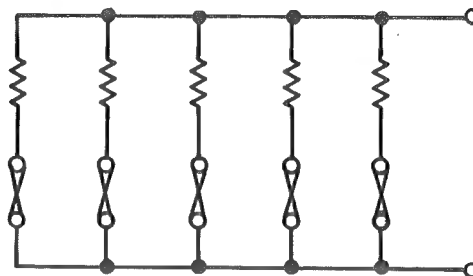
There are three commonly-used methods of trimming an analog IC: fusible links, zener zap, and laser trim. The first two are quantum processes – that is to say, they allow a resistor to be switched in or out of circuit during the manufacturing process. If there is an array of resistors, quite an accurate trim may be possible but it is inherently quantized. Laser trim allows adjustment with virtually infinite resolution.

In a fusible link trim each resistor is connected in series with a very narrow link of aluminum conductor. Each resistor which is not required has its conductor pulsed with a current high enough to fuse the link. While effective, this technique is dirty – it contaminates adjacent areas of the chip with flecks of aluminum – and is not popular for precision analog applications where such contamination may cause long-term instability.

## TWO QUANTIZED METHODS OF TRIMMING RESISTANCE DURING INTEGRATED CIRCUIT MANUFACTURE

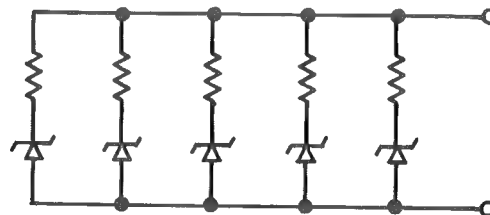
### FUSIBLE LINKS

When Fuses Are Blown, They Open-Circuit Their Resistor But May Contaminate the Chip Surface with Vaporized Aluminum.



### ZENER ZAP

Non-Contaminating But Still Quantized

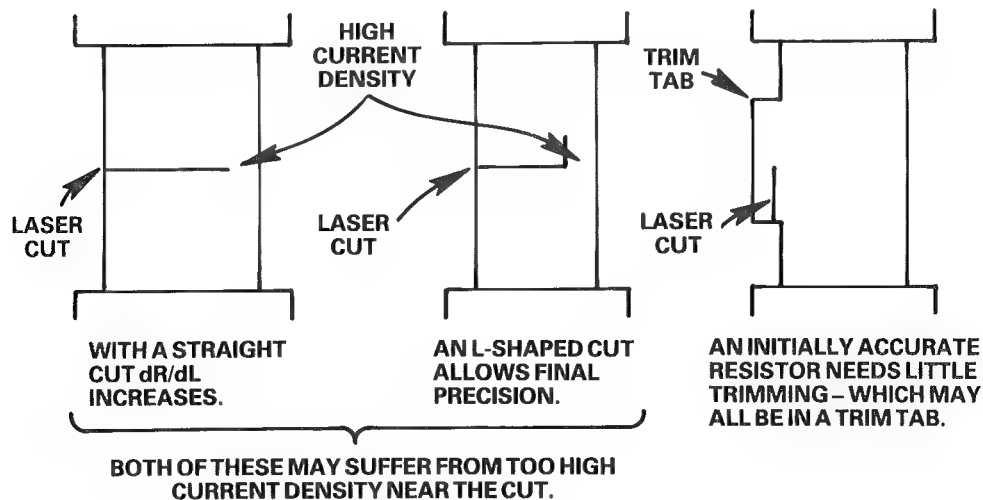


Zener zap is similar but the aluminum link is replaced with a very small diffused zener diode. When this zener diode is destroyed by a current pulse there is no visible damage and no debris to cause contamination. Many manufacturers who have not mastered the problems of laser trim use zener zap to trim the offset of operational amplifiers and where Analog Devices second-sources such amplifiers we use the same technique (for example, in the AD OP-07). In general, though, we find that the greater resolution and control of laser trimming offers major advantages.

This trimming is done by cutting a slot in the resistor with a laser. The basic idea seems simple – after all, Darth Vader has a laser and he blows up planets with his – but is in fact extremely demanding. Since many of the techniques involved are unpatentable it is not possible to give explicit details of the process but a number of points must be considered.

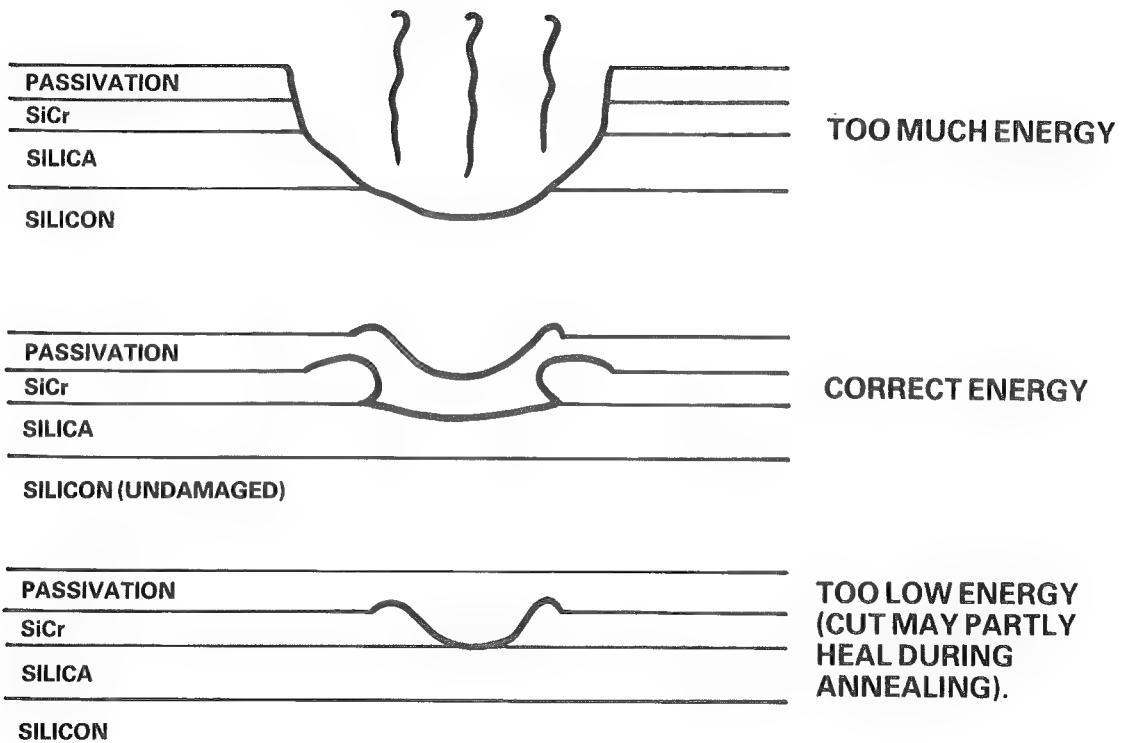
1. The resistor material – it must have good electrical characteristics and long-term stability (even after trimming) and must cut cleanly.
2. The shape of the resistors, and the geometry of the cut by which they are trimmed – if the resistor is initially inaccurate, a large trim will be necessary, but if we just cut across the resistor, the rate of change of resistance with cut will rise as the cut continues until just when we require greatest precision we have the greatest rate of change. An L shaped cut helps with this last problem but an initially accurate resistor which requires little trimming makes the task far more easy – it may be trimmed with a single cut on a special “trim tab” on the side of the main resistor.

## LASER TRIM – GEOMETRIES



3. The laser spot size and shape.
4. The laser energy – should it be pulsed or continuous, and, if pulsed, at what energy and what rate? (Too much energy will damage the silica substrate and the underlying silicon and may perforate the passivation; too little will leave resistor material in the cut which may migrate and cause long-term instability.)
5. The laser wavelength – both for optimum energy transfer and to avoid unwanted interference, effects in the transparent passivation and substrate layers (which have thicknesses comparable with the wavelength of the laser light).
6. Etcetera, etcetera, etcetera, and so forth.

## LASER TRIMMING – ENERGY



To summarize, the ability to fabricate, and laser trim, very precise and stable thin-film resistors, enables Analog Devices to make the most advanced precision monolithic analog ICs in the world. Well-defined and stable semiconductor processes are very important, but the most critical technology, and one which we have spent fifteen years developing and improving, is our ability to make, and trim, precise, stable resistors on the chips of all our different semiconductor processes.

# **OPERATIONAL AMPLIFIERS**



# OPERATIONAL AMPLIFIERS

## CONTENTS

- Basic Amplifier Types
- Specifications and Testing
- Amplifier Architectures
- Linearity and Distortion
- Error Sources
- Applications
- Feedback Techniques



# OPERATIONAL AMPLIFIERS

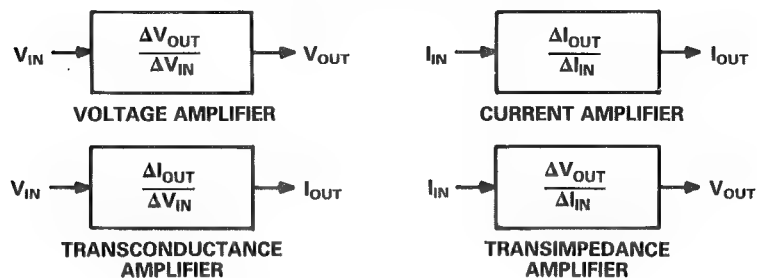
## INTRODUCTION TO AMPLIFIERS

This part of our seminar discusses amplifiers, their specifications, electrical characteristics, physical realization and applications. The greatest attention is paid to the integrated circuit forms of both operational and trans-impedance amplifiers, emphasizing stability, linearity, harmonic distortion, device design, gain, bandwidth, grounding and noise. The application and selection of specific devices for use in active bias networks will also be discussed.

## CLASSES OF AMPLIFIERS

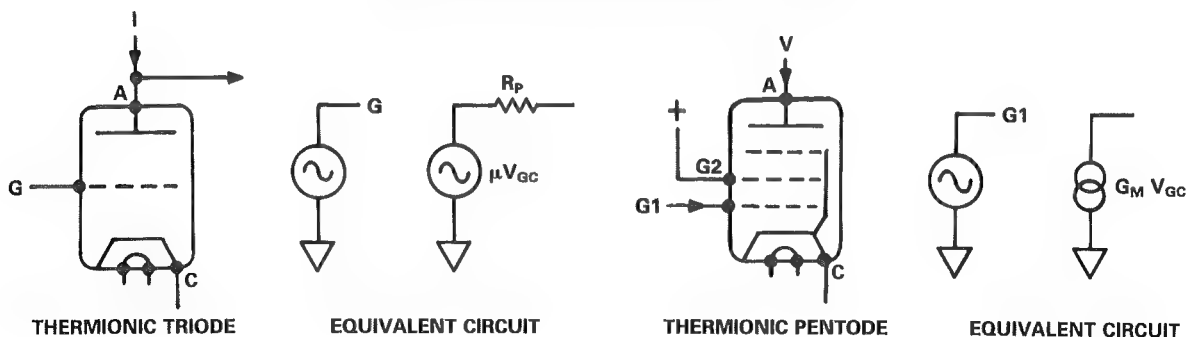
There are four general classes of amplifier, characterized by transfer characteristics expressed in volts per volts, amperes per ampere, volts per ampere, and amperes per volt.

## TYPES OF AMPLIFIERS



These basic amplifiers are the building blocks required to synthesize larger electronic systems. The earliest form of man-made amplifier was the triode vacuum tube, a voltage amplifier, designed by the English inventor Lee DeForest in time for World War 1. The triode is an effective amplifier but has limitations which led to the development of the pentode vacuum tube—a transconductance device. These two vacuum tube devices can be modeled as a voltage dependent voltage source and a voltage dependent current source respectively.

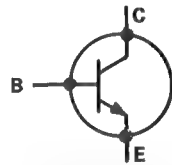
## VACUUM TUBE AMPLIFIERS



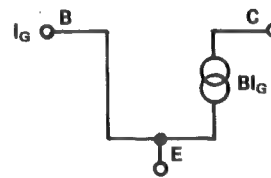


Today vacuum tubes have largely been displaced by transistors, both bipolar and field effect. These are used both as stand alone devices and incorporated into integrated circuits. Although there are simple electronic devices which are voltage amplifiers (the triode vacuum tube), current (the bipolar transistor), and transconductance amplifiers (the pentode vacuum tube and the field effect transistor), there are presently no electronic devices known which demonstrate the intrinsic characteristics of a transimpedance amplifier. Hence transimpedance amplifiers must be synthesized from voltage, current or transconductance amplifiers.

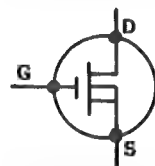
## DISCRETE SEMICONDUCTOR AMPLIFIERS



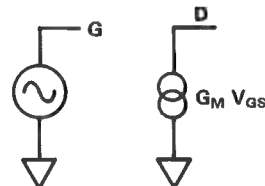
(NPN) BIPOLAR TRANSISTOR



EQUIVALENT CIRCUIT



FIELD EFFECT TRANSISTOR (FET)



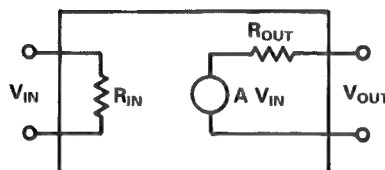
EQUIVALENT CIRCUIT

The general forms of the aforementioned amplifiers are modeled by applying Norton and Thevenin equivalent networks.

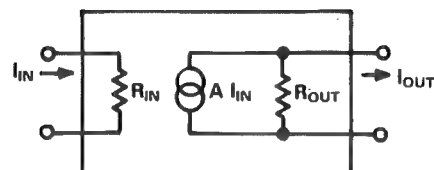
## IDEAL AMPLIFIER CHARACTERISTICS

	AMPLIFIER TYPE			
	VOLTAGE	CURRENT	TRANSCONDUCTANCE	TRANSIMPEDANCE
TRANSFER FUNCTION	$V_O = A V_{IN}$	$I_O = A I_{IN}$	$I_O = G_M V_{IN}$	$V_O = R_M I_{IN}$
$R_{IN}$ $R_{OUT}$	$\infty$ 0	0 $\infty$	$\infty$ $\infty$	0 0

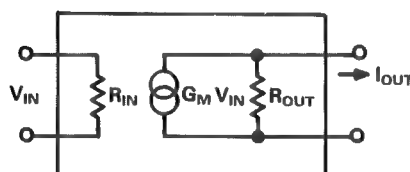
## AMPLIFIER EQUIVALENT CIRCUITS



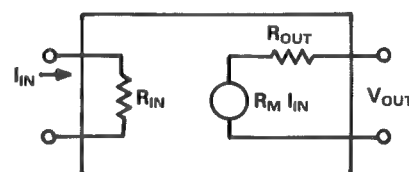
VOLTAGE AMPLIFIER



CURRENT AMPLIFIER



TRANSCONDUCTANCE AMPLIFIER

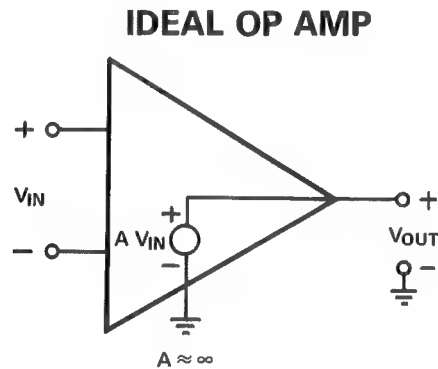


TRANSIMPEDANCE AMPLIFIER

## BASIC OPERATIONAL AMPLIFIER

The operational amplifier or "op amp", is the most commonly used analog component. Op amps are available in a wide variety of technologies, specifications, prices and package styles from a multitude of vendors. When a circuit requires an operational amplifier the designer is confronted with a bewildering number of devices from which to choose. This seminar will serve to make the selection process somewhat simpler.

The ideal op amp has differential inputs, an infinite input impedance, a single-ended output, and infinite gain at all frequencies. Many engineers also assume that the ideal op amp is a three-terminal device and disregard Kirchhoff's Law which, in essence, says that all current circuits are closed ("What goes out must come in again"). This can lead to serious circuit problems. The ideal op amp must always be considered as a four-terminal device, the fourth terminal being the return path for the output current. In most designs, it is assumed that the amplifier is, in fact, an ideal, and that no current flows into the input terminals, there is no input offset voltage and no power is required for its operation.



## THE REAL OPERATIONAL AMPLIFIER

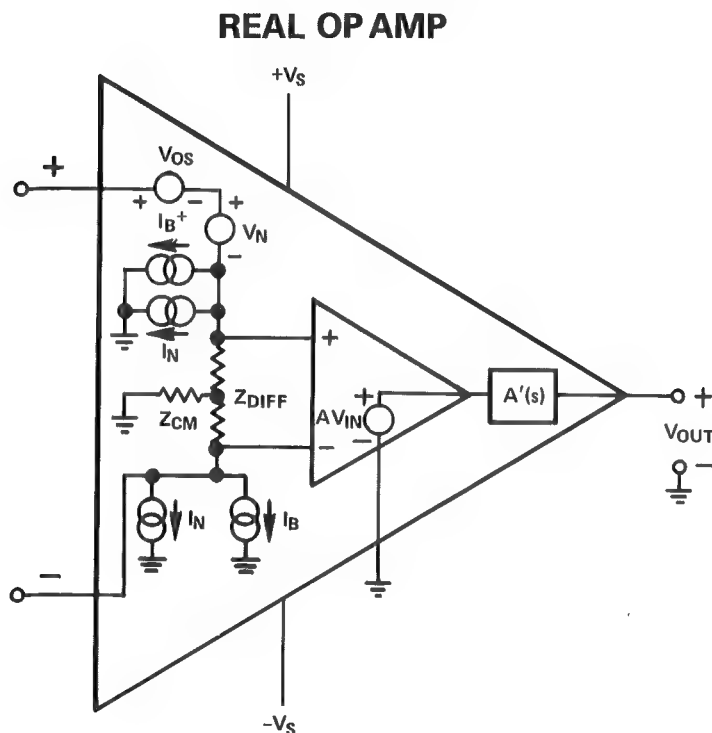
### Input Imperfections

The actual characteristics of real op amps are considerably more complicated. Each input contains a dc current source ( $I_B$ , the bias current), and is a dc voltage source ( $V_{OS}$ , the offset voltage) in series with the inputs. The amplifier has differential and common-mode input impedances ( $Z_{IN(DIFF)}$  and  $Z_{IN(CM)}$ ) respectively which are usually complex, consisting of a resistance and capacitance in parallel.

There are also three uncorrelated noise sources: two current sources (one in series with each input) and a voltage source which appears differentially. Finally the amplifier has gain w.r.t. common-mode signals, which the ideal amplifier has not, and so its common-mode rejection ratio (CMRR) must be specified.

### Output Obstacles

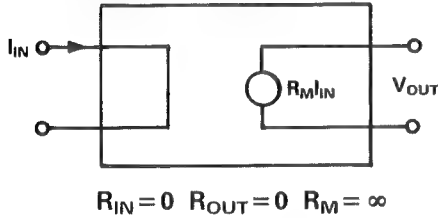
The output side of the model is also not ideal. There is an output impedance ( $R_O$ ) in series with the voltage source. The gain ( $A$ —infinite in the ideal model) is both finite and a function of frequency in a real amplifier, which also has a finite slew rate and limited output voltage and current capabilities.



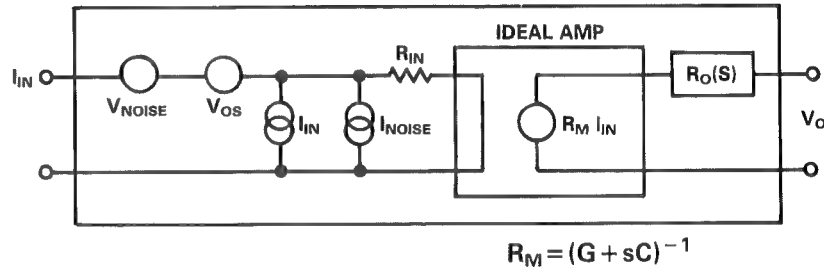
## BASIC TRANSIMPEDANCE AMPLIFIER

The transfer function of a transimpedance amplifier is a scaling factor specified in volts per ampere or simply  $R_M$ . In the ideal case  $R_M$  has zero phase shift associated with it but a real transimpedance amplifier has a frequency dependent  $R_M$ .

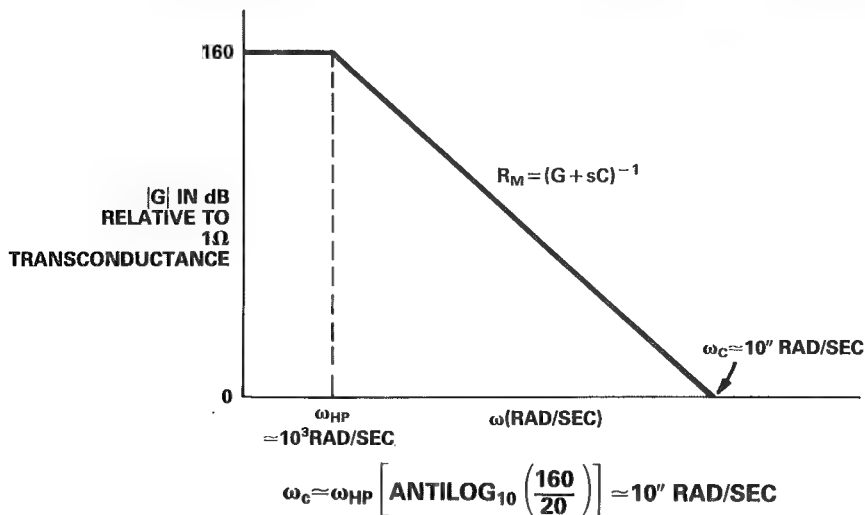
### IDEAL TRANSIMPEDANCE AMPLIFIER



### REAL TRANSIMPEDANCE AMPLIFIER



### AD846 TRANSIMPEDANCE AMPLIFIER – THEORETICAL OPEN LOOP FREQUENCY RESPONSE

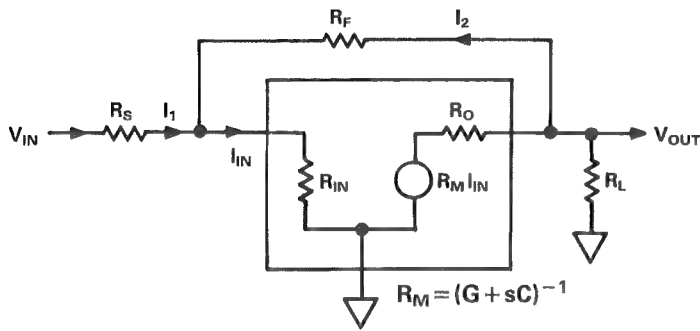


A real transimpedance amplifier and a real voltage (operational) amplifier are very similar with respect to inadequacies and deviation from the ideal model. Regardless of which type of amplifier is considered, limitations exist in fabrication techniques and manifest themselves as temperature variations of parameters, as offset voltages and currents, as nonzero bias currents, and as finite CMRR, PSRR, input and output impedances, and open loop gain.

The significant difference between the devices is that the op amp is a voltage controlled voltage source and the transimpedance amplifier is a current controlled voltage source. The computation of voltage gains, input and output impedances, in a transimpedance amplifier is very similar to those of op amps, Ohms Law and the principal of superposition are utilized.

Since the input to a transimpedance amplifier is a current and the output is a voltage the gain is expressed in ohms ( $R = V/I$ ). Since small changes in current cause large voltage changes the gain in ohms is quite large—about 100,000,000 in the case of the AD846. In the case of the gain is expressed in dB w.r.t.  $1\Omega$  or 160dB. This is by no means the same thing as a voltage gain of 160dB. In a voltage amplifier or a current amplifier it is reasonable to talk of “unity gain” since at unity gain the input and output are equal, but in a transimpedance or transconductance amplifier the input and output signals are of different types and unity gain has little or no meaning. (Volts, amperes and ohms are, in this context, quite arbitrary quantities and to consider unity gain to be equal to a transimpedance of one volt per ampere or a transconductance of one ampere per volt has no more validity than a value of unity gain defined by any other pair of values.) It follows that the 16GHz gain-bandwidth product of the AD846 is due to the choice of unit for its gain and is not a useful parameter. It is more interesting to consider the behavior of a transimpedance amplifier in the inverting mode.

## INVERTING GAIN CALCULATION FOR TRANSIMPEDANCE AMPLIFIER



$$R_{IN} \approx 67\Omega \text{ (ASSUME ZERO)} \\ R_{OUT} \approx 35\Omega \text{ (ASSUME ZERO)}$$

$$\therefore I_{IN} = I_1 + I_2 = \frac{V_{IN}}{R_S} + \frac{V_{OUT}}{R_F}$$

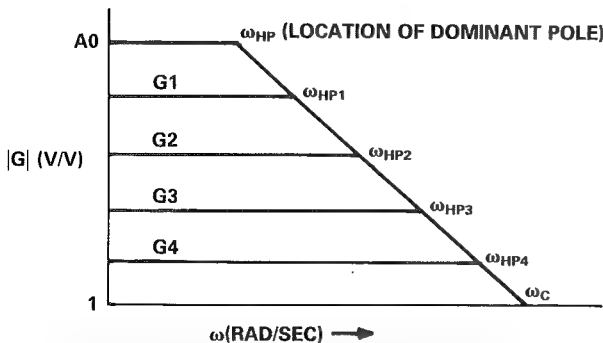
$$V_{OUT} = R_M I_{IN} \quad I_{IN} = \frac{V_{OUT}}{R_M}$$

$$\text{SUBSTITUTE: } \frac{V_{OUT}}{R_M} = \frac{V_{IN}}{R_S} + \frac{V_{OUT}}{R_F}$$

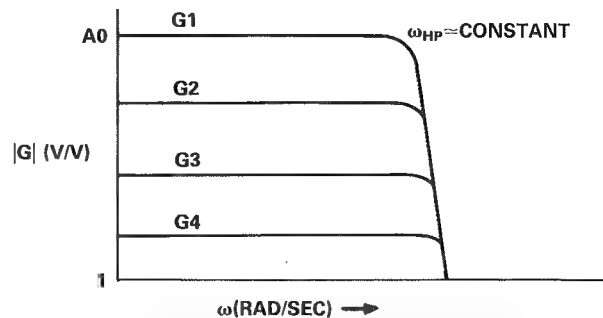
$$\text{SOLVE FOR } \frac{V_{OUT}}{V_{IN}} \quad \frac{V_{OUT}}{V_{IN}} = \frac{-\frac{R_F}{R_S}}{1 - \frac{R_F}{R_M}} = \frac{-\frac{R_F}{R_S}}{1 - R_F(G + sC)}$$

If  $R_F$  is held constant and the variation in closed loop gain is determined by altering the value of  $R_S$ , the half power point remains constant and for values of  $R_F \ll R_{IN}$ ,  $V_{OUT}/V_{IN} = -R_F/R_S$ . Practical values of closed loop gains are in the order of 100 volts per volt. Similar computations, using fundamental principles, can be made to show the effects on the input and output impedances as the loop gain is varied. The transimpedance amplifier is clearly a valuable tool for the circuit designer.

## COMPARISON OF OP AMP AND TRANSIMPEDANCE AMP CLOSED LOOP GAIN/FREQUENCY PERFORMANCE



**DOMINANT POLE OP AMP COMPENSATION WITH  
VARIOUS CLOSED LOOP RESPONSES**



**TRANSIMPEDANCE AMPLIFIER CONFIGURED AS AN  
INVERTING VOLTAGE AMPLIFIER**

## AMPLIFIER SPECIFICATIONS AND TESTING

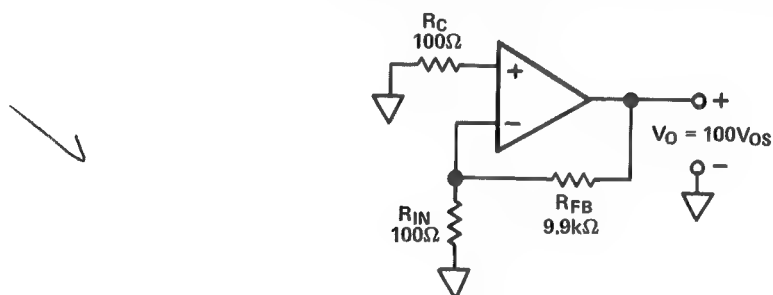
There are two other classes of amplifier, with differential inputs and a single-ended output: Instrumentation Amplifiers and Isolation Amplifiers. They are both voltage amplifiers and differ from the op amp in having gains which are lower (generally in the range 1–1,000), very stable, and accurately defined without negative feedback connections to their inputs. The isolation amplifier also has a common-mode range of many hundreds or thousands of volts. These amplifiers are described in detail in another part of this seminar but since they have a similar architecture they are tested in the same way as op amps. All the op amp test circuitry described in this section may also be used to test instrumentation and isolation amplifiers.

Although op amps and transimpedance amps have similar error terms the application of each part warrants discussing errors in separate contexts. Some specifications will be examined separately, but similarities will be pointed out when appropriate.

In general, dc errors result from lack of symmetry and inadequate matching of components. Consider the op amp. Its offset voltage ( $V_{OS}$ ) is defined as the voltage which must be applied to the input to cause the output to be zero. Offset voltage is the result of mismatch in the base-emitter voltages of the differential input transistors (gate-source voltage mismatch in FET-input amplifiers) and is indistinguishable from a dc input signal. This offset can be trimmed to zero with a potentiometer, which adjusts the balance of the operating currents in the input stage until  $V_{BE1}$  and  $V_{BE2}$  (or  $V_{GS1}$  and  $V_{GS2}$ ) are equal. Even if the offset voltage is trimmed to zero at one particular temperature it is a temperature variable phenomenon. When a bipolar transistor op amp is trimmed for minimum offset it is thereby trimmed for minimum temperature drift but this is not the case for FET-input op amps. The physics of this difference is described in a later section of the seminar.

Many circuits exist for measuring offset voltage. The simplest and most commonly illustrated in textbooks uses only three resistors in addition to the op amp under test. The gain of the amplifier is set by the two resistors  $R_{IN}$  and  $R_{FB}$  and the noninverting input is grounded via a bias compensation resistor (unnecessary if the op amp is a low bias current type). The offset voltage is then amplified by the closed-loop gain of the system. The output voltage is therefore a multiple of the offset voltage and it may be measured and the offset voltage calculated. Of course the closed-loop gain must be less than 1% of the open loop gain if the measurement is to be very accurate, and the circuit is THEORETICALLY unsatisfactory, although in practice perfectly adequate, because the offset voltage is defined as that voltage producing zero output and this circuit actually produces a nonzero output.

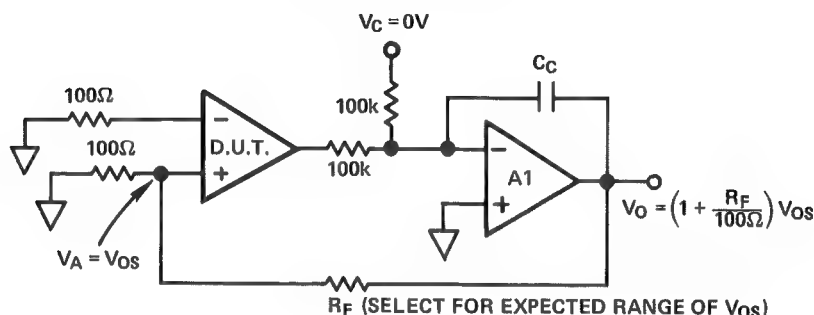
### SIMPLE $V_{OS}$ TEST CIRCUIT



A circuit which is not only theoretically satisfactory but may also be used to measure a number of other op amp parameters is illustrated in the next diagram. It consists of a servo loop built around the device under test (DUT) to determine its output voltage. A second amplifier (with a large feedback capacitor to ensure that it has negligible HF response) is used to provide feedback to force the output of the DUT to be equal in magnitude and opposite in sign to the voltage ( $V_C$ ) applied to the control input. This feedback amplifier must have high gain, low offset voltage and low bias current but does NOT need to have very good performance, and certainly does not need to have specifications which are better than those of the DUT.

When measuring offset voltage the control voltage,  $V_C$ , is set to zero. This forces the output of the DUT to zero as well. Since the output of the DUT will go to zero only when a voltage equal to its input offset voltage is applied to its input,  $V_A$  must equal  $V_{OS}$ . Thus the output of the feedback amplifier is equal to  $V_{OS} (1 + R_F/100)$  and the offset voltage may be calculated from the feedback amplifier output voltage.

### OP AMP OFFSET VOLTAGE TEST CIRCUIT

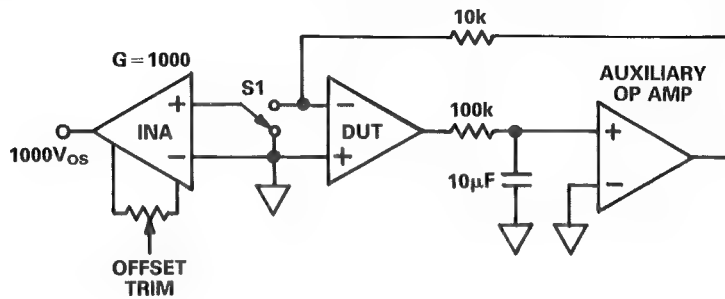


#### Transimpedance Amp Offset Voltage

The transimpedance amp, like the op amp, has a dc error term known as offset voltage which was shown in the transimpedance amplifier model as a voltage source in series with the inverting input terminal. This offset voltage is indistinguishable from an external voltage and introduces errors since it causes additional current to flow in the input of the transimpedance amplifier resulting in an error in the output voltage.

Since the transimpedance amplifier has a very low input impedance it is not possible to use exactly the same measurement system as is used for op amps but a similar arrangement will work. The transimpedance amplifier under test is connected to an auxiliary amplifier as before but feedback is taken to the inverting input of the DUT and therefore the auxiliary amplifier must be used in the noninverting mode. Since the input impedance of the DUT is very low a measurement at the output of the auxiliary amplifier does not tell us anything about the offset voltage at the DUT. That is measured with an instrumentation amplifier set to a gain of 1000. Any offset voltage in the instrumentation amplifier will affect the accuracy of the measurement. The in-amp offset must be set to zero by either automatic or normal procedures.

## TRANSIMPEDANCE AMPLIFIER $V_{OS}$ TEST CIRCUIT



### Op Amp Input Bias Current

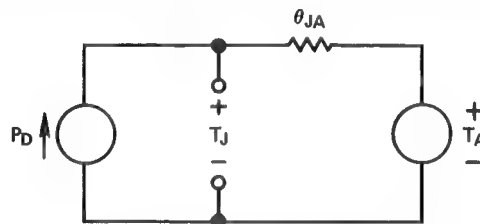
Another dc parameter of op amps is input bias current ( $I_B$ ). If an op amp uses bipolar transistors in its input stage base current must be supplied from somewhere to bias them into their active operating region. Since Kirchoff's Law tells us that current must flow in circles this current must also return to its origin through a dc path. Thus operational amplifiers cannot be used with input signal sources which are not referred to the same power source as the amplifier itself. Although FETs do not require base current they nevertheless have a leakage current from their gate junction diode which results in an input bias current.

In many applications, the errors due to bias currents are actually less than the errors caused by the mismatch of the bias currents on the two inputs. This difference between the bias currents is called the input offset current, and is usually specified along with the bias current.

Like the input offset voltage, bias currents also vary with temperature. In an amplifier with a bipolar input stage the bias current decreases with increasing temperature because the transistors'  $\beta$  increases, and since their emitter current remains constant, the base current decreases. In the case of FET input amplifiers where the bias current is the gate leakage current of an FET (which is the leakage current of a reverse-biased junction diode). Such leakage currents double for every  $10^\circ\text{C}$  rise in junction temperature.

It is important to consider the test conditions under which bias current is specified, particularly in the case of a FET input op amp. Some manufacturers specify bias current at a junction temperature of  $25^\circ\text{C}$ . This corresponds roughly to the bias current immediately after power is applied to the amplifier. Unfortunately most circuits are not operated in a pulsed mode, and the effects of amplifier self-heating must be considered. This effect can be far from trivial. For example, an amplifier which draws 5 milliamps of supply current from  $\pm 15$  volt supplies dissipates 150 milliwatts. The thermal resistance from junction to ambient for 8-lead IC packages is typically  $150^\circ\text{C}/\text{W}$  which means that after warm-up in an ambient of  $25^\circ\text{C}$  the junction temperature of the amplifier in question will be  $22.5^\circ\text{C}$  higher or  $47.5^\circ\text{C}$ . If the bias current was specified as (say)  $50\text{pA}$  at  $25^\circ\text{C}$  junction temperature it will be over  $200\text{pA}$  after warm-up. For this reason Analog Devices makes a practice of specifying the bias current of FET input op amps for a given AMBIENT temperature rather than a particular junction temperature. During production testing the device temperature is allowed to stabilize for about 10 seconds after the application of power before the bias current is measured.

## THERMAL CIRCUIT MODEL FOR IC OP AMP



$$\begin{aligned}\theta_{JA} &= 150^\circ\text{C}/\text{W} \text{ FOR TO-99 TYPE PACKAGES} \\ &= 155^\circ\text{C}/\text{W} \text{ FOR EPOXY MINI-DIP} \\ &= 100^\circ\text{C}/\text{W} \text{ FOR 14/16 PIN CERAMIC DIP}\end{aligned}$$

### CONSIDER AN OP AMP SPECIFIED FOR $50\text{pA}$ $I_B$ AT $T_J = 25^\circ\text{C}$

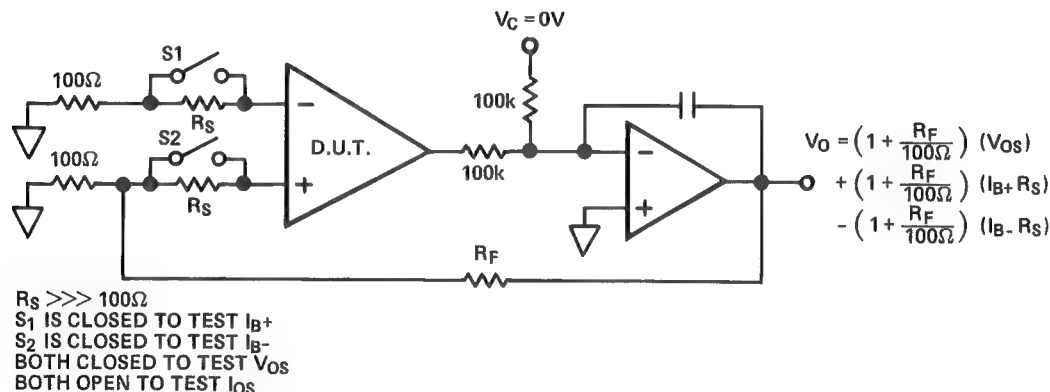
If the Amplifier Draws  $5\text{mA}$  from  $\pm 15\text{V}$ ,

$$\begin{aligned}P_D &= 30 \times 5 = 150\text{mW} \\ T_J &= T_A + (150\text{mW} \times 150^\circ\text{C}/\text{W}) \\ &= 25^\circ\text{C} + 22.5^\circ\text{C}\end{aligned}$$

Therefore,  $I_B$  will be Four Times Higher than Spec.

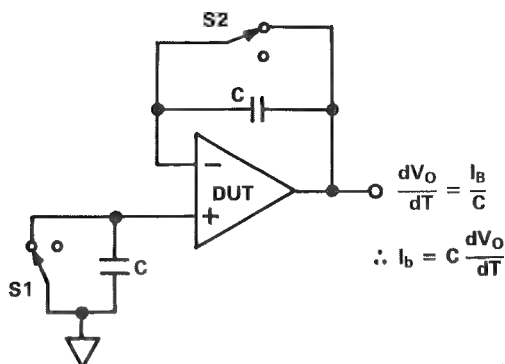
Bias current may be measured by essentially the same method as is used to measure offset voltage. A large resistance is inserted in series with the input under test, creating an apparent additional offset voltage equal to  $I_B \cdot R_S$ . If the actual  $V_{OS}$  has been measured and recorded the change in apparent  $V_{OS}$  due to the change in  $R_S$  can be determined and  $I_B$  is easily computed. The offset current is obtained by taking the difference between the bias current on the inverting input and the bias current on the noninverting input. Typical  $R_S$  values vary from  $100k\Omega$  for bipolar amplifiers to  $10^{12}\Omega$  for some FET input types.

### BIAS/OFFSET CURRENT TEST CIRCUIT



Very low bias currents may also be measured by integration techniques. The current is used to charge a capacitor and the rate of charge is measured. If the capacitor and general circuit leakage is negligible (and this is very difficult to ensure when currents of under  $10fA$  are to be measured) the current may be calculated directly from the rate of change of output of the test circuit when the switch which short-circuits the capacitor is opened.

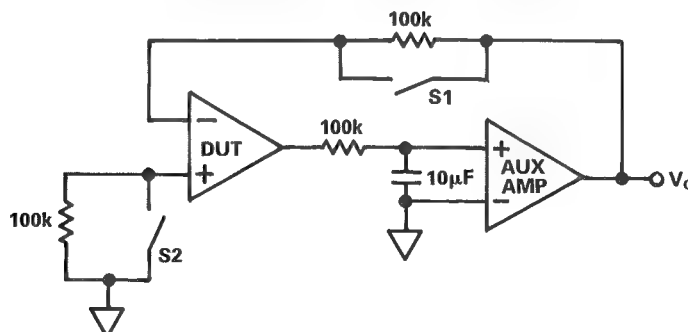
### MEASUREMENT OF VERY LOW BIAS CURRENT



#### Transimpedance Amp Input Current

Unlike the op amp, the transimpedance amplifier does not have an input bias or offset current. Instead an input current is specified. This input current is a measure of how well the input stages and associated circuitry are matched and balanced. This input current is not really a bias current, since an ideal transimpedance amplifier, unlike an op amp, does not require an external current to function correctly.

### TRANSIMPEDANCE AMPLIFIER INPUT CURRENT TEST CIRCUIT



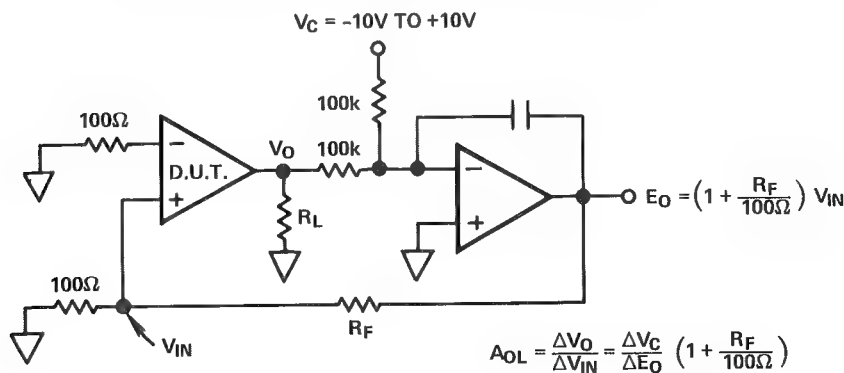
Nevertheless the circuitry used to measure this non-bias current is very similar to the circuitry used to measure op amp bias currents except that, as in the offset measurement circuitry, the feedback is taken to the inverting input of the transimpedance amplifier and the auxiliary amplifier is used in the noninverting mode. The input currents are allowed to flow into resistors ( $R_3$ ) which are short-circuited by switches. By measuring the output of the auxiliary amplifier with the switches open and closed the voltage drop in the resistors may be measured and the input currents calculated.

### Op Amp Open Loop Voltage Gain

Another op amp parameter which distinguishes a real amplifier from an ideal amplifier is open-loop gain. The open loop gain of an ideal op amp is assumed to be infinite. The same assumption is occasionally made of real amplifiers, with unfortunate results, as will be demonstrated later in this chapter. (Instrumentation and isolation amplifiers, on the other hand, have gains which are usually between 1 and 1000 and are very accurately defined.)

The open loop gain of an operational amplifier is an interesting parameter to measure. It is not generally practical to measure open loop gain directly by applying a signal at the input and observing the output change. Op amps generally have around 20 volts of output swing and gains of over one million—the input would therefore need to be of the order of one microvolt and it is very hard to handle such signals without unacceptable errors due to thermoelectric potentials). However, by using the same feedback system that we used to measure  $V_{OS}$  and  $I_B$  it is possible to measure the change in input voltage required to produce a known change in output voltage.

### OPEN LOOP GAIN TEST CIRCUIT

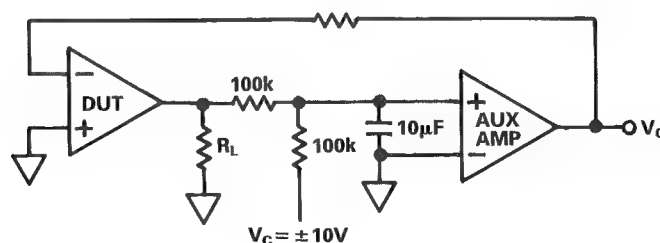


In this circuit, the control voltage,  $V_C$  is varied from  $-10V$  to  $+10V$ , causing the DUT output,  $V_O$ , to vary from  $+10V$  to  $-10V$ . The DUT output is varied by the change in  $V_{IN}$  produced by negative feedback through the second amplifier.  $V_{IN}$  is attenuated from  $E_O$  by the  $R_F/100$  voltage divider.  $E_O$  is easily measured, and hence the open loop gain can readily be computed. This circuit works perfectly well for instrumentation and isolation amplifiers but it is not necessary to use it with them since their lower gain does allow the use of the simpler technique of measuring the input and output voltages.

### Open Loop Transimpedance

The open loop transimpedance of an ideal transimpedance amplifier is infinite. Where such an amplifier has a finite transimpedance this is specified in ohms (volts per ampere). Practical monolithic transimpedance amplifiers have dc transimpedance of the order of 300 million volts per ampere (300 megohms). The sheer magnitude of this transimpedance imposes restrictions on the techniques used to measure it. In principle all that is required is to inject a known current into the input, measure the resulting output voltage and compute the transimpedance. In practice the smallness of the current which must be injected, combined with the value of the input current, makes such a method less than ideal and an electronic servo approach yields more satisfactory results.

### OPEN LOOP TRANSIMPEDANCE TEST CIRCUIT





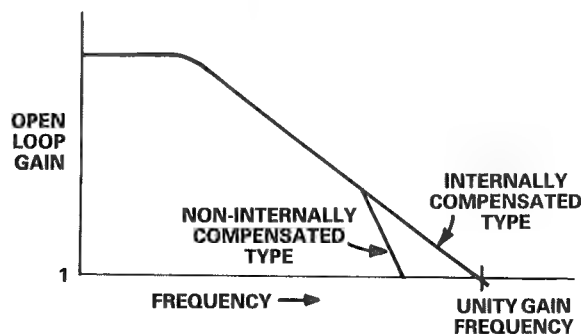
Again the circuitry is similar to the op-amp circuitry but uses the inverting input of the DUT and the auxiliary amplifier in a noninverting mode. Otherwise the procedure is the same as is used for op amps.

As with most amplifier parameters the transimpedance varies with temperature. Under normal operation of the transimpedance amplifier open loop gain variation does not significantly affect circuit performance, because the required system gains are controlled by precision resistors used as feedback elements.

### Frequency Response

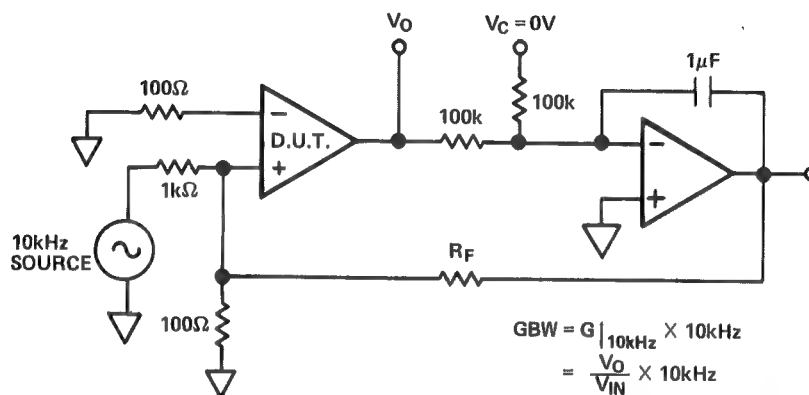
Most operational amplifiers have a very simple frequency response. The gain is constant at dc and very low frequencies and then has a single-pole rolloff, falling at 6dB/octave ( $-20\text{dB/decade}$ ). It is obvious that throughout the region where this single pole frequency response applies the product of gain and frequency is a constant—this constant is known as the “gain-bandwidth product” of the amplifier and is a measure of its high frequency performance. In the majority of op amps this single pole response continues past the point where the gain has dropped to unity (such amplifiers are known as “internally compensated” or “unity gain stable” amplifiers). Some amplifiers have a more complex response and at a gain of something less than 10 a second pole appears. These amplifiers are not stable at low closed loop gains but generally have better high frequency performance than internally compensated types.

### OPERATIONAL AMPLIFIER GAIN/ FREQUENCY PLOT



Since all op amps have a single pole frequency response at gains of more than 10 it is not usual to measure gain at a number of frequencies. It is evident that if the gain is measured at dc and one frequency the response of the amplifier throughout the region where it has a single pole response may be reduced from the gain-bandwidth product.

### GAIN-BANDWIDTH PRODUCT TEST CIRCUIT



In the circuit shown the dc output of the DUT is held at 0 volts by  $V_C$  and the integrator amplifier, and a low amplitude ac signal is applied to the input of the DUT. The frequency of this ac signal is chosen so that the open loop gain is somewhere between 20 and 1000, since lower gain might result in complications from any second pole in the DUT's response and higher gain would necessitate too small an input signal. For most op amps 10kHz is a very suitable frequency. Since the integrator has very low gain at 10kHz there is no ac feedback and the DUT is effectively running open-loop for the ac signal. The ac output from the DUT can be measured and the gain at 10kHz can be calculated. [For example, an AD741 amplifier has an open loop gain of approximately 100 at 10kHz and an easily generated 100mV input will produce an easily measured 10V output. This corresponds to a 1MHz gain-bandwidth product.]

### Slew Rate

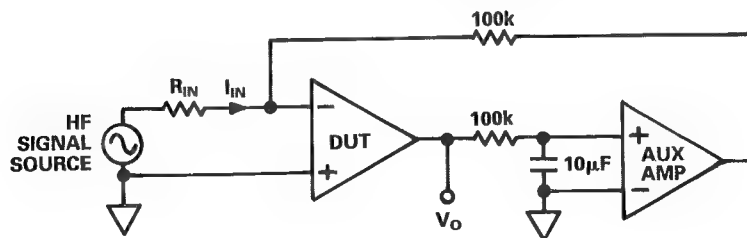
The same test circuit may be used to measure the slew rate of the DUT. The slew rate of an amplifier is defined as the rate at which the output voltage can change when high drive is applied to the input. When the circuit is used to measure slew rate the input signal is a fast square wave of sufficient amplitude to drive the output of the DUT to saturation. As oscilloscope is used to observe the slew rate of the DUT output.

### Open Loop Transimpedance Amplifier Frequency Response

Like the operational amplifier, the transimpedance amplifier generally has a single pole frequency response and the product of its gain and frequency is a constant "gain bandwidth product". The gain need be measured at dc and only one frequency in order to calculate the overall response. The transimpedance amplifier does not have infinite bandwidth but, as will be shown later, it can be configured as a voltage amplifier whose bandwidth is not dependent on closed loop gain as is the case with the dominant pole compensated operational amplifier.

Once again the test circuitry is similar to that used for the op amp except that, again, the feedback is taken to the inverting input of the transimpedance amplifier and the auxiliary amplifier is used in the noninverting mode. The RC filter between the DUT and the auxiliary amplifier prevents any feedback at the test frequency. The signal (which is a current, not a voltage) is applied to the inverting input of the DUT. The amplified signal is measured at the DUT output and the transimpedance calculated.

## TRANSMIMPEDANCE AMPLIFIER H.F. OPEN LOOP GAIN MEASUREMENT

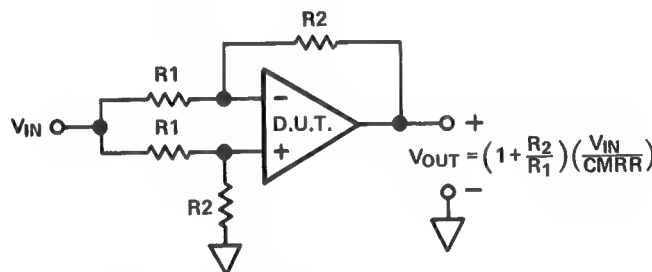


### Common-Mode Rejection Ratio (CMRR)

The ideal operational amplifier has only differential gain and is insensitive to the absolute voltage on the inputs. A real amplifier has several nonideal characteristics associated with input levels. First of all the range of input voltage is limited. Few IC op amps will operate when the voltages on the input terminals are outside the supply voltages. The second, and perhaps more subtle, characteristic is the common-mode rejection ratio (CMRR). The CMRR is defined as the ratio of a change in common-mode voltage to the change in differential input voltage which would produce the same change in output. It is often convenient to specify this parameter in dB.

The common-mode rejection ratio can be measured in several ways. One method uses four precision resistors to configure the op amp as a subtractor amplifier, a signal is applied to both inputs and the change in output is measured—an amplifier with infinite CMRR would have not change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp in determining the CMRR of the whole system. A mismatch of 0.1% between resistor pairs will result a CMRR of only 60dB, no matter how good the op amp. Since most op amps have CMRRs of between 80 and 120dB it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring its own resistance match!).

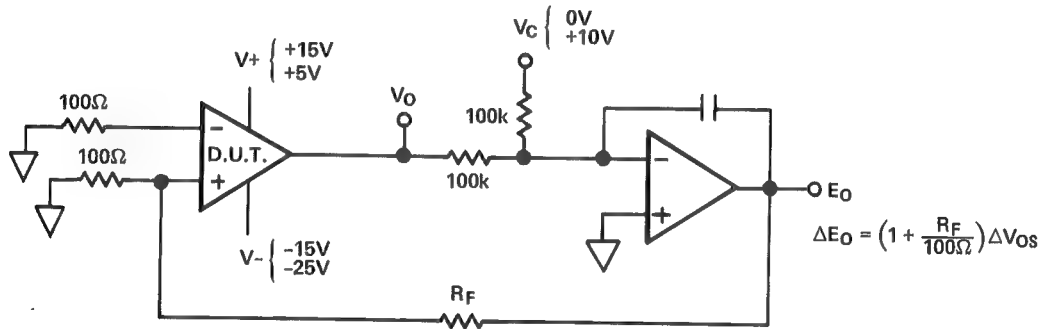
## SIMPLE CMR TEST CIRCUIT



RESISTORS MUST MATCH WITHIN 1ppm (0.0001%)  
IN ORDER TO MEASURE CMR > 100dB

The circuit used for the measurement of offset, bias and gain will, with slight modification, measure CMRR without requiring accurately matched resistors. The circuit is used to measure the offset voltage of the DUT when it is operating with  $\pm 15\text{V}$  supplies (referred to the overall system). Its output, is centered between those supplies by setting  $V_C$  to  $0\text{V}$ . The measurement is repeated with the DUT operating with  $+5\text{V}$  and  $-25\text{V}$  supplies and its output still centered between them (at  $-10\text{V}$ ) by setting  $V_C$  to  $+10\text{V}$ . This change is equivalent to applying  $+10\text{V}$  common-mode signal at the input. The CMRR is the ratio of the  $10\text{V}$  common-mode signal to the change in offset voltage.

## COMMON-MODE REJECTION TEST CIRCUIT



For example if this  $10\text{V}$  change in common-mode voltage creates a  $1\text{mV}$  change in  $V_{OS}$ , the CMRR is  $10\text{V}/1\text{mV}$  ( $= 10000$  or  $80\text{dB}$ )

### Transimpedance Amplifier Common-Mode Rejection

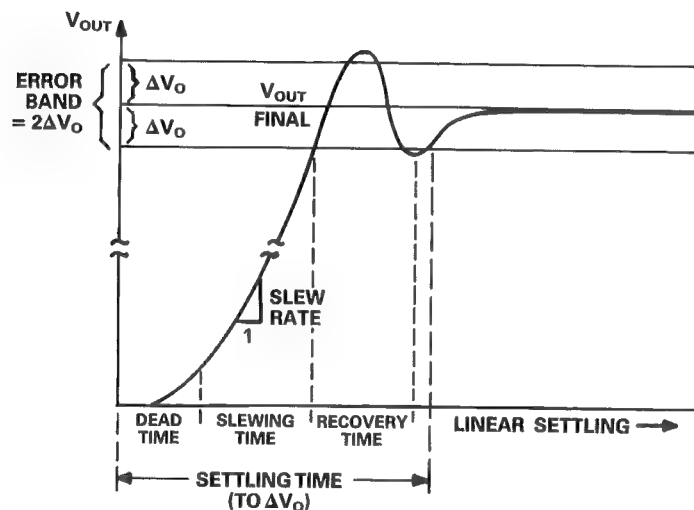
The transimpedance amplifier is designed to be used in the inverting mode and as such the CMRR term associated with op amps is not applicable. The noninverting terminal is grounded and should not be considered as a signal input.

### Settling Time

Settling time is an important op amp specification especially when the amplifier must handle rapidly changing signals. In applications such as multiplexers, sample/hold amplifiers (SHAs) and amplifiers used with A/D and D/A converters it is the amplifier settling time which often determines the maximum data rate for a specified accuracy.

Settling time is defined as the time which elapses between the application of a step input to the time at which the amplifier output enters, and remains within, a specified error band symmetrical about the final output value.

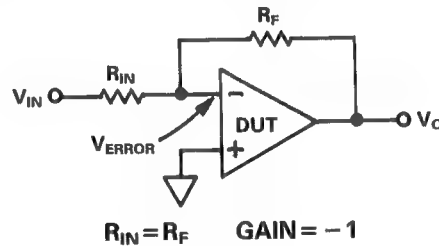
## AMPLIFIER SETTLING TIME



Settling time is determined by both the linear and the nonlinear characteristics of the amplifier. It varies with the input signal level and is greatly affected by impedances external to the amplifier. For these reasons extrapolation of settling times from one set of operating conditions to another becomes virtually impossible. Settling time cannot be predicted from open loop specifications, such as slew rate or small signal bandwidth, as it is a closed loop parameter. The best way to know how fast an amplifier will settle in a particular application is to measure it.

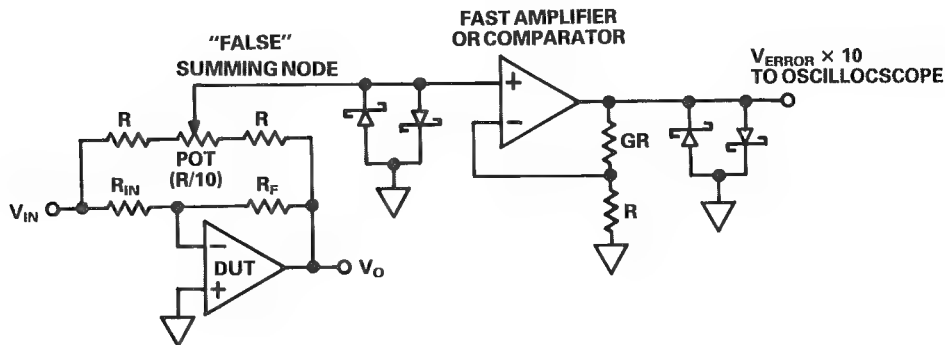
In many test configurations the amplifier is measured in the unity gain inverting mode. An error voltage is present at the inverting input which is generated by the input voltage being subtracted from the output voltage by means of two resistors.

### SIMPLE SETTLING TIME TEST CIRCUIT



A transition in the input test voltage will cause large spikes in the error voltage. However a measurement cannot be made directly at this summing junction without influencing the result of the measurement but a second "false" summing junction may be formed by the use of two more resistors.

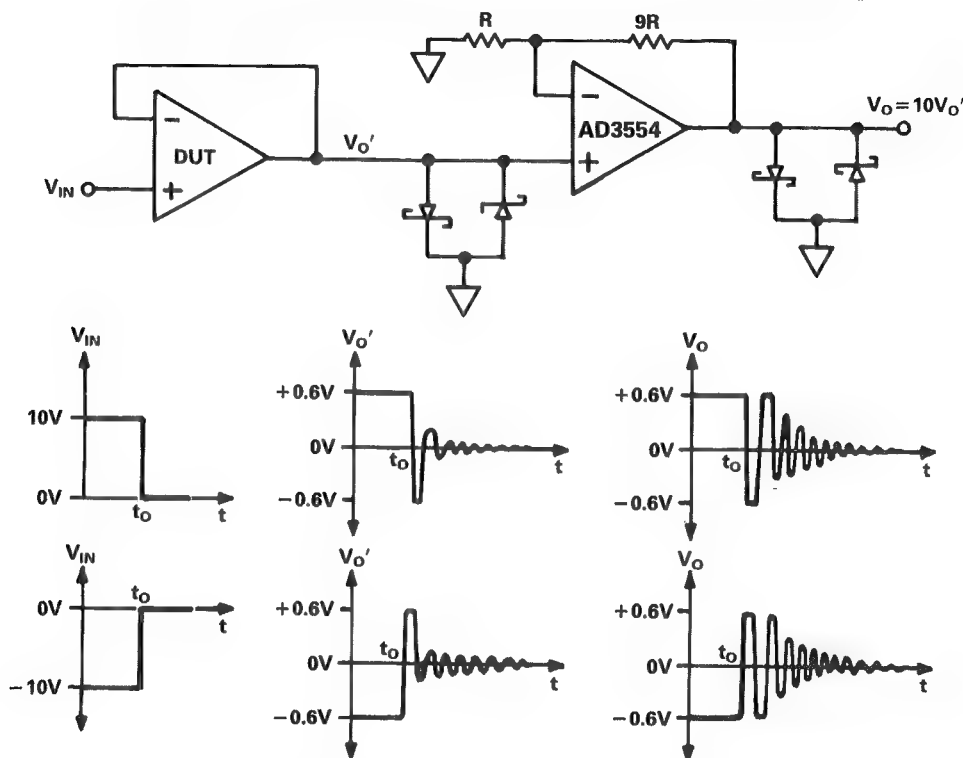
### PRACTICAL SETTLING TIME TEST CIRCUIT WITH "FALSE" SUMMING POINT



These resistors form a Wheatstone bridge with resistors  $R_{IN}$  and  $R_F$  which may be balanced with a potentiometer. The voltage at the artificial junction follows the voltage at the summing node. A comparator is used to observe this error voltage. It usually has gain, and it may also settle more slowly than the amplifier under test, since comparator settling time introduces only second-order errors into the measurement. Clamping minimizes overdrive of both the comparator and the monitoring oscilloscope.

Measuring the settling time of amplifiers in the noninverting mode must be approached differently. As there is no error junction it is unreasonable to attempt to form a false one. The most common noninverting configuration to be tested is the unity gain follower which requires direct comparison of the input step and the output signal as they swing through the entire common-mode range. In this case the comparator measures the difference directly rather than observing an error point. It is subjected to wider voltage swings and must settle at least 2 or 3 times faster than the DUT.

## ALTERNATIVE SETTTLING TIME TEST CIRCUIT



An alternative approach is to limit the input of the amplifier to a ten volt transition with a final value of zero volts. This allows direct analysis of the amplifier's output without overdriving the scope.

### NOISE

In addition to noise present on the input signal there are two types of noise in circuits using op amps: external interference and the inherent noise of the circuit itself. Interference is noise which originates from sources not related to the actual circuit. Such noise sources include ground and power-supply noise created by other circuitry in a system, stray electromagnetic pickup of line frequency energy (and the harmonics thereof) and radio and radar transmissions, contact arcing in mechanical switches and relays, and transients due to switching in reactive circuits. Even mechanical vibration can create noise in high impedance amplifier circuits, either by piezo-electric pickup due to the use of piezo-electric plastic materials in cables or circuit boards, or by capacitance variation as the circuit vibrates. External interference can often be eliminated once the interfering source is identified and appropriate action taken.

The second type of noise is the inherent noise of the circuit itself. Unlike interference, it cannot be totally eliminated since it is caused by components in the actual circuit such as resistors and sources within the amplifier. The best that can be accomplished is to minimize the noise in a specific bandwidth of interest. To do this effectively it is important to construct reasonably accurate models of the noise sources. In op amps there are a current noise source in each input and a voltage noise source which appears differentially. These three noise sources are uncorrelated (although the two current noise sources have similar rms amplitudes), which is to say that there is no connection between them and their instantaneous outputs are not related to each other in any way. When two or more uncorrelated noise sources are to be added together it is done by taking the square root of the sum of their squares. It follows that, for a small number of noise sources, if the effect of any noise source is more than three or four times larger than that of any other only the largest need be considered when analyzing the noise of the system.

#### Voltage and Current Noise Model

A considerable amount of research at Analog Devices and elsewhere over more than fifteen years has demonstrated that the noise sources in op amps really are uncorrelated and are either true Gaussian or white noise sources or differ from true white noise sources by such a small amount that the difference is insignificant for all practical purposes. There are also sources with a "pink" noise spectrum i.e., the noise power density is inversely proportional to the square root of the frequency. The same research has demonstrated that they are true pink noise sources within the present limits of experimental accuracy. We can therefore consider the noise sources in op amps in terms of their statistical properties: rms value, peak value, and frequency content. Measurement of the rms

value of a random noise waveform requires an averaging interval which is long compared to the period of the lowest frequency of interest. The rms noise value is a useful and meaningful way to characterize the amount of noise generated by an amplifier.

$$E_n^2 = \int_0^T e_n^2(t) dt$$

Where  $E_n$  (rms) is the rms Noise Voltage Value  
 $T$  is the Interval of Observation  
 $e_n$  is the Instantaneous Noise Voltage

Low frequency noise is difficult to measure, since very long observation intervals are needed. In some cases low frequency noise is measured by direct observation on a storage oscilloscope screen using very slow sweep periods.

It is common to specify the peak-to-peak noise of an op amp. Although this makes system noise analysis much simpler (the argument goes: if the noise never exceeds  $X$  value the system perturbation never exceeds  $KX$  and all will be well) it is dangerous unless the statistical nature of noise is clearly understood. For Gaussian noise and a given rms noise value statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases—BUT THIS PROBABILITY NEVER BECOMES ZERO. Thus for a given rms noise it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded but it is NOT possible to give a peak-to-peak value which will never be exceeded.

## RMS TO PEAK-TO-PEAK RATIOS

Nominal Peak-to-Peak	% of Time Noise will Exceed Nominal Peak-to-Peak Value
$2 \times \text{rms}$	32%
$3 \times \text{rms}$	13%
$4 \times \text{rms}$	4.6%
$5 \times \text{rms}$	1.2%
$6 \times \text{rms}$	0.27%
$6.6 \times \text{rms}$	0.10%
$7 \times \text{rms}$	0.046%
$8 \times \text{rms}$	0.006%

Peak-to-peak noise specifications, therefore, must always be written with a time limit. A suitable one is 6.6 times the rms value which is exceeded only 0.1% of the time. Since a manufacturer presented with such a specification will always assume Gaussian noise and measure the rms value, the op amp user is well advised to master the relationship between rms and peak values and then specify rms.

### Types of Noise

Four types of noise are commonly encountered in operational amplifiers: popcorn noise, flicker noise, shot noise and Johnson noise.

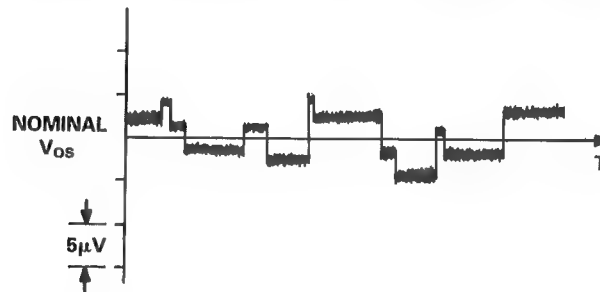
## TYPES OF NOISE ON OP AMPS

- Popcorn Noise
- Flicker (1/f) Noise
- Schottky (Shot) Noise
- Johnson Noise

### Popcorn Noise

When monolithic op amps were first introduced in the late 1960s popcorn noise was the dominant noise source. Whole advertising campaigns were fought to persuade users that Company X had lower popcorn noise than Company A, Company B and Company C. However, all of them A, B, C and X, were pretty bad. Today the causes of popcorn noise are quite well understood and production tests for it are reliable so that no reputable amplifier manufacturer has any difficulty in shipping products that are substantially free from popcorn noise. (Occasionally a digital circuit manufacturer will attempt to manufacture op amps on a TTL diffusion schedule in order to mop up spare plant capacity. These op amps will invariably suffer badly from popcorn noise since the very process steps which improve TTL speed and yield also promote popcorn noise.)

### "POPCORN NOISE" CONSISTS OF RANDOM STEP CHANGES IN $V_{OS}$ IN THE 10ms + TIMEFRAME



Popcorn noise is so-called because when played through an audio system it sounds like cooking popcorn. It consists of random step changes of offset voltage which take place at random intervals in the 10+ ms timeframe. Such noise results from high levels of contamination and crystal lattice dislocation at the surface of the silicon chip, which in turn results from inappropriate processing techniques or poor quality raw materials. It is quite easy to screen for popcorn noise during the manufacture of op amps so even if, for reasons beyond a manufacturer's control, devices should be produced with high levels of popcorn noise they should be detected and rejected at an early stage.

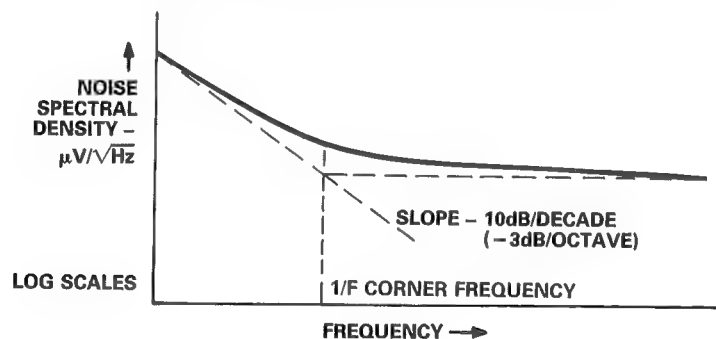
### "Flicker" or "1/f" Noise

Flicker noise is the dominant noise at low frequencies. It has a power spectral density which is inversely proportional to frequency (hence the term "1/f Noise"). The noise voltage spectral density is therefore inversely proportional to the square root of the frequency.

The noise spectral density drops at 10dB/decade ( $-3\text{dB/octave}$ ) with rising frequency. Noise with such a spectrum is called "pink" noise.

In early op amps (once popcorn noise had been conquered) flicker noise was the dominant noise source below frequencies as high as 1kHz. Today it is rarely significant above 50Hz and in devices such as the AD OP-27 it is insignificant above one or two Hz. The frequency at which the flicker noise characteristic of an amplifier intersects the white noise floor is known as the "1/f corner frequency" and is a figure of merit for the amplifier—the lower the better.

### "FLICKER" OR "1/F" NOISE



### Johnson Noise

Thermal excitation of the electrons in conductors causes random movement of charge. In a resistance this random current causes a noise voltage, known as Johnson Noise, whose amplitude is given by the formula:

## JOHNSON NOISE VOLTAGE

$$E_N \text{ (rms)} = \sqrt{4kTRB}$$

Where:  $k$  = Boltzmann's Constant ( $1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$ )

$T$  = Temperature  $^\circ\text{K}$

$R$  = Resistance in Ohms

$B$  = Bandwidth in Hertz

At Room Temperature ( $25^\circ\text{C}$ ) This May Be Simplified To

$$E_N \text{ (rms)} \approx \frac{1}{8} \sqrt{RB} \quad \text{or} \quad e_n \approx 4\sqrt{R}$$

$E_N$  = Total Noise in  $\mu\text{V rms}$        $e_n$  = Spectral Density in  $\text{nV}/\sqrt{\text{Hz}}$

$R$  = Resistance in Kilohms       $R$  = Resistance in Kilohms

$B$  = Bandwidth in Kilohertz

Johnson noise is a fundamental property of resistances and must always be considered when designing low noise circuitry. There are only three ways in which it may be reduced: by reducing the temperature, the resistance itself or the working bandwidth.

Reducing the temperature is generally impractical. Since the function is a square root cooling a resistor from room temperature ( $25^\circ\text{C}/298\text{K}$ ) to liquid nitrogen temperature ( $-196^\circ\text{C}/77\text{K}$ ) will only reduce the noise by 42%. Reducing the resistance itself or the working bandwidth are generally more useful. As a reference point it is useful to remember that at room temperature a  $1\text{K}$  resistor has  $4\text{nV}/\sqrt{\text{Hz}}$  white noise. This is equivalent to  $128\text{nV rms}$  noise in a  $1\text{kHz}$  bandwidth.

Although Johnson noise is one of the causes of internal noise in an amplifier it is generally less important inside the amplifier than it is in the external resistors of the circuit. In many cases the noise from the external resistors is much higher than amplifier generated noise.

### “Shot” (or Schottky) Noise

Current in a conductor consists of a flow of electrons each of which has a discrete charge. Current in a semiconductor consists of a flow of electrons or “holes” depending on whether it is an N-type or P-type semiconductor but the quantized nature of the flow is the same in either case. There are statistical variations in the rate of electron flow and these manifest themselves as a noise current.

## SHOT NOISE

$$I_N = 5.7 \times 10^{-4} \sqrt{I_J B}$$

Where  $I_N$  is Noise Current in Picoamps rms

$I_J$  is Junction Current in Picoamps

$B$  is Bandwidth of Interest (in Hertz)

Since the electronic charge is extremely small the noise current is very small as well and is only significant when the bandwidth is very large or when the noise current is an appreciable fraction of the total current since noise current is proportional to the square root of the current the second case occurs only at very low currents. Thus shot noise is important at high frequencies and in amplifiers with very low bias currents but rarely elsewhere.

### Noise Specifications

The data sheet of a high performance operational amplifier should contain some noise specifications. Noise testing is slow and time consuming and therefore expensive, so it is more normal for manufacturers to quote typical specifications rather than absolute maxima. Specifications may be quoted however, which are “guaranteed but not tested”. Amplifiers intended for low noise applications may be tested, and priced accordingly, and many manufacturers are prepared to test amplifiers for noise as a special at additional cost.

Noise specifications may be presented in a wide variety of ways. In order to understand and compare the noise specifications of devices from different manufacturers, or even those of different devices from the same manufacturer, it is necessary to understand the principles behind noise specifications so that the data available may be manipulated to its most useful form.

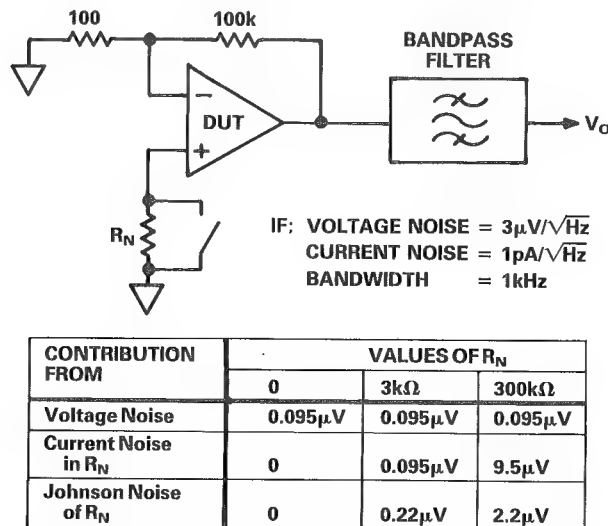


Early op amp specifications often referred to a “noise figure” expressed in dB when the op amp was used with a stated source impedance. This noise figure is the ratio of the actual noise in the circuit to the theoretical minimum noise of a perfect amplifier used in the same circuit. Although noise figure is still widely specified for RF amplifiers and discrete devices it is no longer commonly used for op amps.

Since there are three noise sources in an op amp (as mentioned above, the two current noise sources are of similar magnitude—though uncorrelated) an ideal data sheet would specify the magnitude and spectral composition of each. This is almost never done, simply because the amount of work involved in characterization, and in monitoring production devices, would be prohibitively expensive.

Although the voltage noise is always present and unavoidable, the current noise of an op amp is only amplified if it flows in a resistor and develops a noise voltage. Thus the voltage noise is dominant when an amplifier is driven from a low source resistance and the current noise is dominant when it is driven from a high source resistance. Depending on the actual values of voltage and current noise in the amplifier the Johnson noise of the source resistance itself may dominate both amplifier noise sources. This forms the basis of a simple noise measuring circuit. The DUT is configured as a voltage amplifier, its output passes through a bandpass filter and the output noise is measured both when the input is grounded directly and when it is grounded through a resistor. The resistor is chosen to be large enough that when the current noise of the amplifier flows in it the noise voltage developed is more than three times greater than either the amplifier voltage noise or its own Johnson noise. The first measurement gives the voltage noise of the amplifier, the second its current noise.

## OPERATIONAL AMPLIFIER NOISE MEASUREMENT



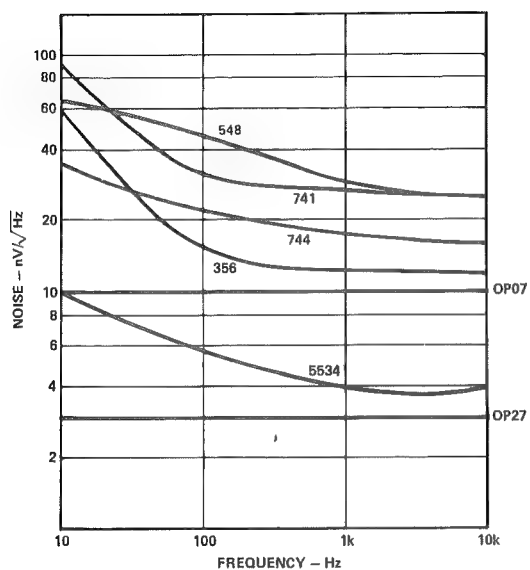
Where a single value is given for the noise of a device (e.g., Noise = 1 $\mu\text{V}$  rms) it should be associated with a band of frequencies and is the total voltage noise of the device within that band. If no frequency information is given the figure should be for the noise in the band from dc to the unity gain frequency. This noise may be specified at a particular source resistance—the specified noise is then the rms sum of the voltage noise and the current noise flowing in that resistance.

A more useful noise specification consists of noise spectral density figure for mid frequencies and the 1/f corner frequency mentioned above. Although such a specification may not contain as much information as might be desired on the relative magnitudes of voltage and current noise it does provide a firm basis for comparisons between devices. Noise is sometimes specified in terms of a graph of total noise up to a given frequency. Such curves may be useful when the noise gain versus frequency characteristics of a circuit are known but it is important to consider both the voltage and current noise curves (and the gain to each with respect to frequency) in a computation of total noise.

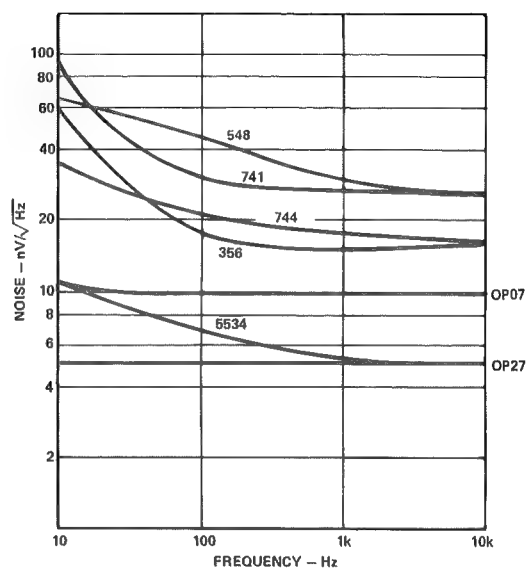
Yet another useful specification is a set of noise spectral density figures (at particular frequencies or plotted as a graph against frequency). The noise spectral density,  $e_n$ , at a given frequency is defined as the rms noise voltage in a 1Hz band surrounding a specified value of frequency. It is usually expressed in nanovolts per root hertz (nV/ $\sqrt{\text{Hz}}$ ). The awkward units arise from the fact that it is noise power which is actually being characterized and voltage is proportional to the square root of power.

The following family of curves demonstrates the noise performance of several common low noise amplifiers at several different values of input resistance. These curves take into account the amplifier voltage noise, the Johnson noise of the source resistance and the voltage noise generated by the input noise current flowing through the source resistance. The relative noise performance of each amplifier is critically dependent upon the source resistance.

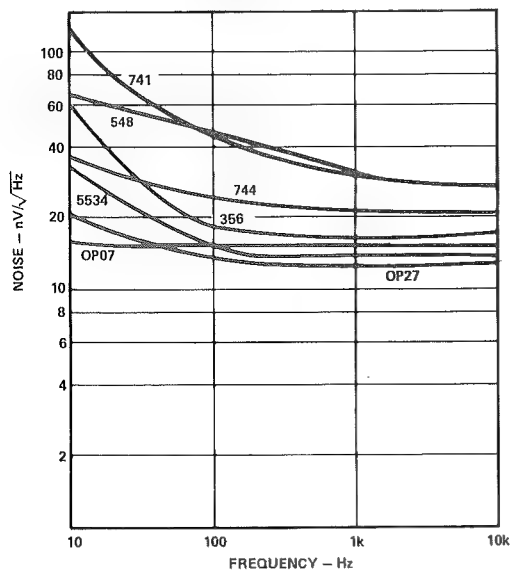
$R_S = 100\Omega$



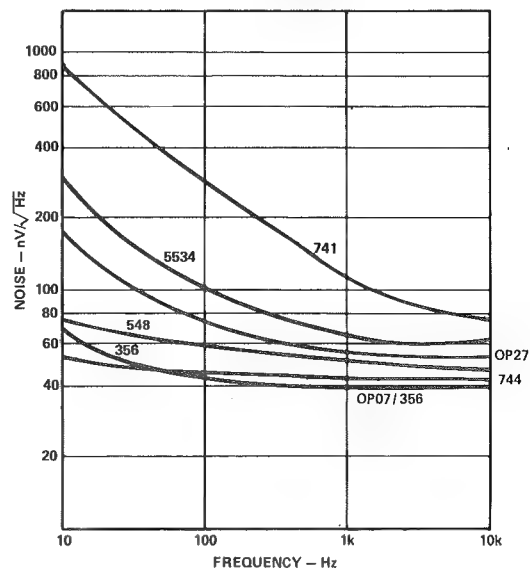
$R_S = 1k\Omega$



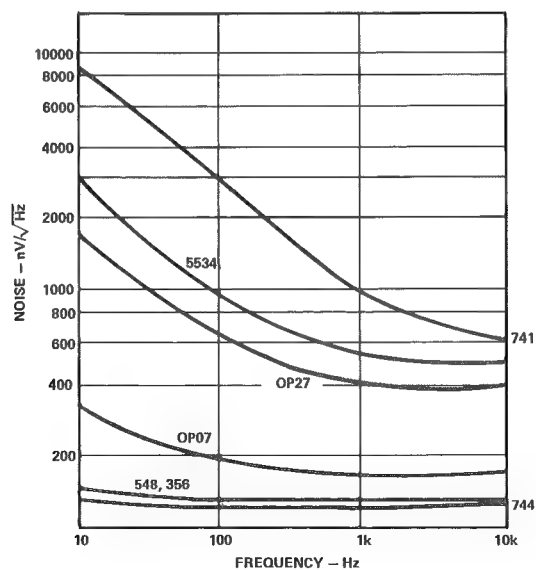
$R_S = 10k\Omega$



$R_S = 100k\Omega$



$R_S = 1M\Omega$



A series of spot noise figures at particular frequencies (10Hz, 100Hz, 1kHz, 10kHz) may be given instead of plots. These numbers are useful for direct comparison of noise characteristics of several amplifiers. Computation of total rms noise in a particular bandwidth requires that the shape of the spectral density curve be known. In the low frequency region, where flicker noise is dominant, the noise at a particular frequency can be computed from the formula.

$$E_n = k/f$$

where  $k$  is the value of  $E_n$  at  $f = 1\text{Hz}$ .

The total  $1/f$  noise in a given bandwidth is given by

$$E_n = k \sqrt{\int_{f_1}^{f_2} \frac{df}{f}} = k \sqrt{\ln \frac{f_2}{f_1}}$$

The total flicker noise in a given band is a function of the ratio of the low and high band edge frequencies since the actual frequency cancels out. It is necessary, however, that the upper band edge is still in the  $1/f$  region. The formula implies that a decade contributes 1.52K (or an octave 0.83K) where  $K$  is the value of  $E_n$  at 1Hz. For example consider an amplifier with  $E_n = 100\text{nV}/\sqrt{\text{Hz}}$  at 1Hz. The total  $1/f$  noise from 0.1 to 10Hz is therefore:

$$\begin{aligned} E_n &= 0.1\mu\text{V}/\sqrt{\text{Hz}} \times 1.52 \sqrt{\log \frac{10}{0.1}} \\ &= 0.1 \times 1.52 \times \sqrt{2} \\ &= 0.21\mu\text{V} \end{aligned}$$

For white noise the computation of total noise is also straightforward. The total rms noise in the band between  $f_1$  and  $f_2$  is given by:

$$E_n = \sqrt{\int_{f_1}^{f_2} e_n^2 df} = e_n \sqrt{f_2 - f_1}$$

If  $f_1$  is less than 10% of  $f_2$ , then ignoring  $f_1$  (i.e., treating it as zero) will introduce less than 5% error. Thus the noise below 10kHz of an amplifier with  $10\text{nV}/\sqrt{\text{Hz}}$  will be

$$\begin{aligned} E_n &= 10\text{nV}/\sqrt{\text{Hz}} \times \sqrt{10^4 \text{ Hz}} \\ E_n &= 1\mu\text{V rms} \end{aligned}$$

In practice it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits since practical filters have finite rolloff characteristics. Fortunately the measurement error induced by a single pole low pass filter is readily computed. The noise in the spectrum above the filter cutoff frequency extends the effective corner frequency to 1.57 times the original  $f_c$  and so if a single pole filter is used in a noise measurement circuit its corner frequency should be set to 0.66 of  $f_2$ . Similarly, a 2 pole filter has an apparent corner frequency of  $1.2f_c$ .

The key points to remember about noise in op amps are:

## SUMMARY OF OP AMP NOISE SPECS

1. Low Frequency Noise Generally Follows a " $1/f$ " (Actually  $1/\sqrt{f}$ ) Characteristic. Total rms Noise in a  $1/f$  Region can be Computed from  $E_n = 1.52k \sqrt{\log \frac{f_2}{f_1}}$  Where  $k = e_n$  at 1Hz.
2. High Frequency Noise Generally Follows a White Noise Characteristic. Total rms White Noise is Computed from  $E_n = e_n \sqrt{f_2 - f_1}$  (or Simply  $e_n \sqrt{f_2}$ , if  $f_2 \geq 10f_1$ ).
3. The " $1/f$  Corner Frequency" can Serve as a Figure of Merit for Comparing Amplifiers.
4. Broadband Noise Test Circuits Should Use Filter Cutoff Frequencies Set for 2/3 of the Desired Bandwidth, to Allow for the Slope of the Filter's Roll-Off.
5. Uncorrelated Noise Sources Add in a Root-Sum-of-Squares Fashion.

The specifications defined in this section are thus far only component specifications. In practical applications it is necessary to examine the importance of each specification relative to the actual application and determine the possible tradeoffs.

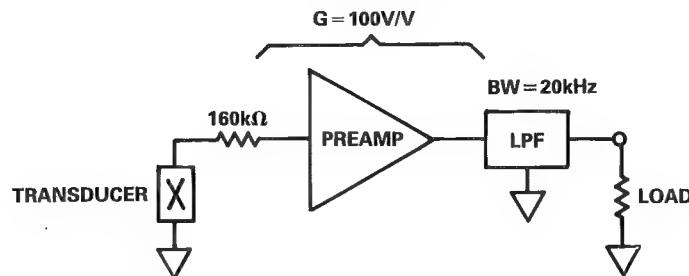
## MAKING SENSE OUT OF NOISE

The sources of noise have been discussed at length, and although we have experienced the limitations imposed by noise (the proverbial background hiss) we have not yet shown quantitatively how the noise renders the input signal less useable. This however will be remedied through the use of the following example.

A well known Beethoven symphony is "Wellington's Victory". This symphony portrays in music Great Britain's famous general, Lord Wellington, commanding an army of 15,000 infantry and 3,000 cavalry, defeating Napoleon and his army at the Battle of Waterloo. The opening movement to the symphony begins with the distant sound of troops marching forward to engage the enemy in an impending battle. Steadily the music increases in intensity, as the troops move within battle range. Suddenly the sound erupts to enormous proportion as cannons boom and rifle shots crack. This absolutely beautiful symphony has to be a favorite, and the significance of this movement lies in the wide dynamic range of sound intensity and easily varies 80dB with peak sound pressure levels reaching 110dB. In the case of this symphony not only is the loudness of the cannons important, but of equal importance is the silence of death as this stillness permeates the battle field which was once filled by living soldiers and charging dragoons.

When this symphony is played from a recording, a limiting factor determining how quiet the music can sound is often the quality of the preamplifier used in the front end of the playback system. In any event this preamplifier should be designed to achieve the lowest possible noise reflected to the input. Generally, the preamplifier has a voltage gain of 40dB, an output signal level of 0.5V rms, a half power frequency (bandwidth) of 20kHz, and an output signal to noise ratio of 80dB. If the transducer driving the input to the preamplifier has an impedance equal to 160k $\Omega$ , what is the minimum signal level that must be available from the transducer to achieve the required preamplifier signal to noise output if the device selected is the AD OP-27?

## SCHEMATIC OF TRANSDUCER AND AMPLIFIER



First compute the noise contributed by the source resistor:

## RESISTOR NOISE VOLTAGE COMPUTATION

$$V_{\text{NOISE}} = \text{RESISTOR} = \sqrt{4 \times K \times T \times B \times R}$$

Where K is Boltzman's Constant =  $1.38049 \times 10^{-23}$  Joules/Kelvin

T is the Temperature in Kelvin

B is the Bandwidth in Hertz

R is the Resistor Value in Ohms

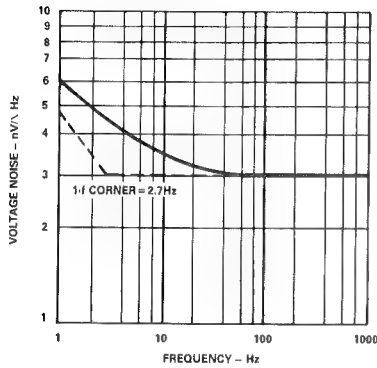
$$V_{\text{NOISE}} = \sqrt{4 \times 1.38049 \times 10^{-23} \times 298 \times 20 \times 10^3 \times 160 \times 10^3} = 7.256 \times 10^{-4} \text{ Volts rms}$$

$$0.162 \mu V$$

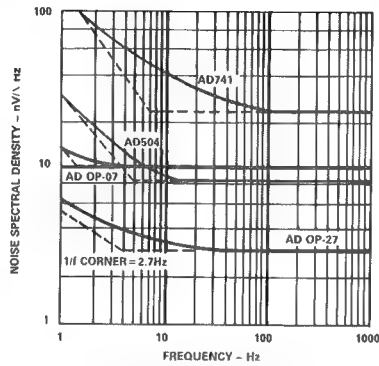
$$\sqrt{72}$$

Second compute the noise contributed by the AD OP-27:

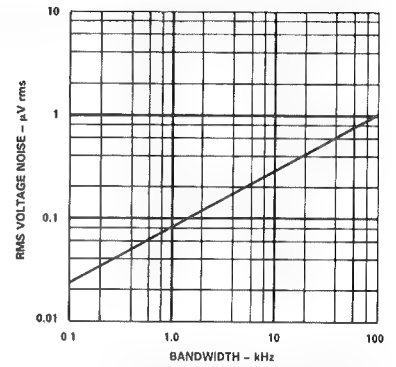
## AD OP-27 NOISE CHARACTERISTICS



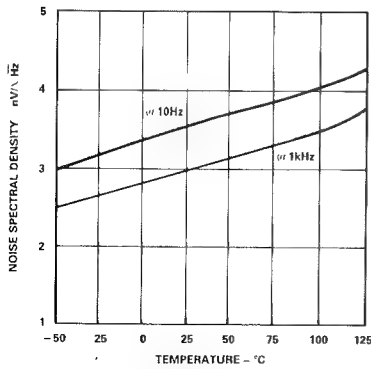
INPUT VOLTAGE NOISE SPECTRAL DENSITY



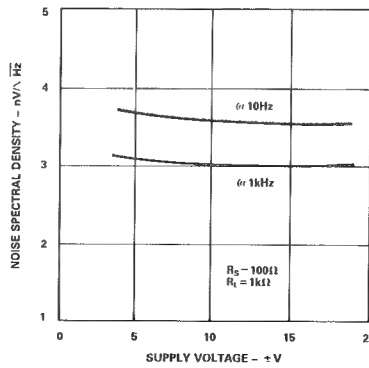
COMPARISON OF OP AMP INPUT VOLTAGE NOISE SPECTRUMS



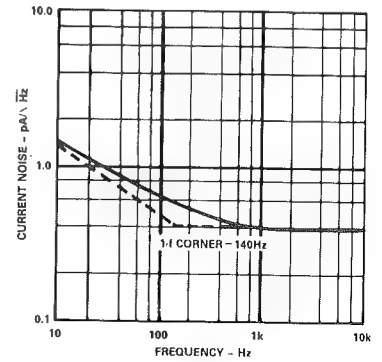
INPUT WIDEBAND NOISE VS. BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



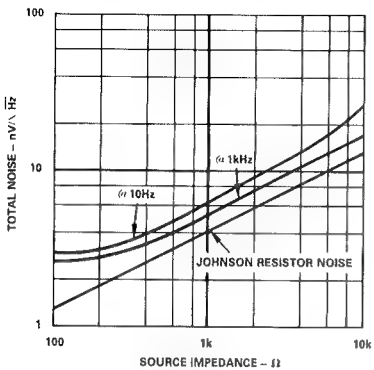
INPUT VOLTAGE NOISE VS. TEMPERATURE



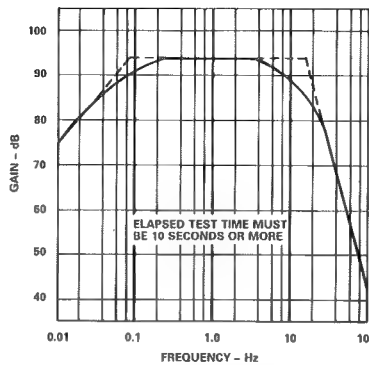
INPUT VOLTAGE NOISE VS. SUPPLY VOLTAGE



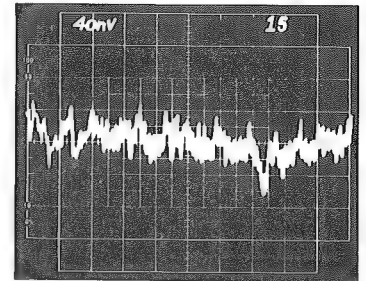
INPUT CURRENT NOISE SPECTRAL DENSITY



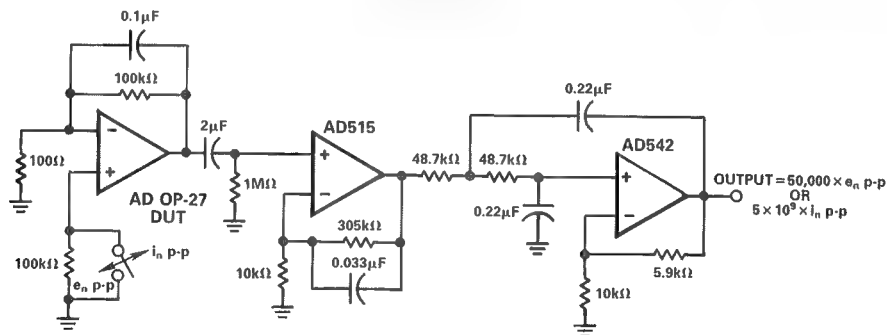
TOTAL NOISE VS. SOURCE IMPEDANCE



0.1Hz TO 10Hz NOISE TEST FREQUENCY RESPONSE



0.1Hz TO 10Hz P-P VOLTAGE NOISE

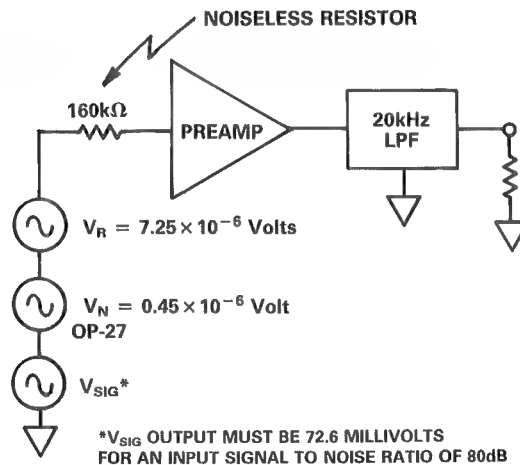


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

0.1Hz TO 10Hz NOISE TEST BANDPASS FILTER (VOLTAGE GAIN = 50,000)

The AD OP-27 data sheet reveals that the wideband noise of the AD OP-27 reflected to the input is 0.45 microvolts rms in a 20kHz bandwidth. The method in which the wideband noise is presented for the AD OP-27 makes the noise comparison easier, for this method gives a sum total regardless of the device specific contributing factor. Clearly in this example the AD OP-27 noise contribution is significantly less than the noise voltage generated by the transducer.

## TRANSDUCER AND AMPLIFIER NOISE CONTRIBUTIONS



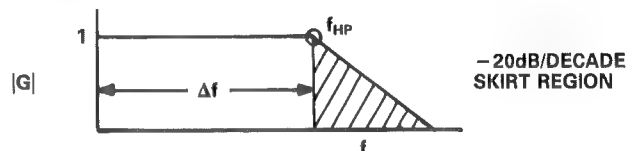
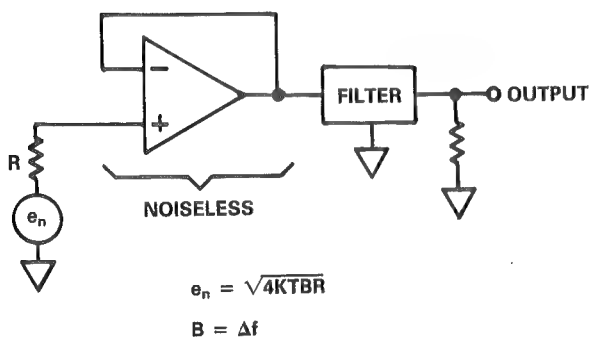
The two sources of noise are the transducer source resistance, and the AD OP-27. It is important to remember that these noise sources are not correlated and the sum contribution is equal to the root sum square of the quantities. This computation is simply the SQUARE ROOT of the sum of the squares.

## ROOT SUM SQUARE CALCULATION

$$\begin{aligned}
 V_{\text{NOISE}} &= \sqrt{V_R^2 + V_N^2} \\
 &= \sqrt{(0.45 \times 10^{-6})^2 + (7.25 \times 10^{-6})^2} = \\
 &= 7.26 \times 10^{-6} \text{ Volts rms}
 \end{aligned}$$

For the preamp output to have an 80dB signal to noise ratio the peak input signal must be 80dB greater than the amplifier noise reflected to the input. Hence the transducer must be capable of producing a peak unloaded signal of 72.6 millivolts.

## NOISE BANDWIDTH CORRECTION



$$G(f) = \frac{1}{1 + jf/f_{HP}}$$

$$f_{\text{NOISE BANDWIDTH}} = f_n = \int_0^{\infty} |G(f)|^2 df = \int_0^{\infty} \left| \frac{1}{1 - j(f/f_{HP})} \right|^2 df$$

$$f_n = \int_0^{\infty} \frac{1}{(1 + f^2/f_{HP}^2)^2} df = \frac{\pi}{2} f_{HP}$$

The 20kHz bandwidth used in the computation of the noise contribution assumed the low pass filter had an infinitely steep skirt response. However, for the mathematicians and purests the bandwidth is corrected by multiplying by  $\pi/2$ , or 1.57. The factor accounts for the noise contained in the skirt region of the filter whose asymptotic response is  $-20\text{dB}$  per decade.

Noise figure is another means of describing the noise characteristics of an amplifier, and can be represented mathematically as follows:

## NOISE FIGURE EQUATIONS

Noise Factor = F

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to source resistance}}$$

OR

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to source resistance}}$$

$$F = 1 + \frac{V_n^2 + I_n^2 R_s^2}{4KTR_s B}$$

$R_s$  = Source Resistance

$U_n$  = AD OP-27 Noise Voltage

$I_n$  = AD OP-27 Noise Current

$K$  = Boltzman's Constant

$T$  = Temperature in Kelvin

$B$  = Bandwidth

$$\text{Noise Figure} = 10 \log \text{Noise Factor} = 10 \log F$$

However, the noise figure can be misleading when applied to small signal amplifiers in the audio range. The misleading aspect arises from the fact that the noise figure of the amplifier in many cases is dependent upon the source resistance. To achieve the optimum noise figures in FETs, for example, it may be necessary to increase the source impedance to tens or megohms. The noise figure may have been improved at the expense of adding considerably more Johnson noise. This is also true to some extent in the design of microwave amplifiers, as there are optimum source impedances to produce the lowest noise figure. The optimum noise source impedance results in a lower gain design, but the minimum discernable signal is lower.

Therefore, it is suggested that whenever considering signals in the presence of noise, *reflect all noises sources to the input* to permit a signal to noise comparison on a one-on-one basis.

## AMPLIFIER TECHNOLOGIES

It is useful for the design engineer to know not only the types of operational amplifier products available, but also the technologies used to produce them. He can then select an amplifier for a particular application from a suitable category of amplifiers and have some familiarity with its probable idiosyncrasies.

### Standard Bipolar Process

The standard junction-isolated bipolar process used in the majority of op amps produces three basic transistors: a high quality vertical NPN transistor, a high quality vertical PNP transistor, and a somewhat lower quality lateral PNP transistor. The vertical PNP is of limited utility since its collector is always connected to the negative power supply. Thus the two transistors which can be used elsewhere in the amplifier circuit are the vertical NPN and the lateral PNP. The lateral PNP is very low performance (low  $\beta$  low  $f_t$ ) and is used primarily in biasing circuitry. It is the NPN, therefore, which is used in the actual signal path as much as possible. An amplifier which uses standard bipolar transistors has bias currents generally in the 100nA to 1 $\mu$ A range, reasonably low offset voltage and drift, and low voltage noise. Examples of these amplifiers include the 741 and 301 types.

### Super-Beta

Super-Beta processing is an addition to the standard bipolar process. With one additional diffusion step, an NPN transistor with a  $\beta$  of several thousand can be produced, reducing input bias current by an order of magnitude, down to 10nA or less. The increased gain of the input stage reduces input bias current and improves common-mode rejection, which are two of the more important specifications of precision amplifiers. Typical open loop gain of a super-beta op amp is several million, common-mode rejection is over 100dB, and input offset voltage characteristics are similar or superior to standard bipolar types. Examples of super-beta amplifiers include the 308, AD510 and AD517 types.

### Dielectric-Isolated (DI) Bipolar

In conventional bipolar and super beta ICs, the individual transistors are isolated from each other by the use of reverse-biased p-n junctions. It is the parasitic capacitance of these junctions which limits the bandwidth of the lateral PNP transistors (and ultimately, the amplifier). The dielectric isolation (DI) process uses a thin oxide layer to provide the isolation between transistors. It then becomes possible to fabricate a high speed PNP transistor and therefore, a high speed amplifier.

The DI process is not without its limitations, however as the oxide layer is easily punctured by electrostatic discharge, resulting in device destruction. Another drawback is the fact the DI circuits require larger geometries than junction-isolated equivalent circuits, resulting in somewhat larger chip sizes.

### Complementary Bipolar

The complementary bipolar process was developed so that both wideband NPN and PNP transistors could be fabricated on the same chip without the use of dielectric isolation. CB is capable of  $F_T$ 's of about 1GHz yielding amplifiers with gain bandwidth's of over 1GHz.

### BIFET

The BIFET process uses ion-implantation to produce a JFET with high breakdown voltage on a chip also containing standard bipolar devices. A pair of these JFETs can be used as input devices for an op amp. The added performance, however, is gained at the expense of generally poorer offset voltage, drift, CMR, and noise specifications. Newer designs allow for factory trimming of BIFET op amp offset voltage and drift.

### BI-MOS

Since JFETs can be used for high-impedance input stages, it is tempting to consider MOSFETs for the same application. Some manufacturers have developed processes which permit MOSFETs to be included on a bipolar IC. Rather than junction leakages inherent in JFETs, MOSFETs ideally have only oxide leakages, which are much lower, potentially reducing input bias current. MOSFETs, however, are ESD sensitive and require protection diodes on the inputs. Very often, these diodes exhibit leakages which are at least as high as the input bias current of a JFET-input amplifier. MOSFETs further tend to be much noisier than JFETs in the audio frequency spectrum, and dc offsets are difficult to control. When MOSFETs are used in the output stage of an op amp, it becomes possible to swing the output very close to the power supply rails. In a conventional bipolar output stage, output swing is limited by saturation voltages and other effects. It is important to note, however, that a MOSFET output stage must be lightly loaded to minimize the effects of  $R_{ON}$ .

### CMOS

Amplifiers constructed entirely of MOSFETs are also available. These amplifiers exhibit poor performance if built along classical op amp designs. Newer designs use CMOS switches and external capacitors to provide offset voltage cancellation similar to the methods used in chopper-stabilized amplifiers. These designs suffer from high noise, poor output drive characteristics, and limited supply voltage ranges.

## MONOLITHIC IC PROCESSES

### STANDARD BIPOLAR

#### Advantages

- Many Suppliers
- Low Noise
- Low  $V_{OS}$ ,  $V_{OS}$  Drift

#### Disadvantages

- High  $I_B$
- Lateral PNP Limits Bandwidth

### BIFET

#### Advantages

- Allows High Breakdown JFET to be Fabricated on Bipolar IC
- High Input Impedance
- Low  $I_B$

#### Disadvantages

- Additional Process Step
- Higher  $V_{OS}$ ,  $V_{OS}$  Drift
- Poorer CMRR
- $I_B$  Doubles Every 10°C Rise in Temperature

### DIELECTRIC ISOLATED BIPOLAR

#### Advantages

- Allows Wide Bandwidth PNP
- Otherwise Similar to Standard Bipolar

#### Disadvantages

- Limited Number of Suppliers
- More Expensive
- ESD-Sensitive

### BI-MOS

#### Advantages

- Uses MOSFET for Potentially Very High Input Impedance
- Inputs can Swing to Supply Rail

#### Disadvantages

- Protection Diode Leakage Defeats Low MOS  $I_B$
- High Noise

### COMPLEMENTARY BIPOLAR

#### Advantages

- Allows Wide Bandwidth PNP & NPN
- Very Fast Settling
- High Current Output
- Low Noise

#### Disadvantages

- Limited Supply Voltage Rating

### CMOS

#### Advantages

- Low Power
- Logic Circuitry and Switches can be Added
- Allows Fabrication of Monolithic Chopper-Stabilized Amplifier

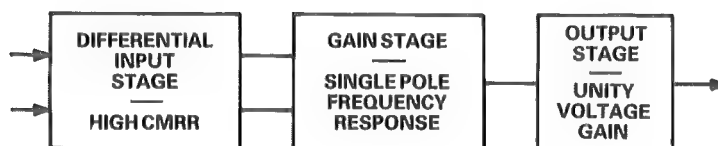
#### Disadvantages

- High Noise
- Limited Output Drive Capability
- Limited Supply Voltage Range



There is an aspect of circuit technology which has an immediate impact on the choice of an op amp—the structure of the input stage. Almost all operational amplifiers have three stages: a differential input stage with good common-mode rejection, a high gain stage with a single pole frequency response which converts the differential output of the first stage to a single-ended signal to drive the output stage, and an output stage.

### TYPICAL OPERATIONAL AMPLIFIER ARCHITECTURE



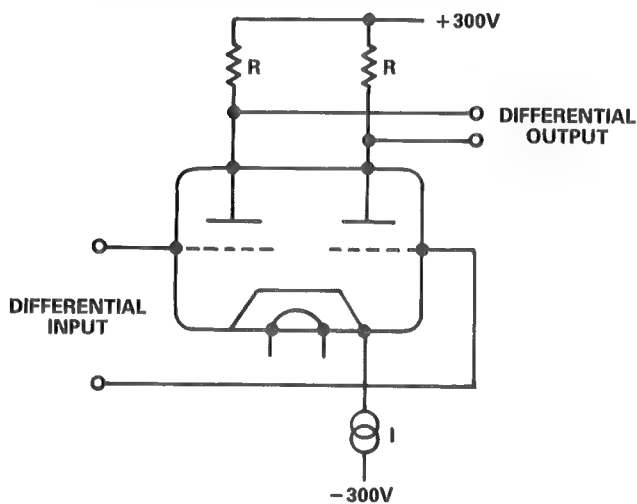
There are differences in the gain and output stages which are possible with different technologies but they are relatively unimportant. The choice of input stage technology is critical. There are three basic input stage technologies: simple bipolar, bias compensated bipolar, and field-effect transistor (FET).

### CHARACTERISTICS OF OP AMP INPUT STAGES

	SIMPLE BIPOLAR	BIAS-COMPENSATED BIPOLAR	FET
OFFSET VOLTAGE	LOW	LOW	MEDIUM
OFFSET DRIFT	LOW	LOW	MEDIUM
BIAS CURRENT	HIGH	MEDIUM	LOW – VERY LOW
BIAS MATCH	EXCELLENT	POOR (CURRENT CAN BE IN OPPOSITE DIRECTIONS)	FAIR
BIAS/TEMP VARIATION	LOW	LOW	BIAS DOUBLES FOR EVERY 10°C RISE
NOISE	LOW	LOW	FAIR

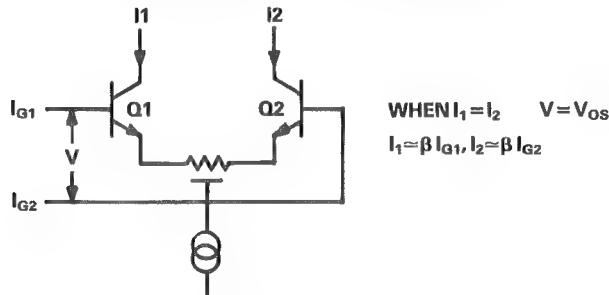
All three differential input stages use the basic “long-tailed pair” of amplifying devices. These design was originally developed with thermionic tubes but may be constructed with any amplifying device: tubes, transistors or FETs. Two similar devices have a common cathode/emitter/source connection, fed from a current source, the input is applied differentially to the grids/bases/gates, and the output is taken differentially from two resistive loads in the anodes/collectors/drains.

### BASIC “LONG-TAILED PAIR” DIFFERENTIAL AMPLIFIER



Let us consider op amps with a bipolar transistor input stage. By diffusing them close together on a single chip and paying close attention to geometry and photo-engraving accuracy it is possible to manufacture a pair of bipolar transistors whose characteristic are very closely matched. When such a pair of transistors is used in a differential amplifier they will have virtually identical values of  $V_{BE}$  when their emitter currents are equal and so the offset voltage of the amplifier will be very low. Moreover, by using a chip-trimming technique such as zener zap or laser trim it is possible to reduce this offset still further.

### SIMPLE BIPOLAR TRANSISTOR DIFFERENTIAL AMPLIFIER

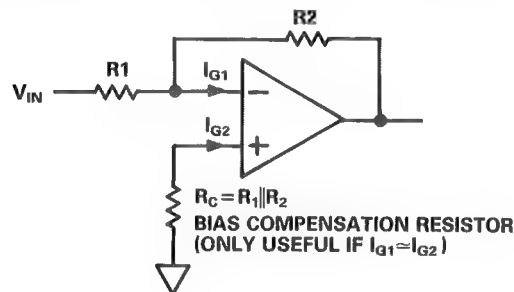


Such a simple stage has excellent characteristics. It has very good offset and low offset drift with temperature (it is a useful feature of bipolar differential amplifiers that when they are trimmed for minimum offset they are thereby also trimmed for minimum drift). In addition they have low noise, wide common-mode range and good frequency response provided that the current in the input stage is not too low.

Their major disadvantage is their bias current. Normal bipolar transistors have current gain ( $\beta$ ) in the range 100 to 500 and there is a type (known as the super- $\beta$  transistor) with values as high as 5000. This means that the bias current in a simple bipolar op amp will be somewhere between 0.02% and 1% of the input stage emitter current—which means that it will probably lie between 50nA and 2 $\mu$ A. This is a major disadvantage in many op amp applications and is only partially offset by the excellent matching of these bias currents and their limited variation with temperature ( $\beta$  increases with temperature so bias currents decrease—typically  $I_B$  at 125°C is roughly 50% of  $I_B$  at -55°C).

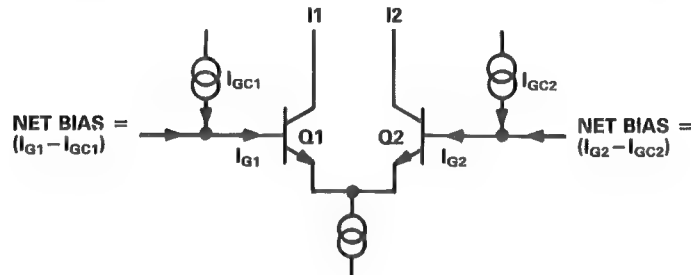
Because the currents are so well matched it is sometimes possible to compensate for their magnitude by the use of a bias compensation resistor. If the resistance seen by each input of an op amp is the same, the voltage drop due to bias currents will cancel out IF THE BIAS CURRENTS ARE EQUAL. Bias compensation is thus useful only with op amps having roughly equal bias currents in the inverting and noninverting inputs and in applications where the signal source impedance is known and constant.

### A BIAS COMPENSATION RESISTOR CAN MINIMIZE BIAS CURRENT ERRORS



The second type of op amp input stage is known as the “bias compensated bipolar input stage”. Despite the similar names it has no relation to the circuit technique described above. In a bias compensated input stage we have a standard bipolar input stage which is equipped, on chip, with current sources to provide its input bias currents.

### BIAS COMPENSATED BIPOLAR INPUT STAGE (Net Bias Current May Flow In Either Direction)

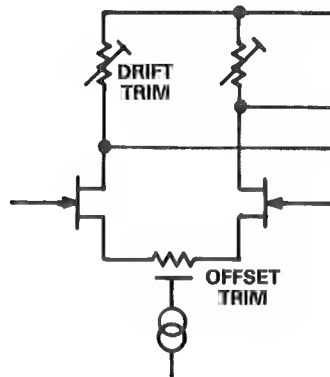


Such an architecture has most of the advantages of normal bipolar input stage: low offset, low drift, low noise and the possibility of high frequency operation. It also has much lower bias currents since the bias current flowing in the external circuitry is only the residual mismatch current between the bias current source and the transistor base. Typical values lie between 1 and 20nA and do not vary greatly with temperature.

However the bias currents in the inverting and noninverting inputs in op amps of this type are not well matched and may even flow in opposite directions (if the bias source current is greater than the base current there will be a net current flow OFF the chip—if it is less than the base current the flow will be ONTO the chip). Bias compensating resistors are therefore inappropriate for amplifiers of this type.

Even bias currents of a few nanoamps can be inconvenient in many applications. Where this is the case FET input op amps should be used. Originally it was necessary to use hybrid techniques in order to combine an FET input stage with bipolar op amp circuitry but the introduction of the “BiFET” process allows the fabrication of both types of device on the same chip. Recent developments in the BiFET process allow the manufacture of monolithic op amps with bias currents as low as 60fA (the AD549).

### FET OP AMP INPUT STAGE Offset and Drift Must Be Trimmed Separately



The gate current of a junction FET is not related to its source current but is the leakage current of the reverse biased diode forming its gate. The bias current of FET input op amps is therefore independent of the current in the input stage and so high speed amplifiers may still have very low bias current.

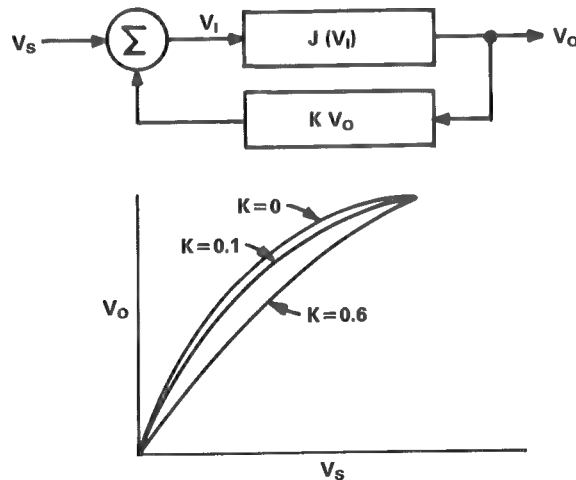
However, there are disadvantages to the architecture. Diode leakage current is not temperature stable, doubling for every 10°C increase in chip temperature, so that an amplifier with a bias current of 50pA at room temperature (25°C) has a bias current of 50nA at the military maximum of 125°C. The bias currents of an FET op amp are not well matched so bias compensation resistors may not be used with it.

Like bipolar amplifiers, FET amplifiers may have their offset voltage trimmed on the chip by laser or zener zap. Unlike bipolar amplifiers there is no intrinsic drift trim in the process—if an FET amplifier is trimmed for minimum offset its temperature coefficient is not minimized, but it may be separately laser trimmed to a minimum (zener zap is unsuitable for this), although it is necessary to make measurements with the silicon wafer at two different temperatures in order to do this. The result of this added complexity of trim is that the offset voltage and drift of an FET amplifier are larger than those of bipolar amplifiers, even though the bias currents are far lower. Which type of amplifier is chosen will depend on the application.

## LINEARITY AND DISTORTION

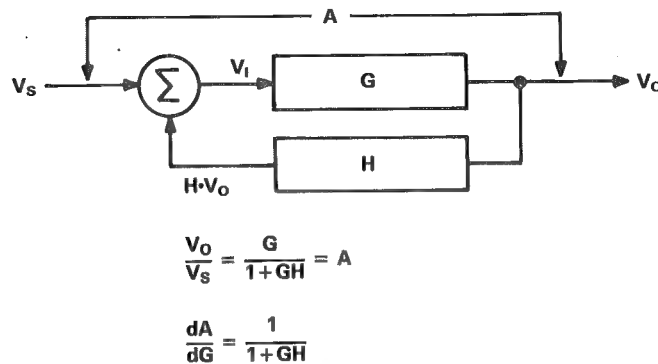
An ideal amplifier produces an exact scaled replica of its input signal at its output. To do this the slope of its transfer characteristic must be constant. Altering the shape of the input signal between the input and the output is referred to as “distorting” it. Distortion is a result of a processing a signal in a nonlinear system. A remarkable property of feedback amplifiers is their ability to improve linearity through the use of feedback. The actual mechanism by which this is accomplished is not obvious but may be approached by using a combination of analytical and graphical techniques.

### FEEDBACK IMPROVES LINEARITY



The effect of adding feedback to improve linearity may be treated mathematically. These methods of analysis become increasingly more important as the total harmonic distortion (THD) in an amplifier is used as a criterion for selecting it.

### NONLINEARITY GAIN SENSITIVITY

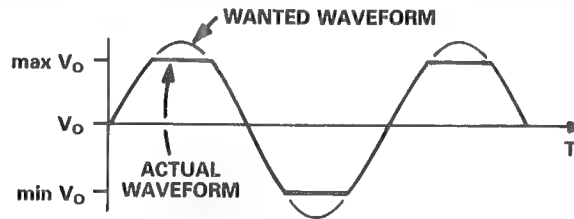


**INCREASING THE PRODUCT  $GH$  REDUCES THE SENSITIVITY OF THE OVERALL AMPLIFIER TO VARIATION OF  $G$  AND HENCE REDUCES NONLINEARITY.**

It is difficult to discern the presence of distortion on a sinusoidal waveform visually by using an oscilloscope—our eyeballs are just not calibrated to detect slightly distorted sinusoids (it is sometimes less difficult to perceive distortion on non-curved waveforms such as pulses and square, triangular and sawtooth waves). The most effective means of measuring distortion is to use a spectrum analyzer and measure the harmonically related components resulting from the nonlinear characteristics of an amplifier. A truly linear amplifier does not change the shape of an input signal—it merely scales it, likewise an amplifier with nonlinearity does change the waveshape and so causes distortion.

The most common form of distortion is "limiting" or "clipping" and occurs when the required output voltage from an amplifier is larger than the maximum voltage that the amplifier can actually provide (the output is said to exceed the amplifier's "headroom" or to "limit"). Symmetrical clipping introduces high levels of odd-harmonics into a waveform, asymmetrical clipping introduces even harmonics as well. The cures are either to reduce the gain of the amplifier or to increase its supply voltages.

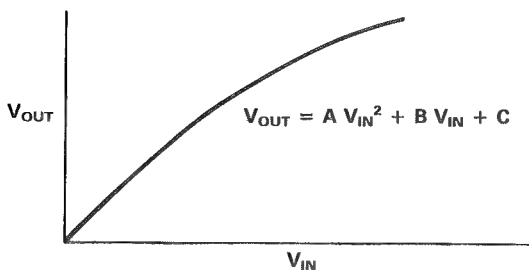
### CLIPPING OCCURS WHEN THE REQUIRED OUTPUT AMPLITUDE EXCEEDS THE POSSIBLE OUTPUT AMPLITUDE



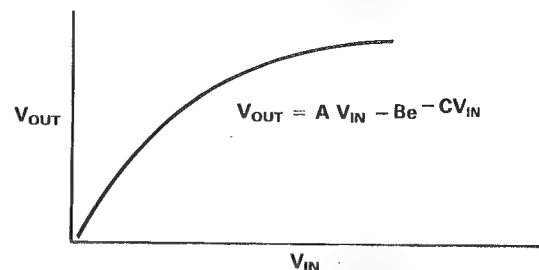
Although clipping may be considered a gross form of nonlinearity the term is normally reserved for phenomena which cause the central part of the amplifier transfer characteristic to deviate from a straight line. Consider a 12-bit system with a full scale range of 10 volts. If the system is specified to be linear to 12-bits it implies that the maximum deviation from the ideal transfer curve is 1LSB (2.44mV).

The two most common type of nonlinearity are square law and logarithmic. Square law nonlinearity occurs when there is a quadratic term in the transfer characteristic of the amplifier and can be produced by a field effect transistor with a resistive load. Logarithmic nonlinearity is produced by a logarithmic (inverse exponential) term in the transfer characteristic and can be caused by bipolar transistors and diodes.

### BASIC TYPES OF NONLINEARITY (In Reality Many Forms of Distortion Will Contain Both)



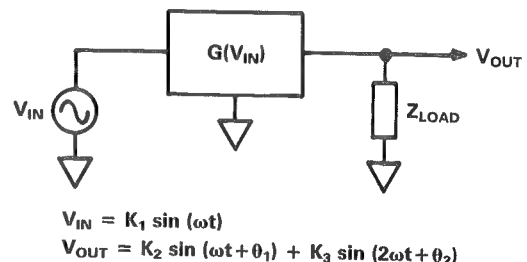
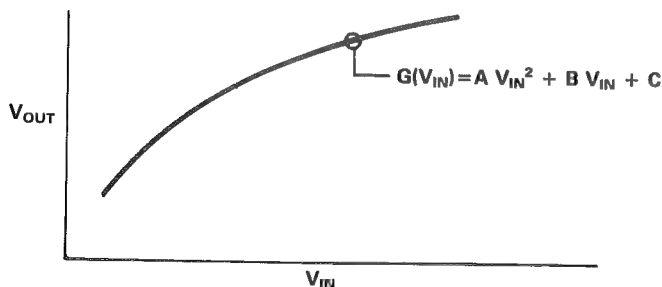
SQUARE LAW NONLINEARITY



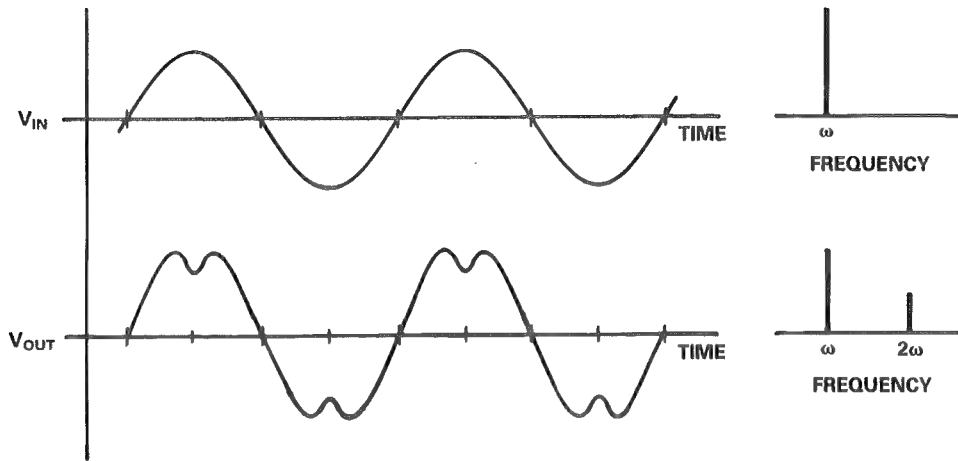
LOGARITHMIC NONLINEARITY

These types of distortion may be modelled by adding either a parabola or a rising exponential (or both) to the device transfer characteristic but it must be appreciated that distortion mechanisms are rarely simple and generally have several distinct causes. Models are thus rarely very accurate. Square law approximation of a nonlinear transfer function can be accomplished using curve fitting techniques, but the important thing to remember is square law transfer characteristics produce second harmonic terms only.

### QUADRATIC DISTORTION

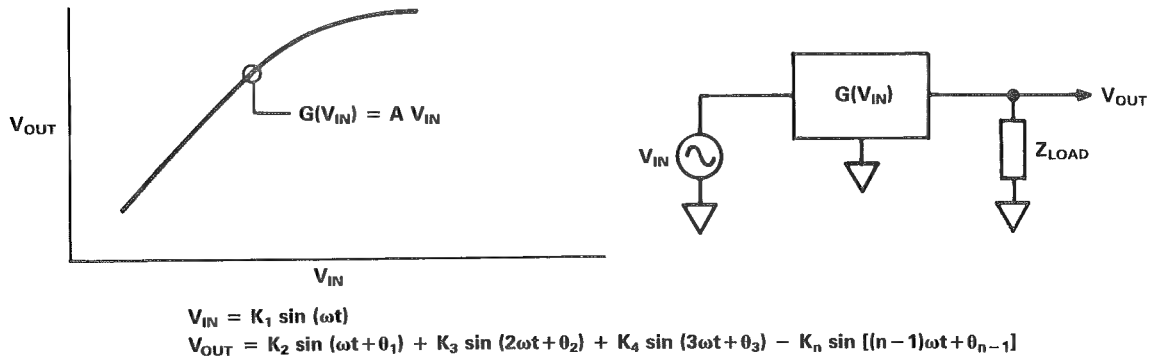


## QUADRATIC DISTORTION

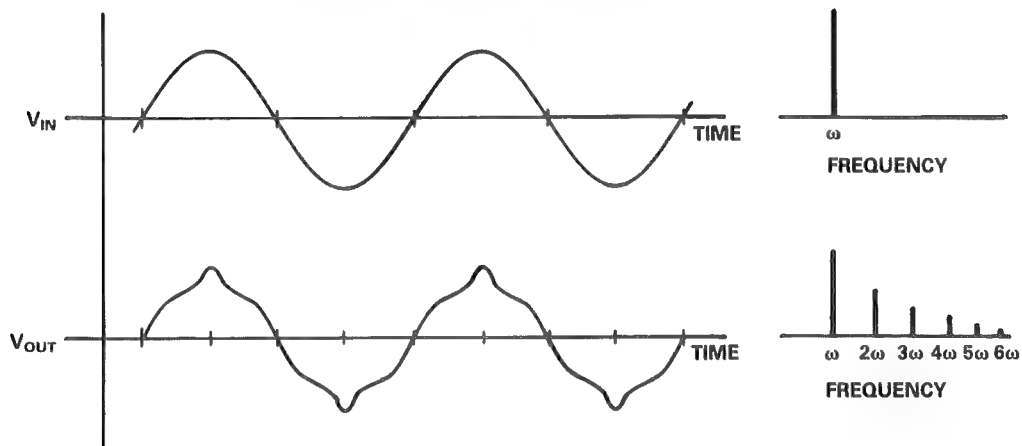


Exponential transfer functions are a bit trickier to analyze, as some are regarded as transcendental. Subsequently the curve fitting equations used are exponential and not quadratic. The result of a logarithmic transfer function is to distort an input signal thus producing both odd and even harmonics in the output signal. This differs fundamentally from the quadratic which produces second harmonics only.

## LOGARITHMIC DISTORTION



## LOGARITHMIC DISTORTION



## SELECTING THE RIGHT AMPLIFIER FOR THE APPLICATION

1. Consider the Signal Source
2. Analyze the Effects of Op Amp Specs on the Application
3. Determine Environmental Variations
4. Don't Spend More (or Less) Than Necessary

The choice of an operational amplifier is generally governed by the application in which it is to be used. The process of selecting the best amplifier for an application involves a rigorous analysis of error sources—both in the amplifier and in the external components. It is important to analyze the characteristics of the input signal, the desired accuracy and the environmental conditions to which the circuit will be subjected. In this section of the seminar we shall consider a series of op amp applications and outline the principles behind the amplifier selection.

### "WHAT DO YOU DO WHEN A 741\* WON'T DO?"

- A. Impossible — 741s Can Do Anything
- B. Use A 741 Anyway and Hope Nobody Notices
- C. Use A Dual 741 (Two Amps are Better than One)
- D. Give Up and Take Up Computer Programming
- E. Select an Amplifier with Specs Which Match the Application

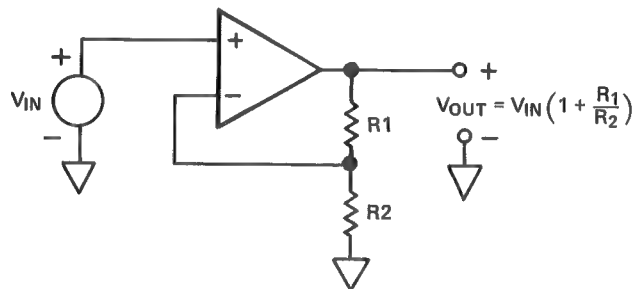
\*Or 301A, 308A, 356A, or Whatever General-Purpose Op Amp You Use "Everywhere".

### PREAMPLIFIER APPLICATIONS

Operational amplifiers were originally intended for use inside analog computational circuits, where feedback networks allowed them to perform analog operations such as integration and differentiation. They are now widely used as low cost gain stages. The choice of op amps in such applications depends upon the characteristics of the signal source, the gain stage and the desired accuracy.

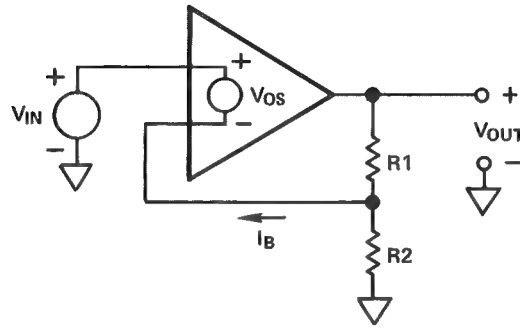
Consider a noninverting preamplifier built with an ideal op amp and ideal resistors, and intended for amplifying a low level signal. The output will be equal to the input times one plus the resistor ratio.

### IDEAL NON-INVERTING GAIN STAGE



The input offset voltage of the op amp will appear as a voltage source in series with the signal, and will be amplified along with it. Any bias current in the amplifier input will flow in the source resistance and develop an additional offset voltage which will also be amplified. Interestingly, since the voltage produced by the bias current is equal to  $I_B(R1R2/(R1 + R2))$  and the gain applied to this voltage is  $(R1 + R2)/R2$  the net effect at the output is a term equal to  $I_BR1$ .

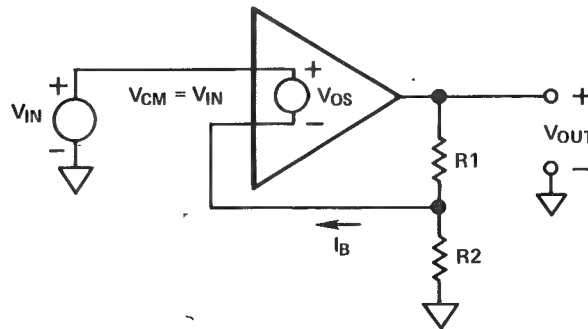
## NON-INVERTING AMPLIFIER FIRST-ORDER ERRORS



$$V_{OUT} = \left[ V_{IN} \left( 1 + \frac{R_1}{R_2} \right) + V_{OS} \left( 1 + \frac{R_1}{R_2} \right) + I_B R_1 \right] = \left( 1 + \frac{R_1}{R_2} \right) \left[ V_{IN} + V_{OS} + I_B \left( \frac{R_1 R_2}{R_1 + R_2} \right) \right]$$

Common mode effects cause an additional error in noninverting amplifiers. Although an ideal op amp is insensitive to common-mode inputs, real amplifiers do respond to them. This error term can be modeled at the input as an additional offset voltage equal to common-mode voltage divided by CMRR. As an offset, it is amplified by the same amount as the signal.

## NON-INVERTING AMPLIFIER SECOND-ORDER ERRORS

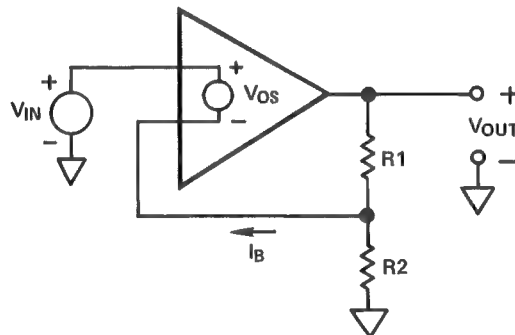


$$V_{OUT} = \left[ V_{IN} \left( 1 + \frac{R_1}{R_2} \right) + V_{OS} \left( 1 + \frac{R_1}{R_2} \right) + I_B R_1 + \left( \frac{V_{IN}}{CMRR} \right) \left( 1 + \frac{R_1}{R_2} \right) \right]$$

$$= \left( 1 + \frac{R_1}{R_2} \right) \left[ V_{IN} + V_{OS} + I_B \left( \frac{R_1 R_2}{R_1 + R_2} \right) + \left( \frac{V_{IN}}{CMRR} \right) \right]$$

Finite open loop gain adds yet another error. It can be shown that the actual gain of the circuit will be equal to the desired gain multiplied by  $1 + [1/A_{OL} \cdot \beta]$  where  $A_{OL}$  is the amplifier's open loop gain and  $\beta$  is the voltage feedback ratio.

## GAIN ERROR INTRODUCED BY FINITE $A_{OL}$



$$V_{OUT} = \left( \frac{R_1 + R_2}{R_1} \right) \left[ V_{IN} + V_{OS} + I_B \left( \frac{R_1 R_2}{R_1 + R_2} \right) + \frac{V_{CM}}{CMRR} \right] \left[ \frac{A_{OL} \frac{R_2}{R_1 + R_2}}{1 + A_{OL} \frac{R_2}{R_1 + R_2}} \right]$$



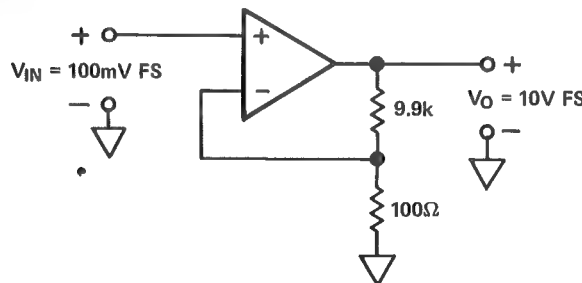
A numerical example may assist in the appreciation of the relative magnitudes of these errors. Consider a noninverting preamplifier with a gain of 100, built with perfect resistor, and intended to amplify 100mV to 10V. We might choose to use an AD741 or an AD OP07.

## COMPARISON OF AD741 AND ADOP-07 SPECIFICATIONS

	AD741CH	ADOP-07CH
$V_{OS}, \text{Max}$	6mV	150 $\mu$ V
$I_B, \text{Max}$	500nA	7nA
CMR, Min	70dB	100dB
$A_{OL}, \text{Min}$	20,000V/V	1,200,000V/V

The largest error is due to offset voltage. Since this error can be reduced or eliminated by trimming it might be thought that it can be neglected but temperature induced offset drifts are not so easily corrected.

## COMPARISON OF 741C AND OP-07C PERFORMANCE



$$V_{OUT}|_{741C} = (100) \left[ 0.1 - 0.006 - (500\text{nA} \times 100\Omega) - \frac{0.1}{3500} \right] \left[ \frac{(20000) \left( \frac{1}{100} \right)}{1 + (20000) \left( \frac{1}{100} \right)} \right]$$

$$= 9.3922 \left[ \frac{200}{201} \right] \text{ V (6.08\% ERROR)}$$

$$= 9.3455\text{V (6.54\% ERROR)}$$

$$V_{OUT}|_{OP-07C} = (100) \left[ 0.1 - 0.00015 - (7\text{nA} \times 100\Omega) - \frac{0.1}{100000} \right] \left[ \frac{1.2 \times 10^6 \times \frac{1}{100}}{1 + (1.2 \times 10^6) \left( \frac{1}{100} \right)} \right]$$

$$= 9.98493 \left[ \frac{12000}{12001} \right] \text{ V (0.15\% ERROR)}$$

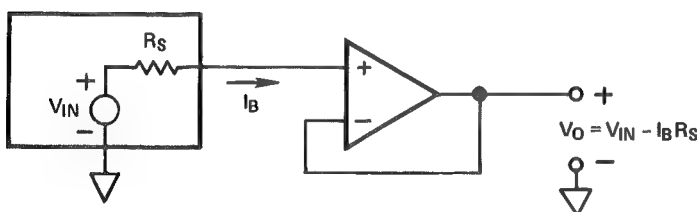
$$= 9.98409\text{V (0.159\% ERROR)}$$

It is also possible to reduce bias current errors by matching the impedance seen at each input of the op amp. The resultant error is now  $I_{OS}$  times the source resistance. CMRR and  $A_{OL}$  induced errors cannot be compensated because they are not constant. CMRR is often a nonlinear function of common-mode voltage.

Noninverting gain stages are often used to buffer high impedance sources. In these applications bias current may be the primary error source. Consider a pH or other ion selective electrode. The desired signal is a few hundred millivolts but the source impedance can exceed 100 megohms and is neither well defined nor stable.

An FET input op amp is the only practical choice for such applications. Consider a simple voltage follower with a wanted signal of  $V_{IN}$ —the actual signal being amplified is  $V_{IN} - I_B R_S$ .

## EFFECT OF BIAS CURRENT IN BUFFER AMPLIFIER



OP AMP  
IDEAL  
AD741  
AD OP-07  
AD711  
AD549

$I_B$   
0  
500nA  
7nA  
15pA  
60fA

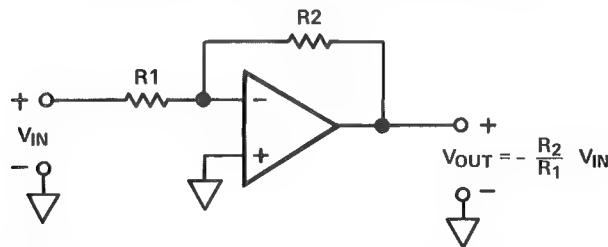
ERROR FOR  
 $R_S = 10\text{M}\Omega$   
0  
5V  
70mV  
0.15mV  
0.6 $\mu$ V

With a 10M source resistance the 500nA bias current of an AD741 op amp will produce an error of about 5V whereas the 60fA of an AD549 FET input electrometer amplifier gives an error of 0.6μV. Neither amplifier should be used in the application: the error from the AD741 is intolerable, while the voltage offset of the AD549 is so much greater than the 0.6μA bias related error that use of an AD549 would be overkill. The correct choice is a less expensive FET input amplifier such as the AD711C which has less than 25pA bias current (giving 250μV error) or the AD545 which has 1pA bias current (giving 10μV error at 25°C and [bias doubling every 10°C] under 250μV at 70°C).

## THE INVERTING AMPLIFIER

Many circuits require a signal to be inverted as well as amplified. Op amps are easily configured for such negative gain. An inverting amplifier consists of an op amp and two resistors, R1 and R2. The noninverting input of the op amp is grounded, its output is connected to its inverting input by R2 and the input signal is applied to the inverting input through R1. Negative feedback keeps the inverting input at the same potential as the noninverting input. This means that the currents in the two resistors must be equal—so that voltages on them must be in the ratio R1:R2 and the output voltage (V<sub>O</sub>) must be  $-R_2/R_1$  times the input voltage (V<sub>IN</sub>). The input impedance is equal to R1 (unlike the noninverting amplifier which has a very high input impedance).

### IDEAL INVERTING AMPLIFIER

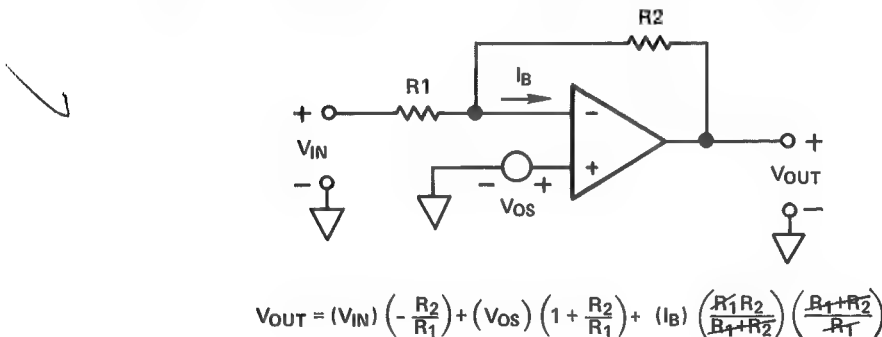


The error analysis of an inverting amplifier differs slightly from that of a noninverting amplifier. Since inverting amplifiers cannot have common-mode voltages CMRR is unimportant but errors due to offset and internal noise are actually amplified more than the signal is. The input offset and noise voltages can be modeled as a voltage source in series with the inputs. The gain seen by this offset/noise voltage is  $(1 + R_2/R_1)$  which is the inverting gain plus 1. Where the desired signal gain is low (particularly where the inverting gain is less than unity), this increased offset/noise gain can be troublesome.

### NOTE THAT IN AN INVERTING AMPLIFIER:

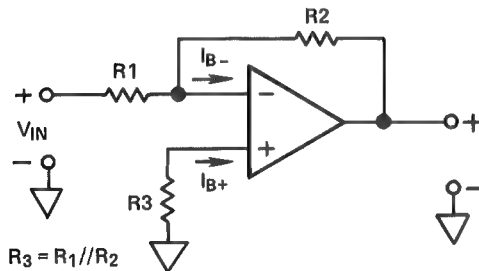
1.  $V_{CM} \approx 0$  so CMRR is Not as Important as it is in a Noninverting Amplifier.
2. "Noise Gain" is Equal to Signal Gain Plus 1. Offset Voltage will be Amplified More than the Signal.

### INVERTING AMPLIFIER WITH FIRST-ORDER ERRORS



Input bias current is another source of error in inverting amplifiers. The bias current flows through a resistance equal to the parallel resistance of  $R_1$  and  $R_2$  creating an offset voltage which is again amplified by  $(1 + R_2/R_1)$  which gives us a bias related output error of  $I_B R_2$ . It is common practice to add a resistance  $R_3$  (equal to the parallel resistance of  $R_1$  and  $R_2$ ) in series with the noninverting input so that the bias related offset  $I_B R_3$  is compensated by an equal and opposite voltage in the noninverting input. As mentioned in an earlier section this resistive bias compensation is only effective in simple bipolar op amps where the bias currents are approximately equal—in bias compensated and FET op amps (whose bias currents may be seriously unequal—i.e.,  $I_{OS}$  may be as large as or larger than  $I_B$ ) the use of this type of bias current compensation may actually increase errors. It does also introduce a small common-mode voltage into the system but this is most unlikely to produce significant errors.

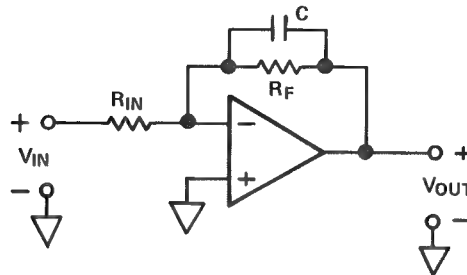
## USE OF BIAS CURRENT CANCELLATION RESISTOR



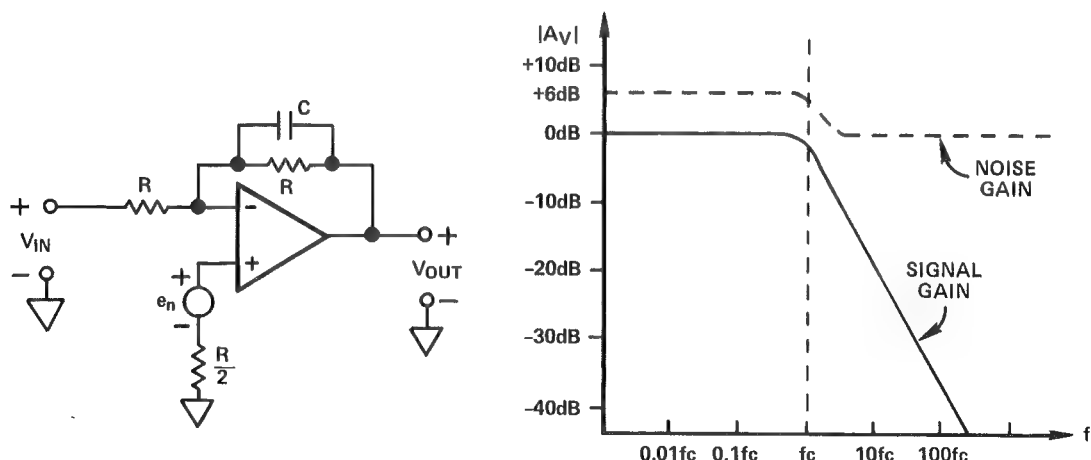
$$\begin{aligned} V_{OUT} &= -V_{IN} \left( \frac{R_2}{R_1} \right) + \left[ (I_{B-} R_2) - (I_{B+} R_3) \left( \frac{R_1 + R_2}{R_1} \right) \right] \\ &= -V_{IN} \left( \frac{R_2}{R_1} \right) + \left[ (I_{B-} R_2) - \left( I_{B+} \frac{R_1 R_2}{R_1 + R_2} \right) \left( \frac{R_1 + R_2}{R_1} \right) \right] \\ &= -V_{IN} \left( \frac{R_2}{R_1} \right) + [ (I_{B-} - I_{B+}) R_2 ] \\ &= -V_{IN} \left( \frac{R_2}{R_1} \right) + I_{OS} R_2 \end{aligned}$$

The useful dynamic range of any amplifier is limited by the input level at which clipping occurs and by the random noise generated within the circuit. In analyzing the effects of noise it is important to consider the frequency response of the noise gain. The gain of an inverting amplifier with a capacitor in parallel with  $R_2$  will drop at 6dB/octave forever from the frequency at which the reactance of the capacitor equals  $R_2$ —the noise gain of the same circuit drops at the same rate (but the noise gain was higher than the signal gain to begin with) but only drops to unity, after that it remains constant with rising frequency. Thus as the frequency goes up the ratio of signal gain to noise gain degrades at 6dB/octave.

## INVERTING AMPLIFIER WITH INTEGRATING CAPACITOR

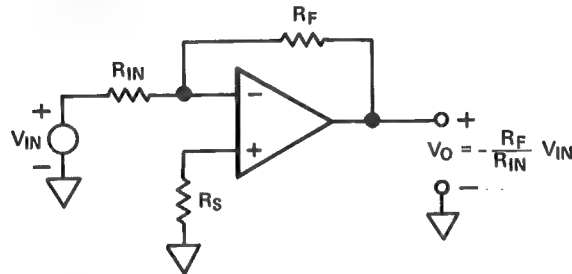


## FREQUENCY RESPONSE OF UNITY-GAIN INVERTING AMPLIFIER



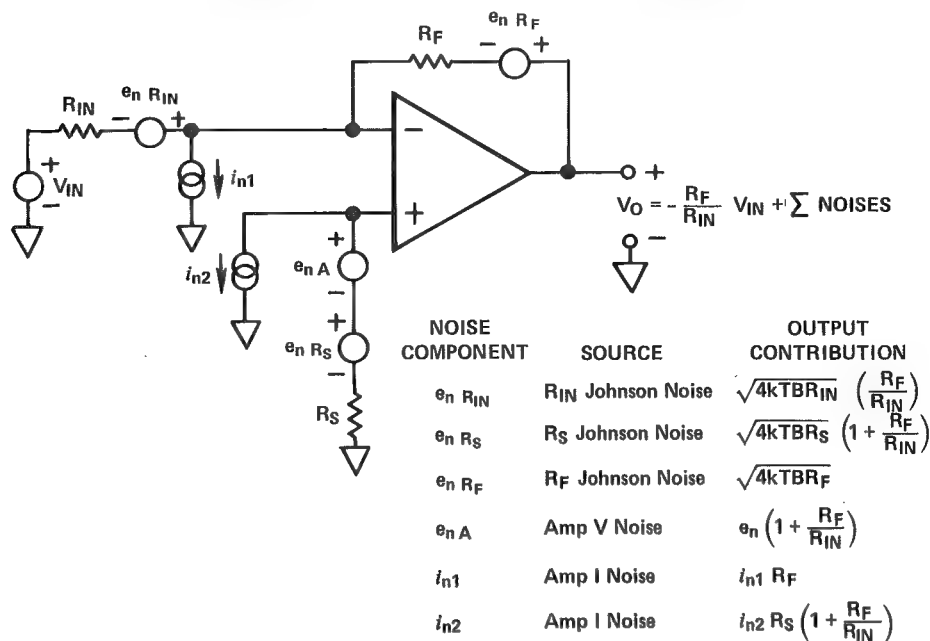
In addition to considerations of noise gain there are other factors which must be taken into account when designing op amp circuits for low noise. If we assume all components to be free of noise an amplifier circuit is easy to model.

## NOISELESS INVERTING AMPLIFIER



Such a model is completely unreal since even perfect resistors have Johnson noise at any temperature above absolute zero. The noise model of a real inverting amplifier contains six separate uncorrelated noise sources! These are the three amplifier noise sources (differential voltage noise and the current noises in each input—which develop noise voltages when they flow in the circuit resistors) and the Johnson noise in the input resistor, the bias compensation resistor and the feedback resistor (this last is often overlooked because it is not in the input circuitry but it can be important).

## NOISE IN INVERTING AMPLIFIER



As mentioned in an earlier section the Universe is a noisy place and it is not always possible to achieve both the noise performance and the impedance levels that one requires simultaneously. Understanding the theory behind noise can be of great assistance in designing circuits and systems with optimum noise performance.

## CHOOSING AN AMPLIFIER FOR LOW NOISE

1. Examine Circuit Impedances.
2. Determine Noise Voltage Gain.
3. Trade Off Between Low Current Noise and Low Voltage Noise.
4. Note that the Desired Noise Performance May Be Physically Impossible if Impedances are too High.

## FILTER APPLICATIONS

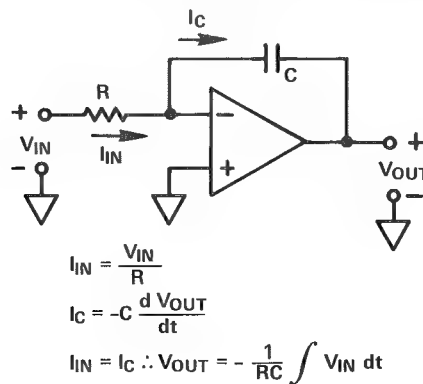
A filter is a circuit which amplifies some of the frequencies applied to its input and attenuates others. There are four common types: high pass, which only amplifies frequencies above a certain value; low pass, which only amplifies frequencies below a certain value; bandpass, which only amplifies frequencies within a certain band; and bandstop, which amplifies all frequencies except those in a certain band.

Filters may be produced using many different methods. These include passive filters which use only passive components such as resistors, capacitors and inductors, filters which use mechanical resonances in quartz or other piezo-electric materials as a means of constructing frequency dependent circuitry, digital filters which use analog-digital converters to convert a signal to digital form and then use high-speed digital computing techniques to filter it, and active filters which use amplifiers in addition to resistors, capacitors and inductors in order to obtain performance impossible with passive filters. Operational amplifiers are frequently used as the gain blocks in active filters. While it is beyond the scope of this text to provide a detailed study of active filter design some important considerations will be discussed.

### Integrators (Low Pass Filters)

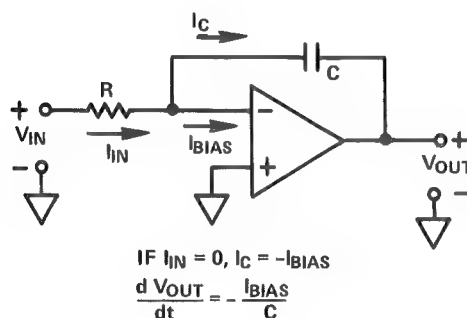
The ideal integrator uses a perfect op amp in the inverting configuration with a capacitor in the feedback path. It provides an output signal which is proportional to the integral of the input signal. The op amp maintains both inputs at zero volts, so the input current,  $I_{IN}$ , is equal to  $V_{IN}/R$ . Ideally all of this current flows into the capacitor and none into the op amp input.

### IDEAL INTEGRATOR/LOW-PASS FILTER



Bias current is always present in a real op amp and it goes to charge the capacitor, causing the output to move in the absence of an input signal. This output voltage will appear as a dc output drift with respect to time, and is equal to  $(-I_B/C)$  volts/second. As an example of the relative magnitude of this drift an amplifier with 100nA bias current used in an integrator with 1000pF integrating capacitor has an error due to bias current charging of 100 volts/second. This means that the amplifier will saturate shortly after power is applied and the integrator function will be lost.

### INTEGRATOR WITH BIAS CURRENT



$$\frac{dV_{OUT}}{dt} = \frac{I_{BIAS}}{C} \frac{V}{SEC}$$

$$\text{FOR } C = 1000\text{pF AND } I_{BIAS} = 100\text{nA}$$

$$\frac{dV_{OUT}}{dt} = 100 \frac{V}{SEC} !$$

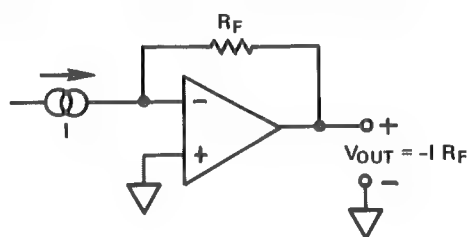
While this is a simple case it does illustrate that dc parameters of op amps can have a significant impact on active filter circuit performance. To select an op amp for a filter application assume that it is ideal and select appropriate pole and zero locations for the desired response characteristics. Once the capacitor and resistor values have been selected, determine the effect of offset and other dc parameters. Keep in mind that even in ac coupled stages large dc offset gains can cause large dc offsets, which cause clipping or saturation.

### Current-to-Voltage Converters

Some transducers produce an output voltage, others an output current. Current transducers include photodiodes, some temperature sensors and a variety of biological probes. Often the currents produced are very small—of the order of nanoamps or less. Such currents require amplification before they can be used in a system and the first stage of such amplification is usually a current/voltage converter.

While a resistor is a genuine current-to-voltage converter it is generally impractical to force the current directly through a resistor and measure the voltage produced since most current sources have a limited range of compliance voltage. A better technique for converting transducer currents to voltages uses an op amp and a feedback resistor. The input current source drives a constant terminal voltage (zero volts) and the current flows through the resistor to the op amp output. The output voltage is equal to the input current times the feedback resistor.

### CURRENT-TO-VOLTAGE CONVERTER



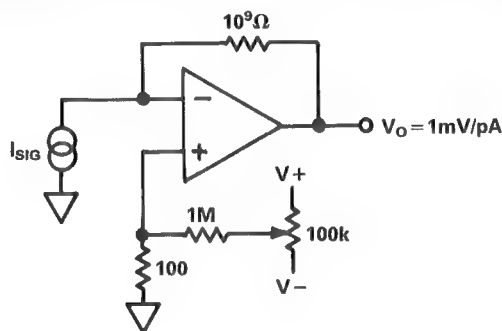
The amplifier input bias current will clearly cause an error so amplifiers chosen for this application have very low bias currents and are generally FET input types. The lowest available bias current is 60fA at room temperature from the monolithic AD549.

### AD549 FEATURES

Ultra Low Bias Current	60pA max
Low Offset Voltage	250 $\mu$ V
Low Offset Drift	5 $\mu$ V/ $^{\circ}$ C
Low Noise	4 $\mu$ V p-p (0.1Hz – 10Hz)
Low Power	700 $\mu$ A Supply Current

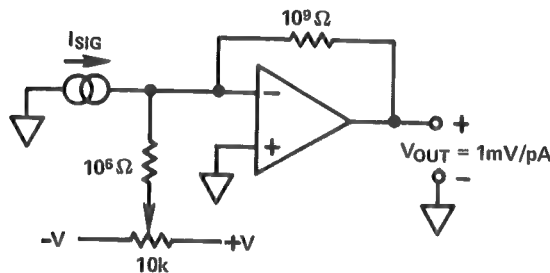
The best way to minimize the offset voltage of current/voltage converters is to use the offset null terminals provided by the manufacturer. Dual op amps, however, tend not to have offset null terminals and other techniques must be used. The correct method is to apply a correction voltage to the noninverting input.

### THE CORRECT WAY TO NULL THE OFFSET OF A I/V CONVERTER WITHOUT OFFSET TRIM TERMINALS



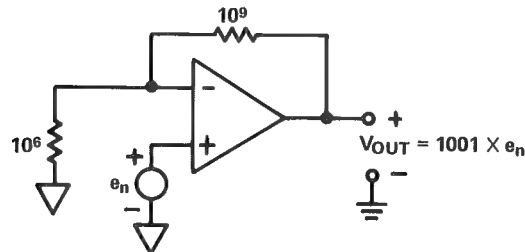
If offset null is applied to the inverting input the noise and drift performance will be drastically degraded. Consider the circuit which might be used—a potentiometer connected to a high value resistor is used to inject a correction current into the summing junction of the amplifier.

### NULLING OFFSETS IN CURRENT-TO-VOLTAGE CONVERTER (WRONG WAY)



If we draw the equivalent circuit we see that we have a noise/offset gain of 1001 because of the high ratio of feedback to injection resistors. The circuit is obviously unsatisfactory.

### EQUIVALENT CIRCUIT FOR NULLED I/V CONVERTER



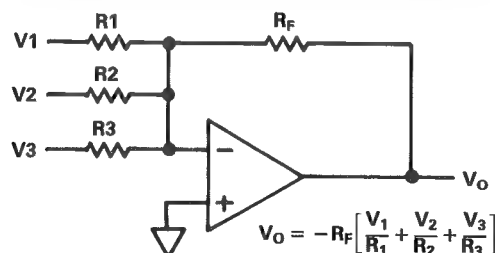
### APPLICATIONS

There are innumerable ways in which operational and transimpedance amplifiers may be used in practical applications and whole books have been written on the subject. This section of our seminar is not exhaustive but discusses a number of amplifier applications which will probably be useful in themselves and which will certainly be useful in demonstrating the philosophy behind amplifier applications.

#### Inverting Amplifier

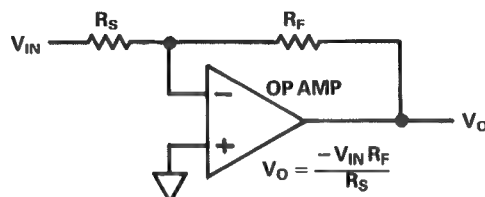
Operational amplifiers were originally intended for use as inverting amplifiers and they are probably more often used in this mode than in any other since it is so flexible. In this mode negative feedback acts to maintain the inverting input at the same potential as the noninverting input. A point which is not ground but is maintained at low impedance ground potential by negative feedback in this way is known as a “virtual ground” or “virtual earth”. The inverting input is therefore a low impedance summing point. If a number of resistors are connected to it and a signal applied to each the signals will be summed without interacting. Furthermore, the scaling factor applied to each signal will depend only upon the resistor through which it is connected to the summing junction.

### OPERATIONAL AMPLIFIER USED AS A SUMMING AMPLIFIER



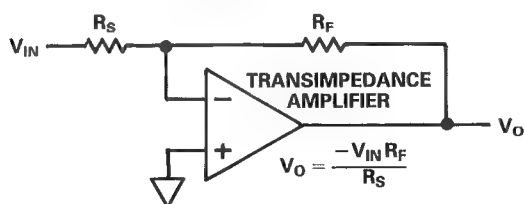
This is a special case of a simple inverting amplifier.

## SIMPLE INVERTING AMPLIFIER



The above circuits use an operational amplifier as the active element. Transimpedance amplifiers have several characteristics that make them particularly suitable for use in inverting amplifiers. One is their high slew rate and the other is their feature of maintaining constant bandwidth as their closed loop gain is varied. The constant bandwidth is achieved only if the closed loop gain is adjusted by varying the input resistance,  $R_S$ , while holding the feedback resistance,  $R_F$ , constant.

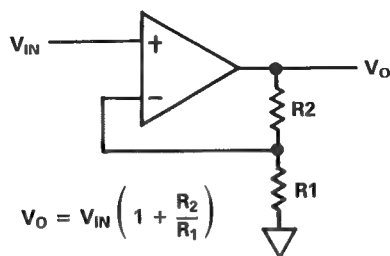
## INVERTING AMPLIFIER USING A TRANSIMPEDANCE AMPLIFIER



### Noninverting Amplifier

The noninverting amplifier configuration offers several advantages over the inverting amplifier configuration but also certain drawbacks. The major advantage of the noninverting mode is its high input impedance—the common-mode impedance of the op amp being used. Despite the high impedance of such an input the bias current of the amplifier must still be allowed for—it should be modelled as a current source feeding the input terminal.

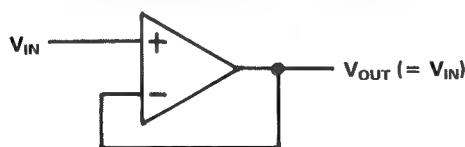
## NONINVERTING AMPLIFIER



The high input impedance of a noninverting stage offers minimum circuit loading at a cost of lowered noise immunity. Amplifiers with high input impedance are much more sensitive to E-field noise (electrostatic pickup) and must be guarded against it by attention to circuit layout and shielding.

One of the most common noninverting amplifiers is the unity gain “voltage follower”. It consists of an internally compensated op amp with its output connected directly to its inverting input and uses no other components. It has a very high input impedance (don’t forget the bias current!) and a very low output impedance and is widely used to buffer signals from high source impedances to low load impedances.

## OPERATIONAL AMPLIFIER USED AS A VOLTAGE FOLLOWER

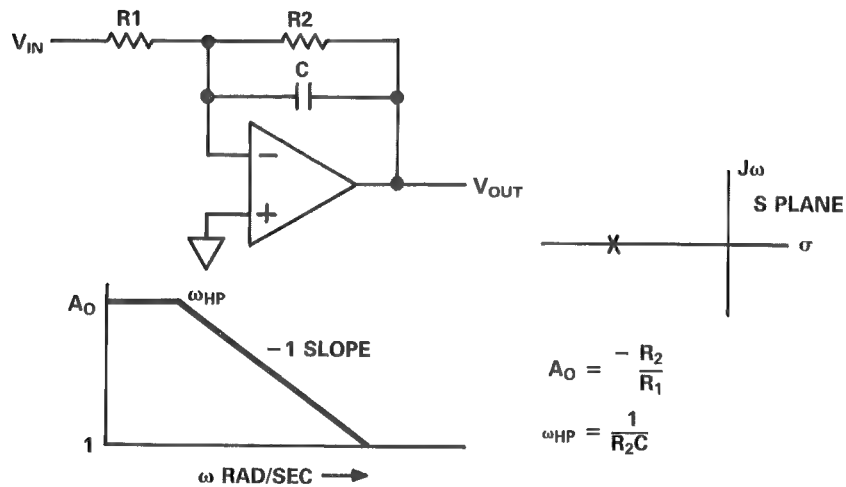




### Basic Low Pass Filter

The low pass filter is the most simple one of all. It consists of an inverting amplifier with a capacitor in parallel with its feedback resistor. As the frequency increases the capacitive reactance decreases—hence the gain decreases.

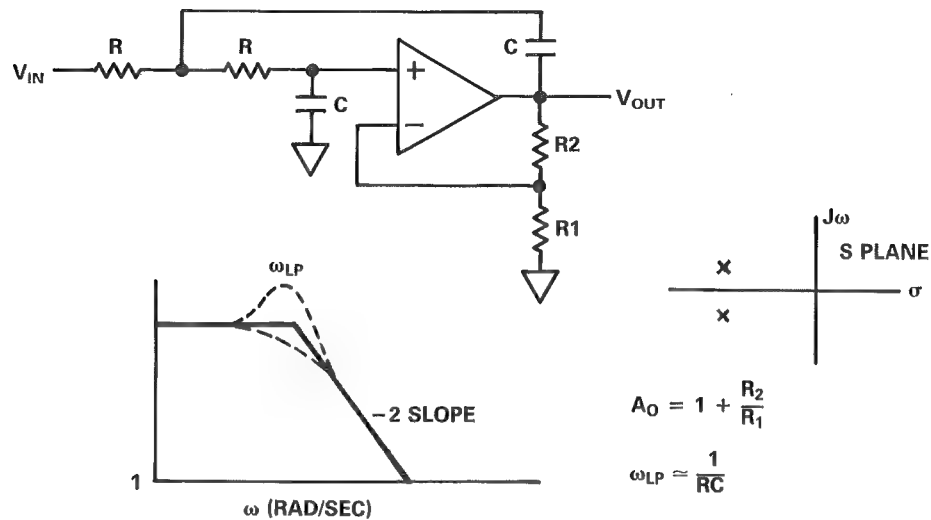
### BASIC LOW PASS FILTER



The cutoff frequency,  $\omega_{HP}$ , is simply  $1/(R_2 C)$  and the rolloff is 6dB/octave (20dB/decade). The noise is a factor of  $\pi/2$  more than would be encountered if the filter skirt were infinitely steep.

Another low pass filter is the Sallen and Key. This two capacitor filter is easily implemented, as the component selection is not critical and a high performance filter is readily synthesized.

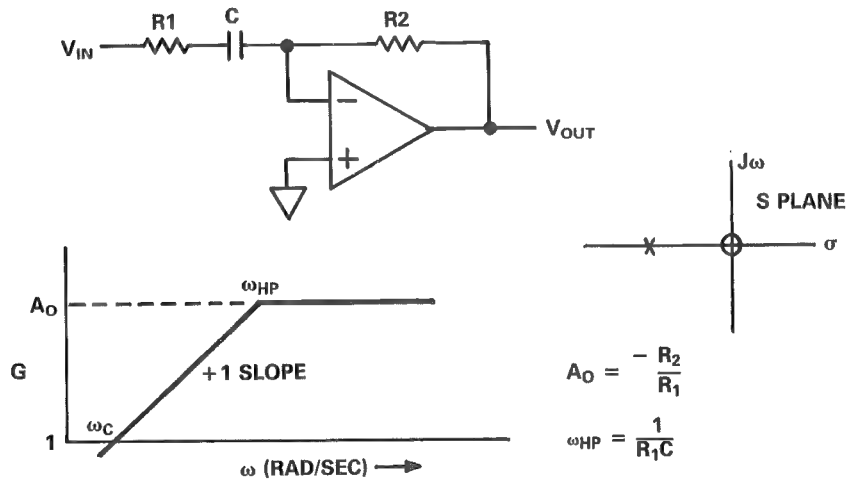
### SALLEN AND KEY LOW PASS FILTER (2 POLE)



### Basic High Pass Filter

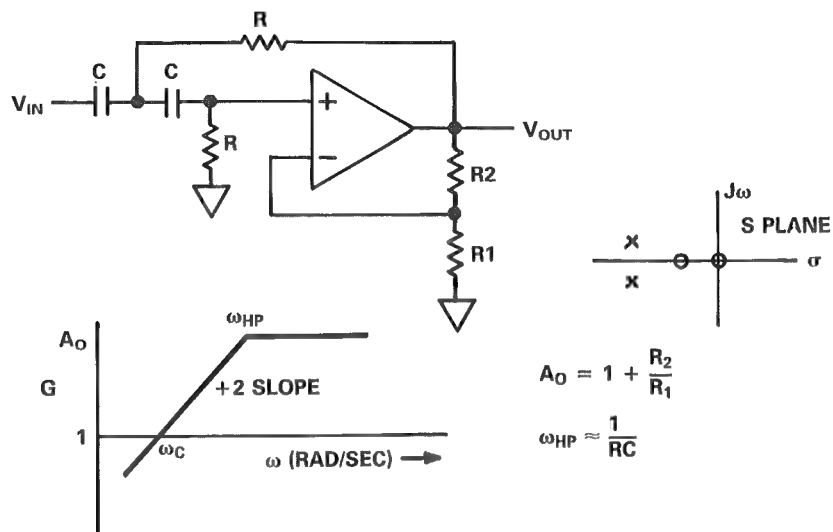
The basic high pass filter uses a capacitor as an input element. The gain increases with frequency until it is limited by the series resistor  $R_1$ . The high frequency gain therefore flattens out at a value of  $R_2/R_1$ . This response shows both a pole and a zero. If the high frequency gain were not limited by  $R_1$  and  $R_2/R_1$  the system would probably oscillate.

### BASIC HIGH PASS FILTER



The Sallen and Key structure can also be used to produce a high pass filter. Like the low pass design the component selection is straight forward. Note the zero at the origin, the zero on the real axis and the pair of conjugate poles.

### SALLEN AND KEY 2-POLE HIGH PASS FILTER

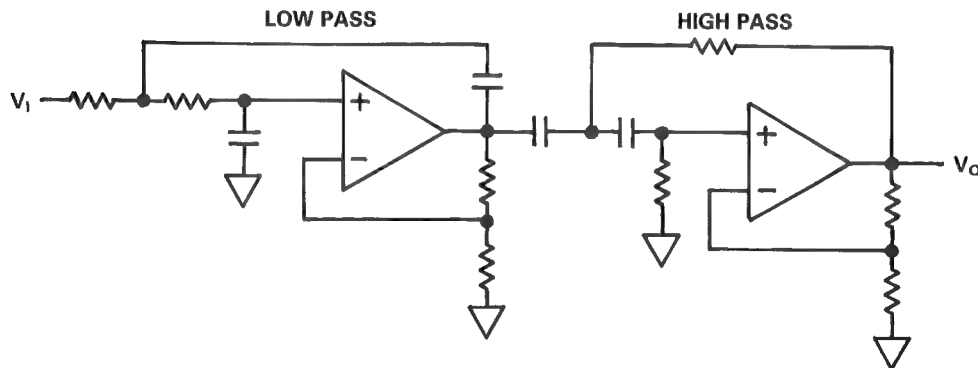


### Band Pass Filters

The simplest bandpass filter consists of cascaded high pass and low pass filters. Where quick and predictable results are required there is a great deal to recommend this approach since the upper and lower cutoff characteristics may be manipulated separately.

Integrated bandpass filters where a single amplifier functions in both high pass and low pass modes are considerably more demanding to design and frequently require very inconvenient (and very accurately defined) component values. For details on the design of active filters consult "Electronic Filter Design Handbook".

## BAND-PASS FILTER USING LOW PASS AND HIGH PASS SALLEN AND KEY FILTERS

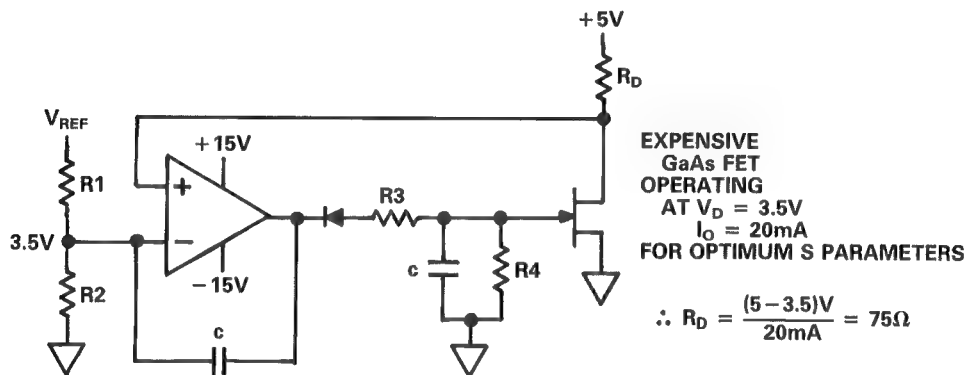


### Active Bias Networks

An op amp active bias network is a handy means of reliably establishing precise voltage and current bias conditions for an external component. Consider the following example.

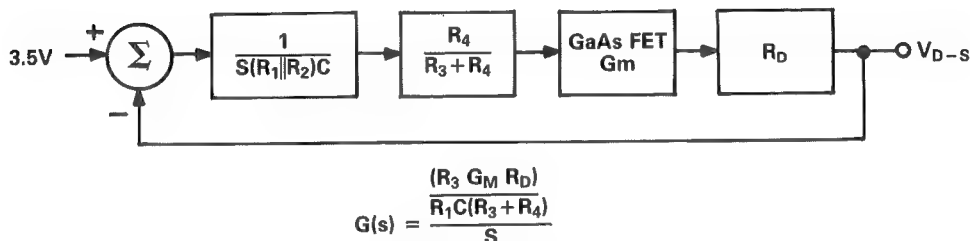
Gallium arsenide field effect transistors (GaAsFETs) are used in amplifiers at microwave frequencies and their high frequency performance is usually specified with S-parameters—which are merely voltage reflection coefficients measured in a  $50\Omega$  system. The S-parameters of a GaAsFET are measured at a specific dc bias and if the bias conditions change the amplifier performance will suffer. It is thus necessary to ensure that the bias conditions remain constant over the required environmental temperature range. This is done with an active bias network.

## ACTIVE BIAS CIRCUIT FOR UHF AMPLIFIER (ALL RF COMPONENTS OMITTED FOR CLARITY)



The operational amplifier contains an integrator to establish a predictable unity gain crossover frequency. The voltage divider limits the maximum voltage that can be applied to the gate of the GaAsFET and the diode prevents a positive voltage from being applied to the gate (designers should always assume that supply voltages may be applied to a network in random order and should design their circuit so that it will tolerate this).

## CONTROL SYSTEM MODEL OF ACTIVE BIAS NETWORK

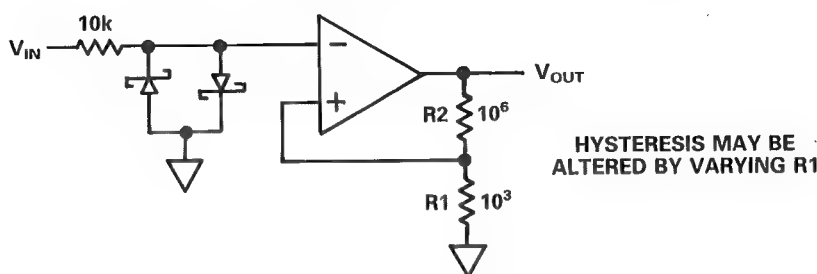


In this application the critical items are the stability of the reference voltage (as this establishes the drain to source voltage) and the +5V supply, and the value of the drain resistor (which sets the drain current). Almost any operational amplifier can be used in this application.

### Comparators

Operational amplifiers make perfectly adequate comparators in applications where high speed is not essential. Dedicated comparators frequently have an open collector output for convenient logic interface but in many cases the output stage of an op amp will work as well as necessary—and the op amp will probably be less expensive. If hysteresis is required to minimize noise or oscillation in the transition region it may be provided with two resistors. The circuit shown is an example of an op amp used as a comparator in a zero crossing detector. The design incorporates hysteresis and a diode clamp. This type of circuit is often used to produce a square wave or to clean up a noisy signal.

## OPERATIONAL AMPLIFIER USED AS A ZERO CROSSING COMPARATOR

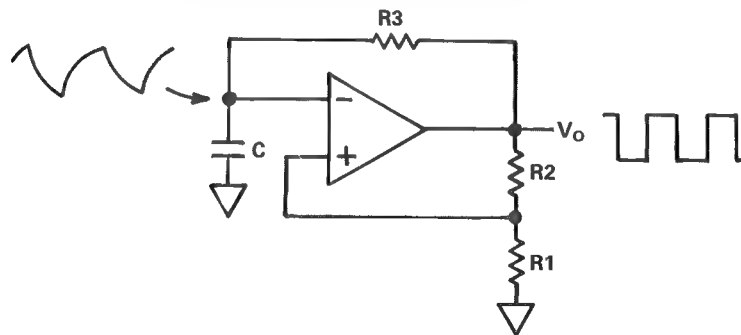


## Oscillators

The subject of oscillators is so large that it is impractical to cover it in a seminar of this type. It is important, however, to realize that operational amplifiers are used as gain blocks in oscillators of many different types and that the same care should be devoted to the choice of op amp for oscillator use as for any other application. It is undoubtedly true that with sufficient positive feedback any circuit can be made to oscillate but problems of bias current, noise, phase shift and slew rate will affect the quality of an oscillator's performance just as they would affect any other op amp application. The basic principle of design is to design a system assuming a perfect op amp and then analyze the effects of those parameters likely to affect its operation.

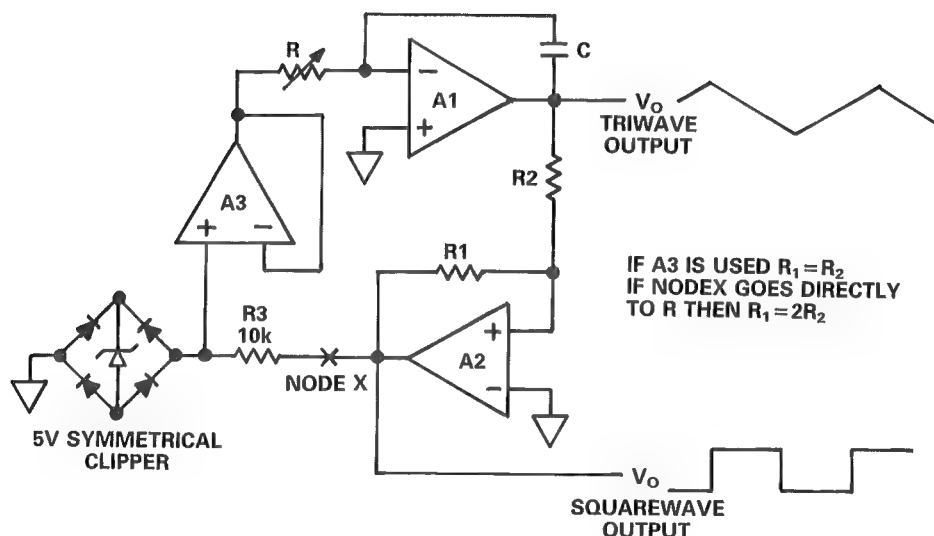
In a relaxation oscillator using an op amp and just three resistors and a capacitor the parameters which affect operation are its output levels (how much "headroom" does the output stage have?) and bias current. The headroom will affect the frequency of oscillation while the bias current will affect the mark:space ratio of the (nominally) square output waveform as well as having a second-order effect on oscillation frequency.

## OPERATIONAL AMPLIFIER RELAXATION OSCILLATOR



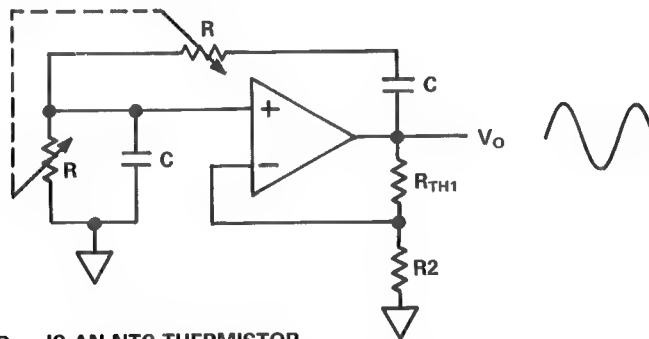
Another oscillator which can be classified as a relaxation oscillator is a triangular wave oscillator using two or three op amps (the third, the unity gain buffer between the clipper and the integrator input, is not essential but improves performance). The frequency is set by the values of R and C and the amplitude of both the square and tri-wave outputs by the bipolar clipping circuit made with a zener diode and a diode bridge. If amplifier A2 limits symmetrically the circuit may be simplified by connecting the node X directly to A2 output and omitting the clipper, A3 and R3—in this case R2 must be smaller than R1 and the amplitude of the triwave will be smaller than that of the square wave.

## TRIWAVE OSCILLATOR



No work on op amp oscillators would be complete without a Wien bridge circuit. The Wien bridge contains two equal resistors and two equal capacitors has an attenuation of 3 at zero phase shift. (No bridge that I ever saw in Vienna looks anything like it.) If it is used in a positive feedback loop the circuit will oscillate at this zero phase frequency. The amplifier used in a Wien bridge oscillator must have gain at least 3. The gain is exactly 3 the circuit will take forever to start oscillating, if it is much more than three the amplitude of oscillations will increase until the amplifier limits and the sine wave output becomes distorted. Wien bridge oscillators therefore contain agc circuitry to stabilize their output level at some preset value.

## WIEN BRIDGE OSCILLATOR



$R_{TH1}$  IS AN NTC THERMISTOR  
 AT AMBIENT TEMPERATURE  $R_{TH1} \geq 4R_2$   
 WHEN  $V(rms)_{TH1} = (.66 \text{ WANTED } V_O)$  THEN  $R_{TH1}$  SHOULD BE  $2R_2$



# **SPECIAL PURPOSE AMPLIFIERS**





# **SPECIAL PURPOSE AMPLIFIERS**

- 1. Why Special Purpose Amplifiers?**
- 2. Limitations of Op Amps**
- 3. Instrumentation Amplifiers**
  - Characteristics**
  - Design Techniques**
  - Applications**
- 4. Single-Ended SPGA**
- 5. Isolation Amplifiers**
  - When to Use Isolation Amplifiers**
- 6. Transducers**
  - Types**
  - Characteristics**
  - Interfacing**
- 7. Specialized Signal Conditioning Circuits**



## 1. WHY SPECIAL PURPOSE AMPLIFIERS?

When working in the *real* world one must accept the fact that there will be deviations from the ideal. Zero output impedances and convenient output ranges are not characteristics of most practical transducers. Also included in the real world are environmental conditions which may complicate the process of acquisition.

In real world data acquisition the most simple scenario consists of a transducer which is connected directly to a data processing system. In most cases some amplification is required and under ideal conditions can be provided by a simple op-amp and a couple of resistors. However, electrical interference, voltage drops caused by current through the resistance of leads from remote locations, nonlinear transducers, requirements for galvanic isolation and fluctuating temperatures will often complicate the task of providing accurate amplification.

In this section we will discuss various means of signal conditioning in an environment hostile to precision measurements. Instrumentation amplifiers will often serve those applications where isolation is not required and where extremely high common-mode voltages are not encountered. Isolation amplifiers are intended for use under those latter conditions. We will also discuss some highly specialized signal conditioning circuits which simplify circuit design in specific applications.

## WHY SPECIAL PURPOSE AMPLIFIERS ARE REQUIRED

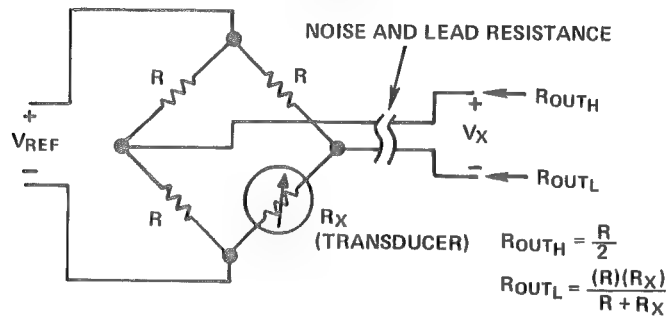
- 1) Inconvenient Transducer Output Characteristics
  - Format of Output (Capacitance, Resistance, Current, Voltage, etc)
  - High Output Impedances
  - Inconvenient Voltage Ranges
  - Unbalanced Outputs
- 2) Hostile Environmental Conditions
  - Noise
  - High CMV
  - Remote Locations
  - Temperature Variances
- 3) Requirements for Isolation
  - Safety
  - Protection for Circuitry
  - Ground Loops

## 2. LIMITATIONS OF OPERATIONAL AMPLIFIERS

IC operational amplifiers are without a doubt the most widely used analog building block in the electronics industry. Op amps are available with a wide variety of performance features at costs that are low for general purpose devices and slightly higher for devices which exhibit increased precision and/or speed. Reasons for op amp popularity are its extreme versatility (it can be configured to do more than simple amplification) and the fact that every analog circuit designer has at least a working knowledge of op amp techniques. However, in less than ideal situations, op amps have several serious shortcomings.

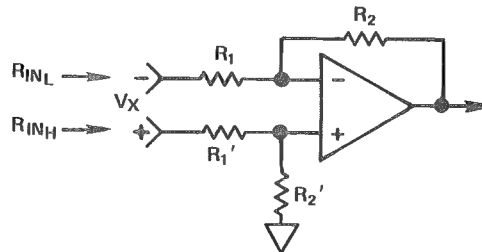
Practical transducer applications usually involve differential connections, nonzero source impedances and noise. A typical transducer bridge application is illustrated below:

### PRACTICAL TRANSDUCER CIRCUIT WITH DIFFERENTIAL OUTPUT



It can be seen that the output impedance of the above circuit is nonzero, unbalanced and varies with the parameter being measured. Also, lead resistance and noise pickup cannot be totally avoided. Due to the nature of the output, a differential amplifier is required, but a single op amp in a differential configuration is not well suited to such nonideal applications as shown below.

### OP AMP IN DIFFERENTIAL CONNECTION



- Low Input Impedance
- Common Mode Rejection Depends on Resistor Ratio-Matching

To achieve balanced gain,  $G = (R_2/R_1) = (R_2'/R_1')$

For balanced input impedance,  $R_1' + R_2' = R_1$

To provide balanced impedance return paths for amplifier bias currents (to minimize offset voltage drift),

$$R_1 R_2 / (R_1 + R_2) = R_1' R_2' / (R_1' + R_2')$$

Furthermore, these mutually exclusive conditions are only valid for ideal transducers. Finite input impedances, even if balanced, can disturb unbalanced transducers with lead resistances further aggravating the situation.

Common-mode rejection for most op amps is typically between 60dB and 90dB (some types, like the AD517 and AD OP-07, may have up to 110dB). This may not be sufficient to reject common-mode noise.

Also, op amps do not exhibit galvanic isolation between input and output. They cannot handle signals superimposed upon common-mode voltages in excess of  $\pm 10$  volts and if the common-mode input voltage exceeds the supply voltage, they may be destroyed.

### 3. INSTRUMENTATION AMPLIFIERS

An instrumentation amplifier (IA) is a precision differential voltage amplifier that is intended for use when acquisition of a useful signal is difficult. As was stated earlier, real world signals from practical transducers are often plagued by problems such as noise, unbalanced output impedances, etc. IA's are designed to solve these signal acquisition problems. IA's have stable gain, high input impedances, low bias currents, high common-mode rejection and balanced differential inputs. Gain is normally determined via pin strapping, or a user-selectable resistor or resistor pair, and can be programmed in the range of 1 to 10,000. All other necessary precision components are internal which allows the manufacturer to guarantee a specified level of performance. The output is single ended, usually with sense and reference terminals.

## INSTRUMENTATION AMPLIFIER CHARACTERISTICS

- |   |   |
|---|---|
| 1) Fixed, Stable Gain Determined by User-Selectable Resistor, Resistor Pair, or Pin Strapping (Internal Resistors)<br>2) High Input Impedance<br>3) Low Bias Currents | 4) High Common-Mode Rejection<br>5) Balanced Differential Inputs<br>6) Stable, Well Characterized Specs<br>7) Single-Ended Output |
|---|---|

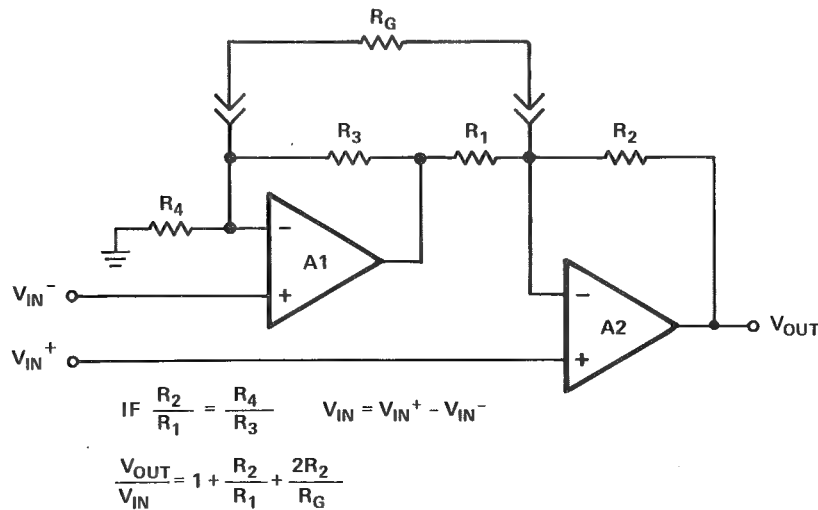
The performance of an IA, like that of an op amp, is described by its specifications. Unlike op amps, however, IA's do not have as wide a variety of performance levels. This is because IA's themselves are a specialized class of amplifier.

### DESIGN TECHNIQUES

IA configurations are based on op amps. We have already analyzed the simplest design, using a single op amp, and found that it lacks the performance required for precision applications.

An IA can be designed using two amplifiers which overcomes some of the weaknesses exhibited by a single amplifier.

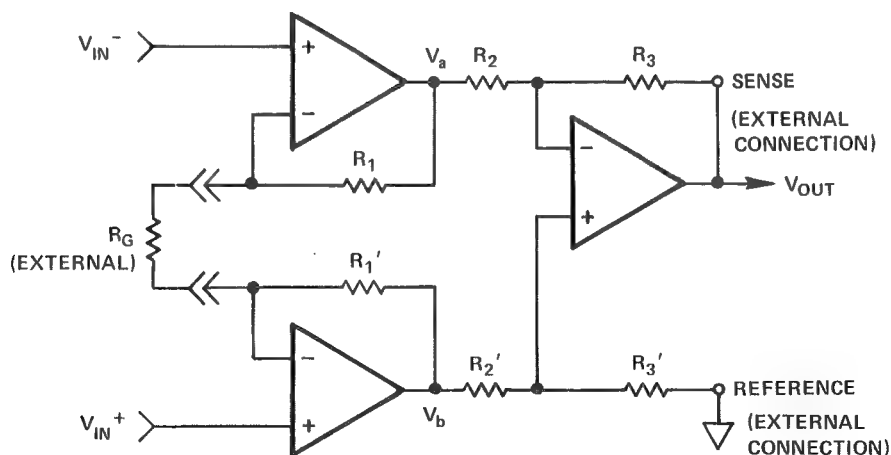
### "TWO-AMPLIFIER" INSTRUMENTATION AMPLIFIER



The input impedance of this circuit is high, permitting the signal sources to have high and unbalanced output impedance. The major disadvantage of this design is that the common-mode voltage input range must be traded off against gain range. The amplifier A1 must amplify a common-mode signal by  $(R_3 + R_4)/R_4$ . If  $R_3 > R_4$ , saturation of A1 will occur if the common-mode signal is too high leaving no headroom to amplify the differential signal of interest and if  $R_3 < R_4$ , low gains cannot be realized.

The most popular configuration for op amp based instrumentation amplifiers is shown below.

### "CLASSIC" 3 OP AMP INSTRUMENTATION AMPLIFIER



The transfer function of this circuit is:

$$V_{OUT} = ((+V_{IN}) - (-V_{IN}))(2R1/RG + 1)(R3/R2)$$

where  $R1 = R1'$ ,  $R2 = R2'$ , and  $R3 = R3'$

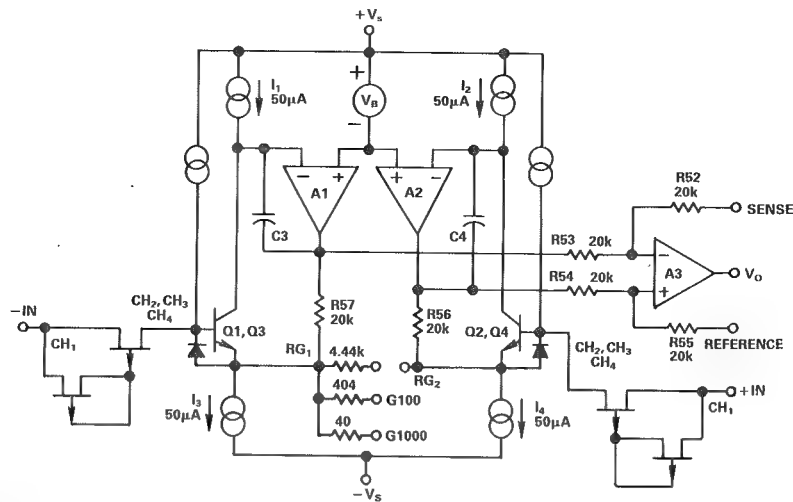
In this configuration, gain accuracy and CMR depend upon the ratio matching of  $R2$ ,  $R2'$ , and  $R3$  and  $R3'$ . Circuit analysis shows, however, that CMR does not depend on the matching of  $R1$  and  $R1'$ .

Within limits, the user may take as much gain in the front end as he wishes (set by the value  $R_G$ ) without increasing the common-mode error signal. Thus, CMR will theoretically increase in direct proportion to gain. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain (no common-mode voltage will appear across  $R_G$ , hence, no common-mode current will flow in it because the input terminals of an op amp operating normally will have no significant potential difference between them). This means that the large common-mode signals (within the op amp limits) may be handled independent of gain.

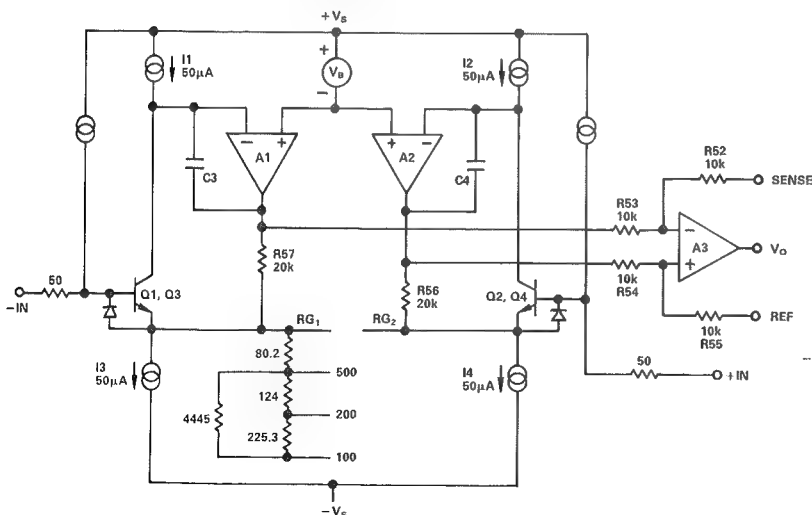
Finally, because of the symmetry of this configuration, first order common-mode error sources in the input amplifiers, if they track, tend to be cancelled out by the output stage subtractor. IA's of this type include the AD524, AD624 and AD625. They are characterized by extremely high precision. The input amplifiers may be either FET or Bipolar. FET input op amps have very low bias currents and are well suited for use with very high source impedances, but generally have poorer CMR than bipolar amplifiers because nongeometry-related mismatches usually cause larger input offset voltage drifts.

The AD524, AD624 and AD625 are monolithic instrumentation amplifiers based on the classic 3 op amp circuit. The advantage of monolithic fabrication is that the closely matched components required to construct the preamplifier are easily fabricated on a single chip. The preamplifier section develops the programmed gain by the use of feedback. The gain is programmed by varying the value of  $R_G$  (smaller values increase the gain). Feedback forces the collector currents of  $Q1$ ,  $Q2$ ,  $Q3$  and  $Q4$  to be constant which impresses the input voltages across  $R_G$ .

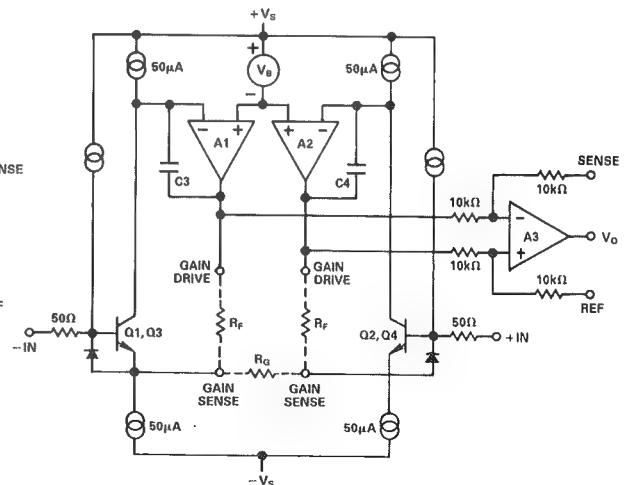
**AD524 SIMPLIFIED SCHEMATIC**



**AD624 SIMPLIFIED SCHEMATIC**



**AD625 SIMPLIFIED SCHEMATIC**



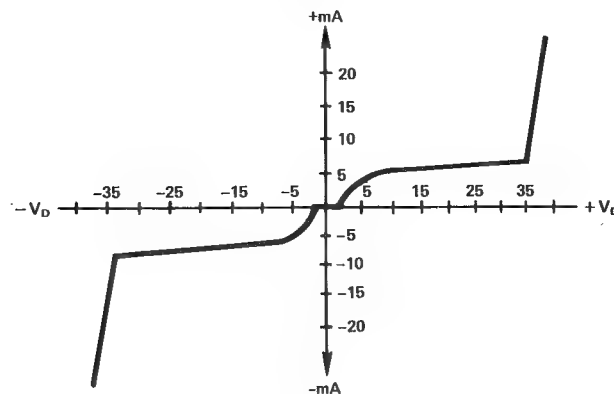
As  $R_G$  is reduced, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of  $3 \times 10^8$  at a programmed gain of 1000, reducing gain related errors to a negligible 30ppm. Second, the gain bandwidth product which is determined by  $C_3$ ,  $C_4$  and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the current of the input transistors for an RTI noise of  $4\text{nV}/\sqrt{\text{Hz}}$ , at  $G=1000$ .

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of  $R_G$  will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit the current to below 5mA with a full differential overload (36V) would require over  $7\text{k}\Omega$  of resistance which would add  $10\text{nV}/\sqrt{\text{Hz}}$  of noise. To provide both input protection and low noise the AD524 utilizes a special series protection FET.

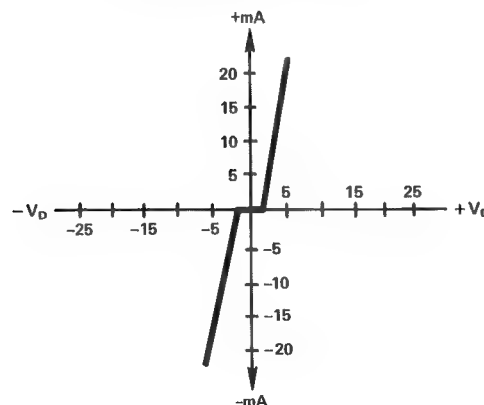
This unique FET design was used to provide a bidirectional current limit, protecting against both positive and negative overload conditions. Under nonoverloaded conditions, three channels  $\text{CH}_2$ ,  $\text{CH}_3$  and  $\text{CH}_4$  act as a resistance ( $1\text{k}\Omega$ ) in series with the inputs as before. During an overload in the positive direction, a fourth channel,  $\text{CH}_1$ , acts as a small resistance ( $3\text{k}\Omega$ ) in series with the gate, which draws only the leakage current, and the FET limits to  $I_{\text{DSS}}$ . When the FET enhances under a negative overload, the gate current must go through the small FET formed by  $\text{CH}_1$  and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range with power on or power off.

For applications where input overload is not expected, the AD624 and AD625 replace the protection FETs with  $50\Omega$  resistors. This reduces the input voltage noise to  $4\text{nV}/\sqrt{\text{Hz}}$  while limiting input current to 10mA with a 2.5V differential input overload.

### AD524 INPUT PROTECTION CHARACTERISTIC



### AD624 INPUT PROTECTION CHARACTERISTIC



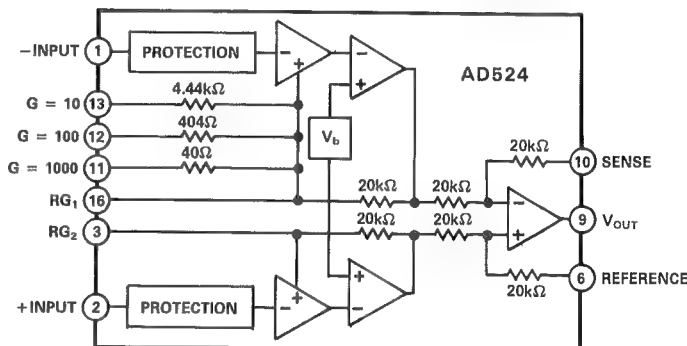


The AD524 and AD624 are high precision monolithic instrumentation amplifiers designed for data acquisition applications requiring high accuracy. As previously stated, the AD524 is fully protected from overloads with power on or off, making it suitable for operation under worst case conditions. The AD624 has been optimized for use with low level transducers, including load cells, strain gages and pressure transducers. Its combination of high linearity and low noise make the AD624 ideal for use in high resolution data acquisition systems.

## AD524 FEATURES

Low Nonlinearity: 0.003% ( $G = 1$ )  
 High CMRR: 120dB ( $G = 1000$ )  
 Low Offset Voltage:  $50\mu\text{V}$   
 Low Offset Voltage Drift:  $0.5\mu\text{V}/^\circ\text{C}$   
 Gain Bandwidth Product: 25MHz  
 Pin Programmable Gains of 1, 10, 100, 1000  
 Complete Input Protection Power On – Power Off  
 No External Components Required  
 Low Noise:  $0.3\mu\text{V p-p}$  (0.1Hz to 10Hz)

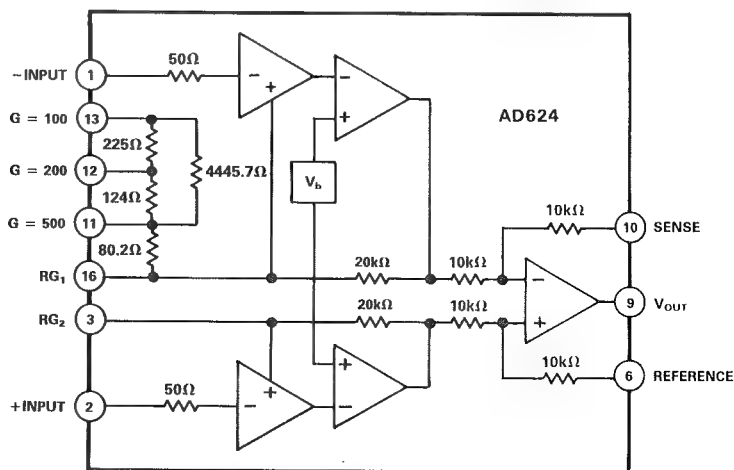
## AD524 FUNCTIONAL BLOCK DIAGRAM



## AD624 FEATURES

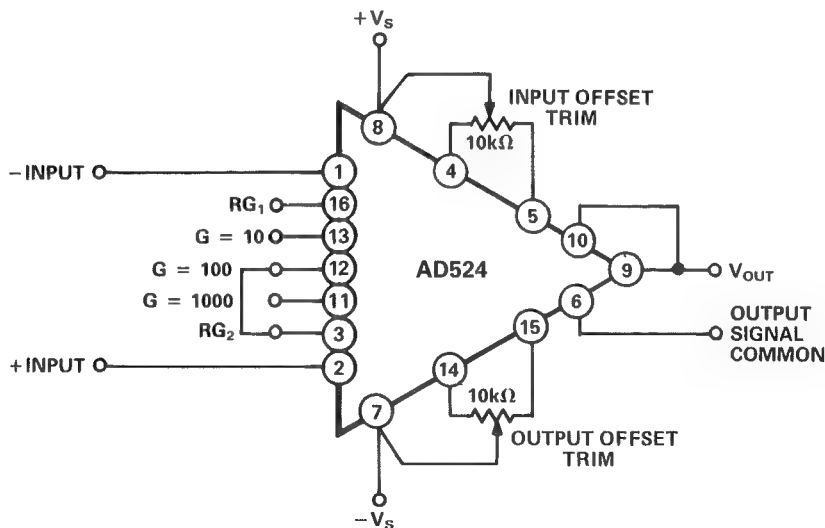
Low Nonlinearity: 0.001% ( $G = 1$ )  
 High CMRR: 115dB ( $G = 500$ )  
 Low Offset Voltage:  $25\mu\text{V}$   
 Low Offset Voltage Drift:  $0.25\mu\text{V}/^\circ\text{C}$   
 Gain Bandwidth Product: 25MHz  
 Pin Programmable Gains of 1, 100, 200, 500, 1000,  
 and More  
 No External Components Required  
 Internally Compensated  
 Low Noise:  $0.2\mu\text{V p-p}$  (0.1Hz to 10Hz)

## AD624 FUNCTIONAL BLOCK DIAGRAM



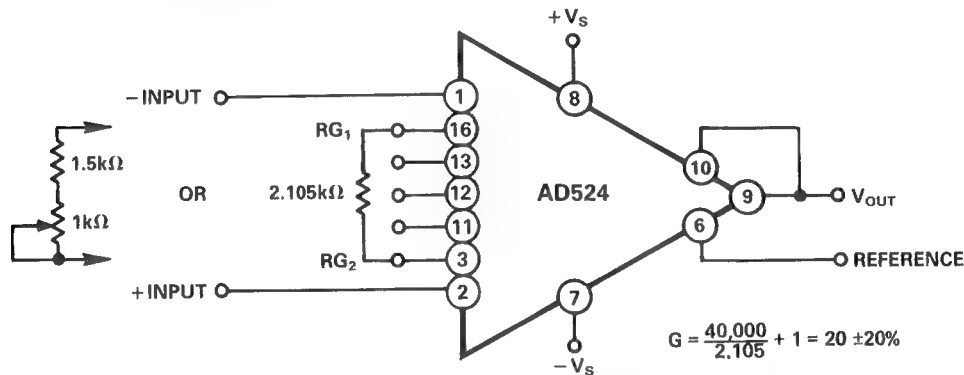
The AD524 and AD624 have internal high accuracy pretrimmed resistors for pin programmable gain setting (1, 10, 100 and 1000 for the AD524; 1, 100, 200, 500 and 1000 for the AD624). One of the present gains can be selected by pin strapping the appropriate gain terminal to  $RG_2$ .

## OPERATING CONNECTIONS FOR $G = 100$



The AD524 and AD624 can be configured for other gains. An external resistor can be connected between pins 2 and 16 which programs the gain according to the formula  $G = 1 + 40k\Omega/R_G$ . The external resistor should be a precision low TC resistor. An external  $R_G$  effects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external  $R_G$  and the absolute accuracy of the internal resistors ( $\pm 20\%$ ). Gain drift is determined by the TC of  $R_G$  compared to that of the internal resistors ( $-50\text{ppm}/^\circ\text{C}$  typ).

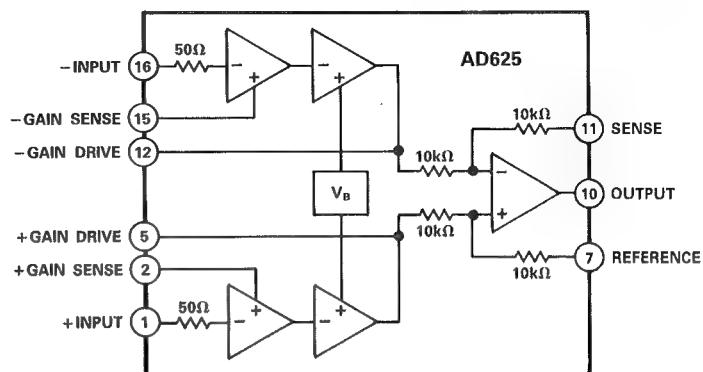
## OPERATING CONNECTIONS FOR $G = 20$



In the AD625, the appropriate circuit points have been pinned out so that the gain can be completely determined using external resistors. The absence of internal gain setting resistors alleviates the problem of gain accuracy and gain drift due to mismatch in internal/external resistors.

In the resistor-programmed mode of the AD625, only three external resistors are needed to select any gain from 1 to 10,000. Depending upon the application, discrete components or a pretrimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625 contributes less than 0.02% gain error and under  $5\text{ppm}/^\circ\text{C}$  gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors ( $R_F$ ).

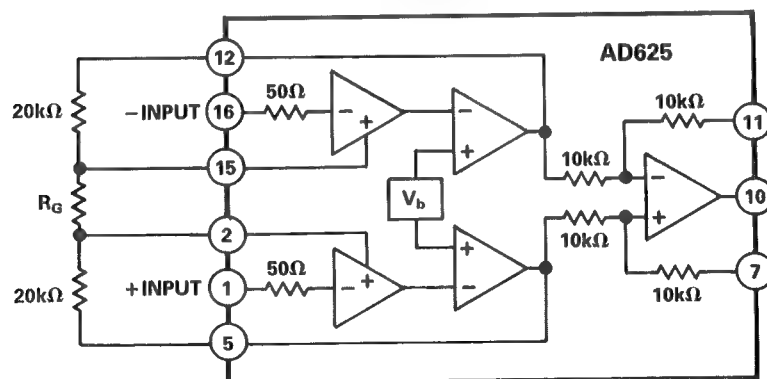
## AD625 FUNCTIONAL BLOCK DIAGRAM



## AD625 FEATURES

User Programmed Gains 1 to 10,000  
 Low Gain Error: 0.02% max  
 Low Gain T.C.:  $5\text{ppm}/^\circ\text{C}$  max  
 Low Nonlinearity: 0.001% max  
 Low Offset Voltage:  $25\mu\text{V}$   
 Low Noise:  $4\text{nV}/\text{Hz}$  (at 1kHz) RTI  
 Gain Bandwidth Product: 25MHz

## AD625 RESISTOR PROGRAMMED MODE



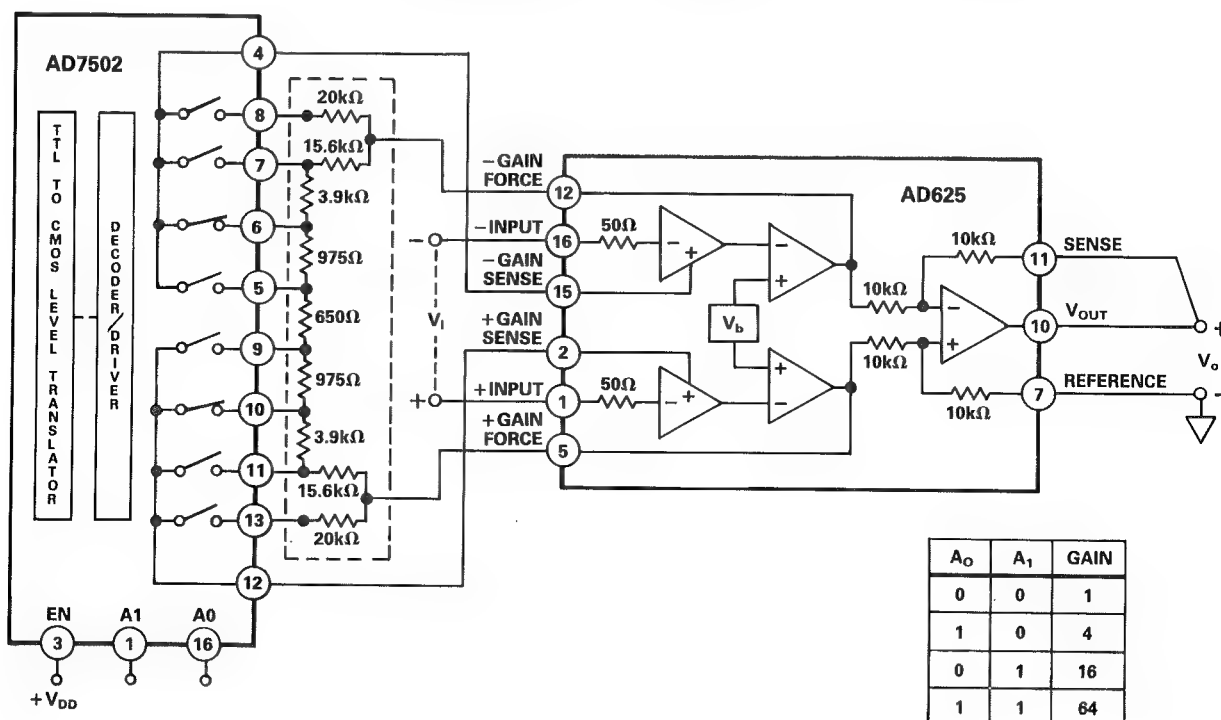
$$G = \frac{2 R_F}{R_G} + 1$$

A software programmable gain amplifier (SPGA) provides the ability to program precision gains digitally. Historically, the problem in the systems requiring electronic switching of gains has been the ON resistance of the multiplexer, which appears in series with the gain setting resistor  $R_G$ . This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain sense pins available (Pins 2, 15, 5 and 12). As a consequence, the multiplexers ON resistance is removed from the signal current path. This transforms the ON resistance error into a small, nullable offset error.

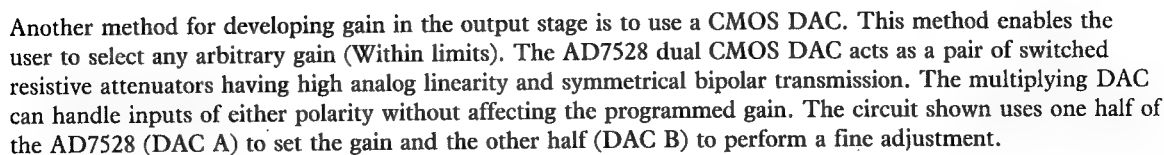
The figure below demonstrates an AD625-based SPGA with gain of 1, 4, 16 and 64.  $R_G$  is the resistance between the gain sense lines (pins 2 and 15) of the AD625. With the multiplexer in the state shown,  $R_G$  is the sum of two 975 $\Omega$  resistors and the 650 $\Omega$  resistor, or 2600 $\Omega$ .  $R_F$  is the resistance between the gain sense and the gain drive pins (pins 12 and 15, or pins 2 and 5), the 15.6k $\Omega$  resistor plus the 3.9k $\Omega$  resistor, or 19.5k $\Omega$ . The gain is therefore:

$$(2R_F/R_G) + 1 = 9(19.5k\Omega)/(2.6k\Omega) + 1 = 16$$

## SOFTWARE PROGRAMMABLE GAIN AMPLIFIER USING THE AD625



## PROGRAMMABLE OUTPUT GAIN



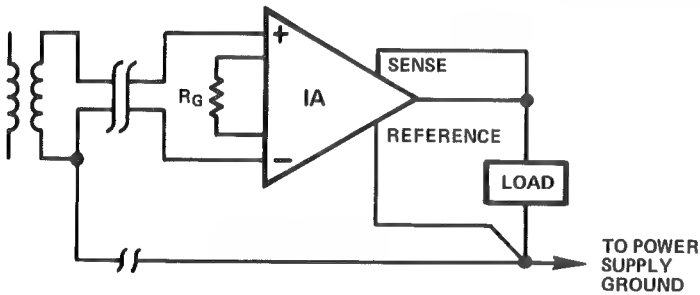
## PROGRAMMABLE OUTPUT GAIN USING A DAC



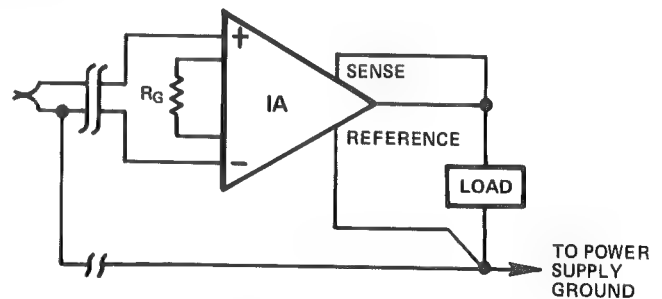
## APPLICATION NOTES

Although instrumentation amplifiers have differential inputs, the bias currents do not flow from one to the other but to the external circuit. There must, therefore, be a return path for the bias currents. If this path is not provided, those currents will not flow, causing the output of the amplifier to drift uncontrollably or to saturate. Therefore, when amplifying floating input sources such as transformers and thermocouples, as well as ac-coupled sources, there must be a dc return path from each input to ground. Suitable connections are shown below. In applications where it is impossible to provide a dc path for bias currents, an isolation amplifier is necessary.

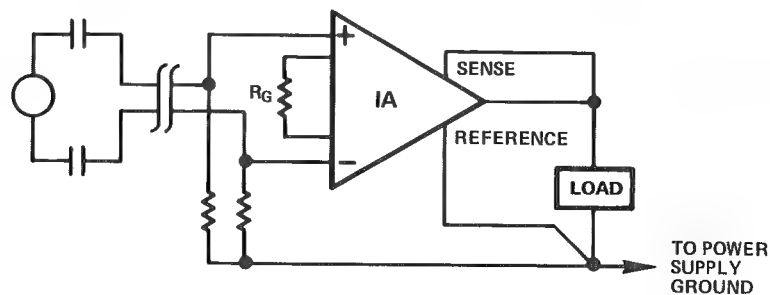
### INDIRECT GROUND RETURNS FOR BIAS CURRENTS



a). TRANSFORMER COUPLED



b). THERMOCOUPLE

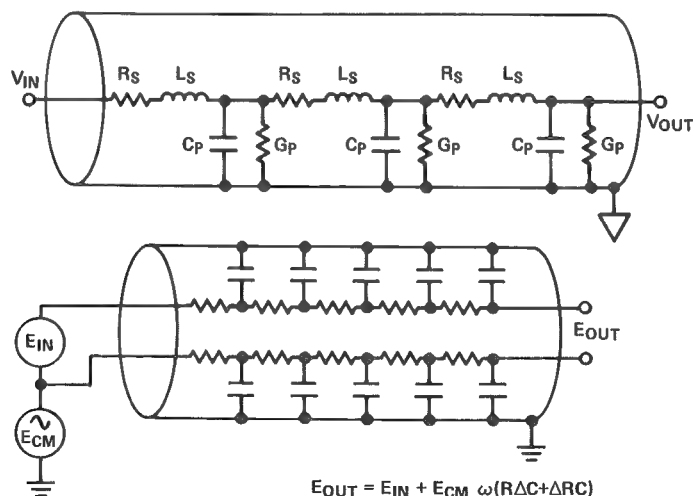


c). AC COUPLED

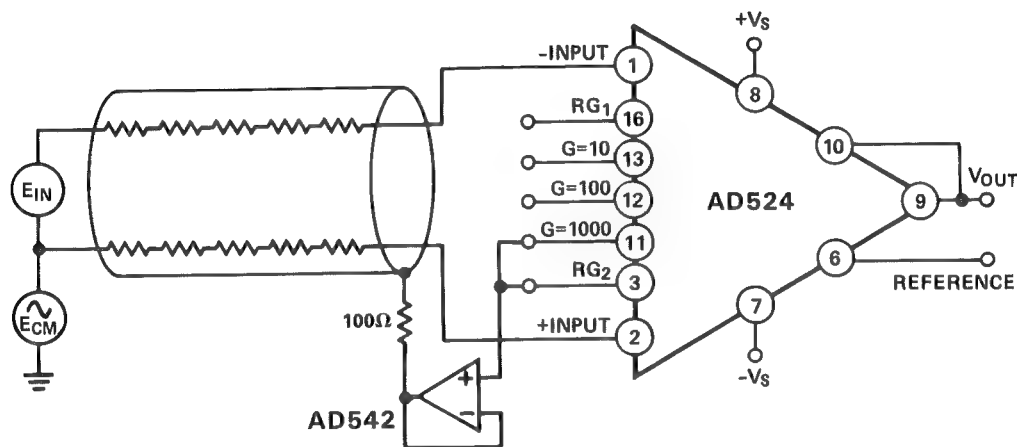
#### Data Guard

Signals from remote transducers are often transmitted to an IA through shielded cables. While this may reduce noise pickup, the distributed RCs in such cabling can cause differential phase shifts in those lines. When ac common-modes signals are present, these phase shifts will reduce common-mode rejection. If the shields are driven by the common-mode signal, the cable capacitance is "bootstrapped" thus making the capacitance effectively zero for common-mode signals.

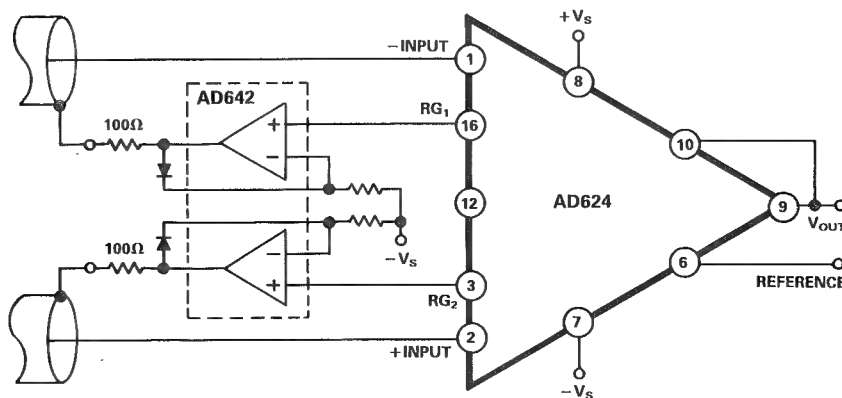
#### RG58 CABLE



IC instrumentation amplifiers do not have a buffered data guard available externally. However, the common-mode voltage for amplifiers such as the AD525, AD624 and AD625 is available at  $RG_2$  and should be buffered with an operational amplifier. The op amp should be of the FET input variety for low bias currents (AD542, AD548, etc). Low bias currents are required because bias currents flowing through the gain setting resistor will cause an offset error.



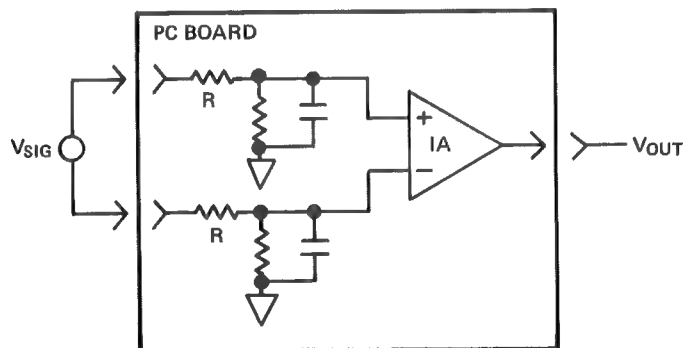
## DIFFERENTIAL SHIELD DRIVER



Most circuits today are designed on printed circuit (PC) boards. Although the benefits of PC construction include reduction in circuit size and reduced noise pickup, the ability to apply shields and guards can be even more effective in improving circuit performance.

In some circuits, wiring capacitance and leakage resistance can degrade performance. In an instrumentation amplifier, ac common-mode rejection is directly limited by differential phase shift.

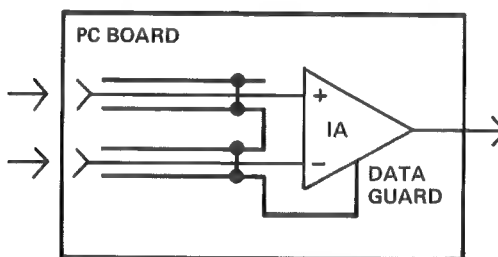
## PARASITICS IN PRINTED CIRCUITS



Unequal drops across unbalanced PC board track resistances and differential phase shift due to varied stray capacities can cause a decrease in common-mode rejection similar to the effect of long input cables.

A data guard allows the common-mode rejection to be restored by guarding the inputs as shown in the diagram below.

### DATA GUARD "BOOTSTRAPS" PARASITICS FOR COMMON-MODE SIGNALS

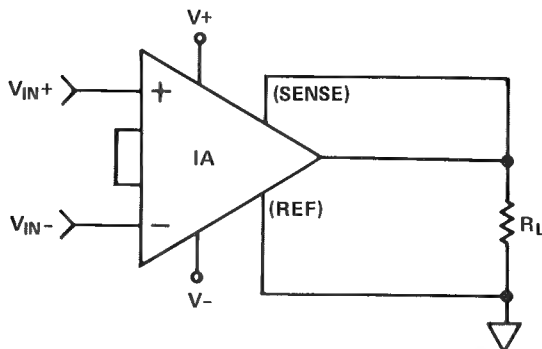


The parasitic components of the PC board are "bootstrapped" for common-mode signals. That is, if there is no voltage across the strays and leakages, no current will flow. Therefore, the effects of these parasitics are minimized.

#### Sense Terminal

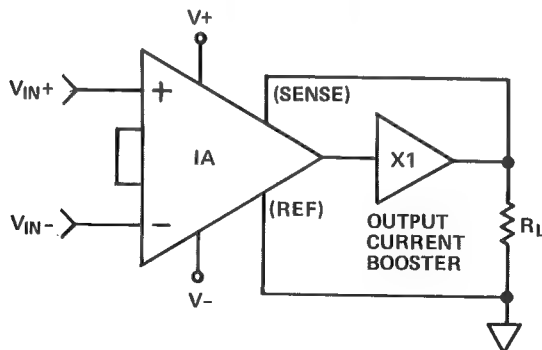
The sense terminal is the feedback point for the IA output amplifier. Normally it is connected directly to the IA output. If heavy load currents are to be drawn through long leads, IR drops can cause errors. Under these conditions, the sense terminal can be wired to the IA output at the load, putting the IR drops inside the loop and virtually eliminating this source of error.

### INSTRUMENTATION AMPLIFIER OUTPUT CONNECTIONS



Typically, IC instrumentation amplifiers are rated for a full  $\pm 10$  volt output swing into a  $2k\Omega$  load. In some applications, however, more current is required. This cannot be provided on-chip because of the damaging effect of thermal gradients, due to differential heating, on the analog accuracy of an IA. A high-current booster, which can be an inexpensive audio amplifier in unity gain mode, may be connected inside the loop of an instrumentation amplifier to provide the required current boost without degrading overall performance. Non-linearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier, as is offset drift.

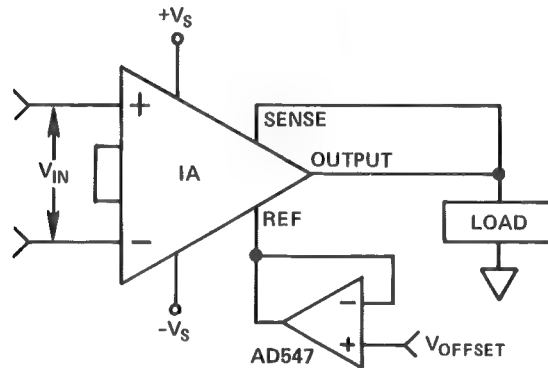
### INSTRUMENTATION AMPLIFIER WITH OUTPUT CURRENT BOOSTER



### Reference Terminal

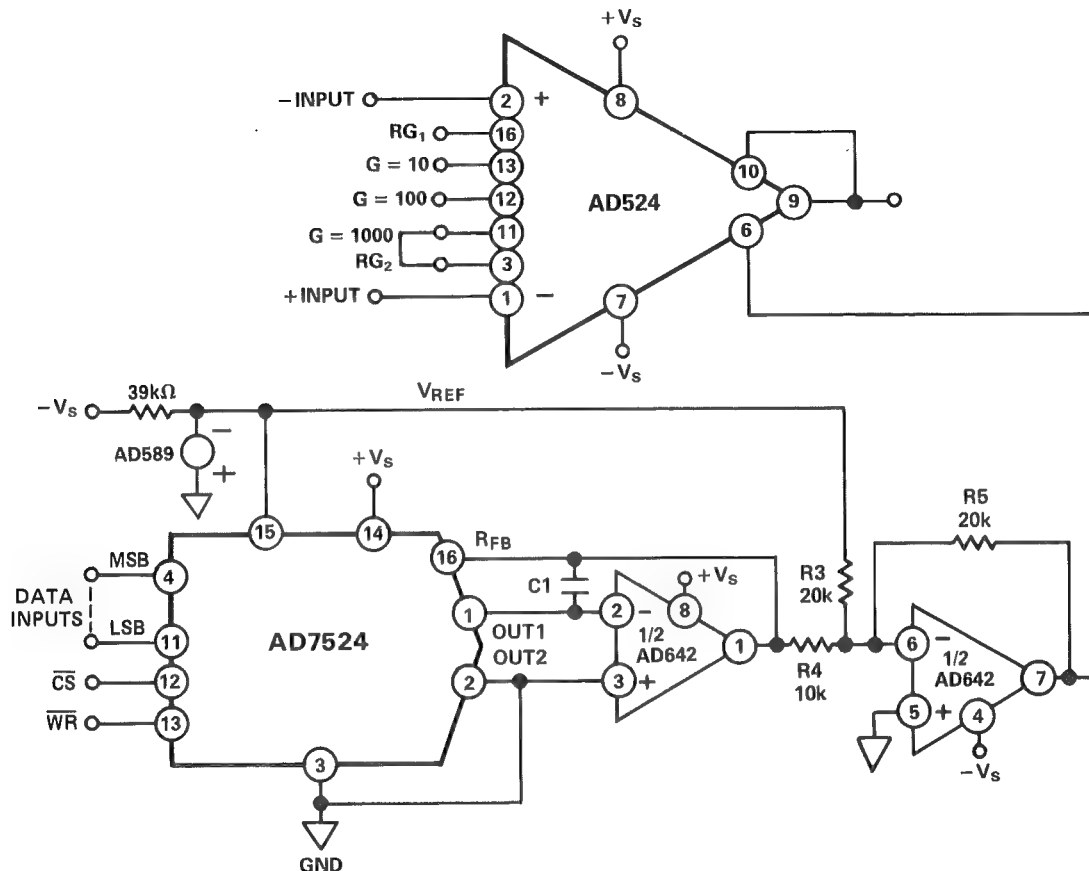
The reference terminal may be used to offset the output by up to  $\pm 10$  volts. This is useful when the load is floating or does not share a ground with the rest of the system. It also provides a means of injecting a precise offset. When injecting this offset, it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA. An operational amplifier is an ideal choice to provide this low impedance reference point.

### USE OF REFERENCE TERMINAL TO PROVIDE OUTPUT OFFSET



In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature, offset effects can be nulled by the use of trim pots. Over a wide operating temperature range, however, offset nulling becomes a problem. The circuit below uses a CMOS DAC connected to the reference terminal to provide software controllable offset adjustments.

### SOFTWARE CONTROLLABLE OFFSET





## Grounding and Decoupling

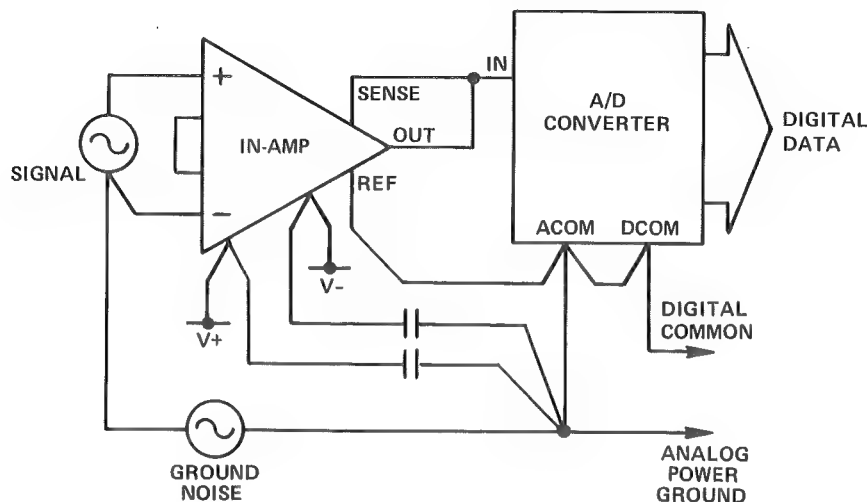
Data acquisition components usually have two or more ground pins which are not connected together within the device but have to be connected to a ground system externally. Ideally, a single solid ground would be desirable and typically that is what is used. The result is that a great amount of effort and many decoupling components are expended attempting to correct problems created by poor ground current management. In large systems and systems which combine high-level and low-level signals, "ground" (or common bus) management becomes an important aspect of design. Allowing low-level analog signals to share conductors with logic returns or power connections is an invitation to trouble.

In large systems it is often impractical to rely on a single common point for all analog signals. In these cases, some form of differential amplifier is required to translate signals between grounding systems. A simple subtractor or instrumentation amplifier can often be used for this purpose, translating a signal which is referred to one ground system into a similar or amplified signal which is referred to a different ground system. The common-mode rejection of the amplifier is used to eliminate the effects of voltage differences between the two ground or common points.

If an operational amplifier is used as a subtractor the op amp should be powered from the load power and/or decoupled with respect to load common. The reason for this can be deduced from the circuit architecture of the most common types of op amps. An op amp converts a differential input signal to a single-ended output signal. In many popular op amps the differential-to-single-ended conversion is done with respect to  $V_-$ , and the resulting signal drives an integrator. The integrator characteristic is used to frequency compensate the amplifier, and its input is referred to the single-ended output, at  $V_-$ . The integrator acts as a unity gain follower for fast signals applied to its noninverting (or reference) input. As a result, signals applied to the  $V_-$  terminal have their high frequency components conveyed directly to the output. Signals having frequency components above the amplifier closed-loop bandwidth will be transmitted from  $V_-$  to the output with little or no attenuation.

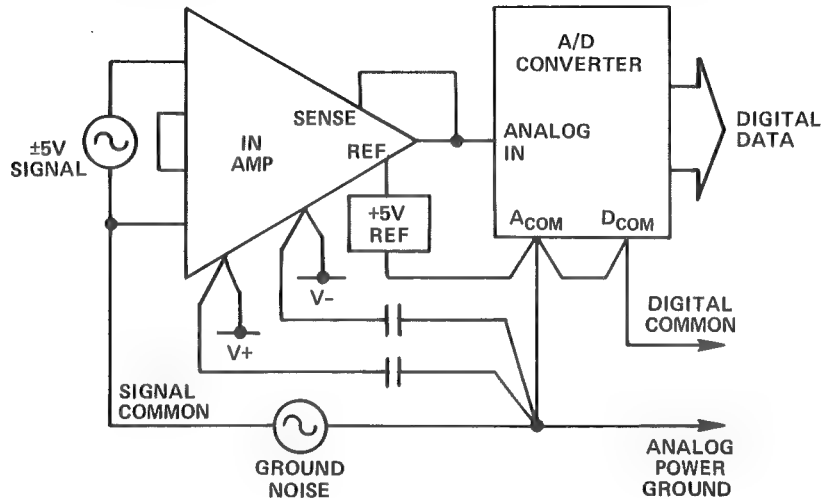
As discussed earlier, the noise rejection performance of the subtractor depends on carefully matched source and feedback resistance ratios and it cannot be used in all situations. Whenever the source impedance cannot be controlled or is exceptionally high, the subtractor (or dynamic bridge) becomes impractical. In this situation, ground noise and other remote grounding difficulties can often be avoided by the use of an instrumentation amplifier. The IA accepts differential input signals at its high impedance input. It provides a fixed gain without introducing overall feedback joining the input and output circuitry. The output signal is developed with respect to a reference terminal, which may be connected to the input common of a remote load-circuit.

## INSTRUMENTATION AMPLIFIER SIMPLIFIES SIGNAL CONDITIONING FOR A/D CONVERTER



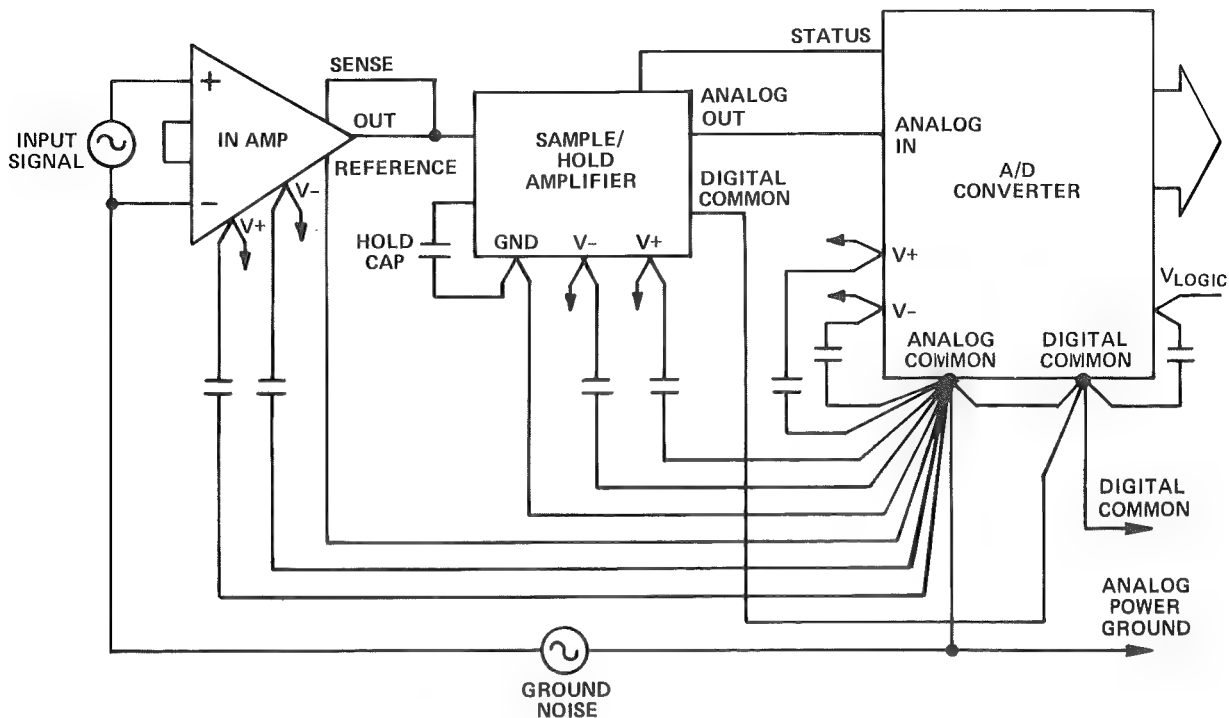
Some IAs are quite versatile and can be adapted to provide additional functions while they isolate common returns. For example, converting a bipolar input signal for use with a unipolar ADC. By referring the IA output to +5 volts, the  $\pm 5$  volt amplifier input signal will appear as a 0 to +10 volt signal to the converter. This extra feature can be provided without compromising the ground noise rejection of the system.

## INSTRUMENTATION AMPLIFIER USED FOR BIPOLAR OFFSET AND ISOLATION



In data acquisition systems containing instrumentation amplifiers, sample-and-hold amplifiers and A/D converters the grounding problems become complex. In such a case, the analog subsystem should be powered by a supply with a local common return which may be connected to the digital common but does not share any current carrying conductors. Ideally, there are not foreign currents which flow between the analog system and the digital system, except for those within the converter. If the two systems are joined only at the converter, the foreign currents share the shortest path, and their effects are minimized.

## DATA ACQUISITION SYSTEM GROUNDING



### Discrete Instrumentation Amplifiers

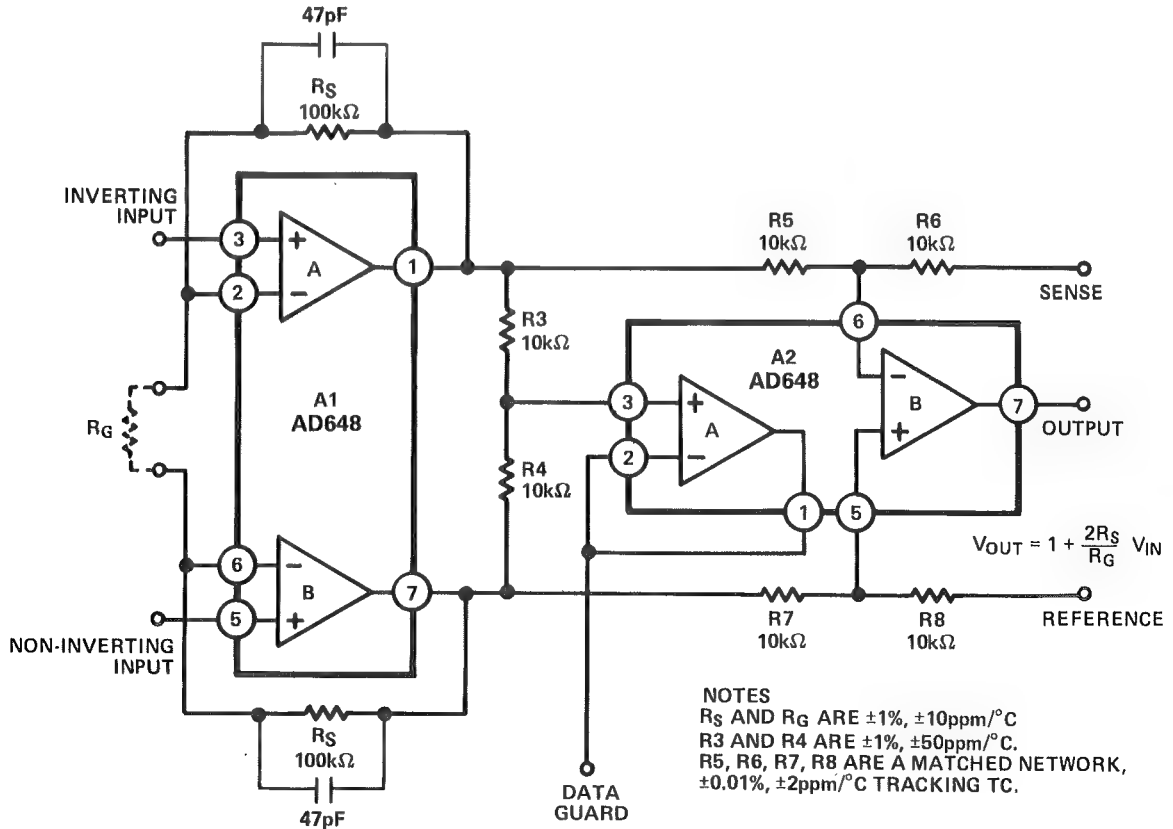
Various forms of discrete instrumentation amplifiers can be constructed using IC operational amplifiers. The advantage of a discrete IA is flexibility in design, optimizing the IA for the most important aspect of a particular application, for instance, using FET input op amps for low bias currents or using fast, precision amplifiers for wideband applications. The disadvantage of a discrete design is that careful component selection is required.

The "classic" 3 op amp instrumentation amplifier can be implemented using 2 dual FET input amplifiers for applications requiring low bias currents and low power. In this application, the matching characteristics of the two amplifiers are critical to ensure high performance. The use of an AD648C ( $A_1$ ) as the input amplifiers, guarantees a maximum input offset voltage of  $300\mu\text{V}$ , input offset voltage drift of  $3.0\mu\text{V}/^\circ\text{C}$  and bias currents of  $10\text{pA}$ . The AD712C may be substituted for greater speed, at the cost of increased supply current ( $200\mu\text{A}$ ).

vs. 2.8mA per amplifier).  $A_2$  serves less critical functions in the IA and, therefore can be an AD648A. Amplifier A of  $A_2$  is an active data guard which increases ac CMR and minimizes extraneous signal pickup and leakage. Amplifier B of  $A_2$  is the output amplifier of the IA.

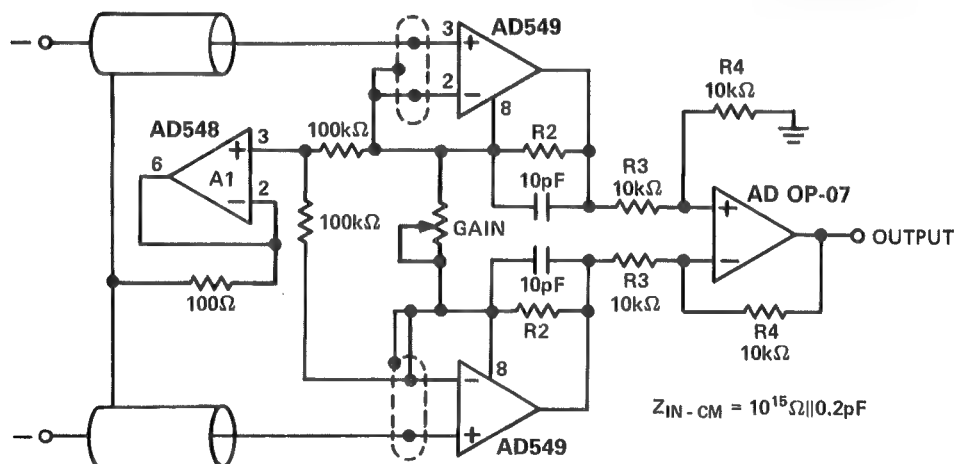
The external resistor characteristics are very critical to achieve the precision available from the AD648C in this configuration, therefore, a great deal of care should be taken in their selection. CMRR will depend upon the matching of resistors  $R_5$ ,  $R_6$ ,  $R_7$  and  $R_8$ . For example, a resistor mismatch of 0.1% results in a CMR of 60dB while a 0.01% will yield an 80dB CMR. The gain drift and CMR over temperature is directly effected by the TC match of the resistors used, therefore, it is recommended that a matched resistor network which tracks to  $\pm 2\text{ppm}/^\circ\text{C}$  should be used.

## PRECISION FET INPUT INSTRUMENTATION AMPLIFIER



If there is a need for even lower bias current, a pair of AD549Cs (0.075pA) bias currents should be used as the input amplifiers. The AD549 has laser-trimmed offset voltage of 250 $\mu\text{V}$ , low drift (5.0 $\mu\text{V}/^\circ\text{C}$ ), low noise (4.0 $\mu\text{V}$  p-p, 0.1 to 10Hz) and low power consumption (600 $\mu\text{A}$  supply current).

## VERY HIGH IMPEDANCE INSTRUMENTATION AMPLIFIER

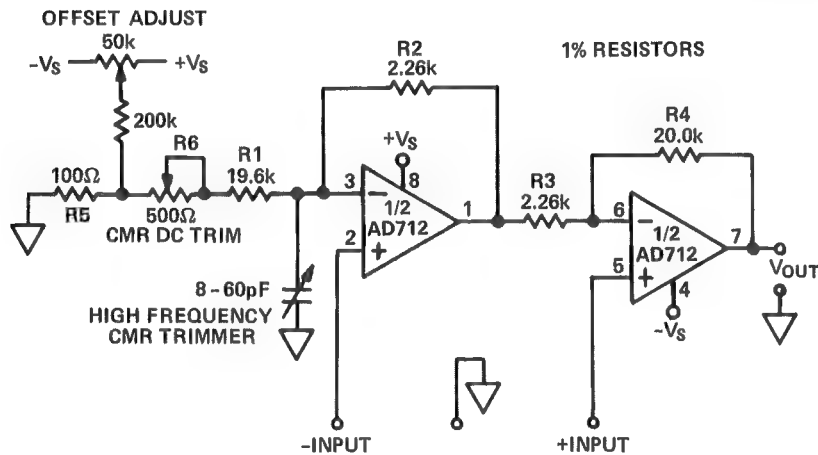


(ALL RESISTORS OF SAME NUMBER SHOULD BE MATCHED  $\pm 0.1\%$ )

(BUFFER A1 BOOSTS COMMON MODE  $Z_{IN}$  BY DRIVING CABLE SHIELDS AT COMMON MODE VOLTAGE AND NEUTRALIZING CM CAPACITANCE)

A two op amp IA built with an AD712 can provide high accuracy signal conditioning with high frequency input signals. The circuit will have an offset voltage drift of 5V/°C, CMRR of 90dB over a range of dc to 1kHz and a bandwidth of 500kHz (–3dB) at 1V p-p output. The circuit can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

## WIDE BANDWIDTH INSTRUMENTATION AMPLIFIER



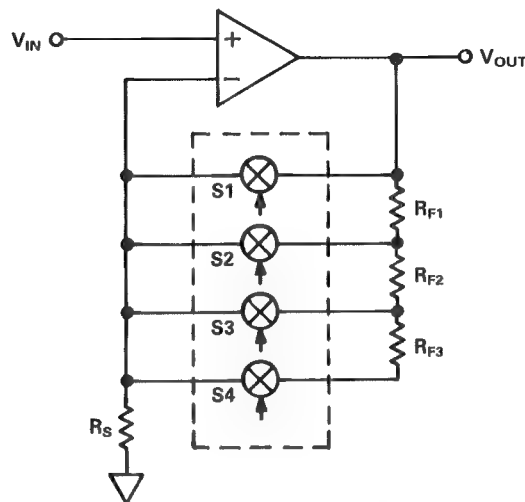
$$V_{OUT} = \left[ \left( \frac{R_4}{R_3} + 1 \right) (+V_{IN} + V_{OS2}) - (-V_{IN} + V_{OS1}) \left( \frac{R_4}{R_3} \right) \left( \frac{R_2}{R_1} + 1 \right) \right]$$

INSTRUMENTATION AMPLIFIER WITH GAIN OF TEN

### 4. SINGLE-ENDED SPGA

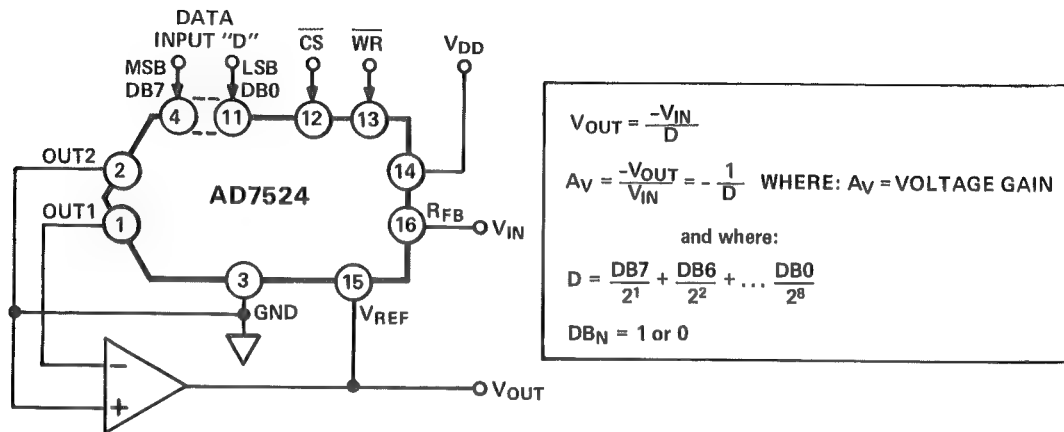
The previous section discussed software programmable gain configurations of instrumentation amplifiers. SPGA applications include gain ranging pre-amps and dynamic range extension for ADC systems. The advantages of an IA based system is its high common-mode rejection which reduces the effects of noise between grounding systems. Its disadvantage is that a minimum of two packaged devices is required and choosing precision, ratio matched resistors (or a network) may be necessary.

## PGA USING OP AMP AND CMOS SWITCHES



In systems where ground management does not require high CMR the IA may be replaced by a less expensive operational amplifier. An op amp configured for noninverting gain has desirable high input impedance and can be made software programmable with a CMOS DAC in the feedback loop, or by using precision resistors and CMOS switches to select the gain setting resistance. An advantage to this approach (other than cost) is the op amp may be chosen for a particular attribute (FET input for high input impedance, wideband for fast response). Its drawback, like that of the IA based system, is the number of components required and the use of precision resistors or networks.

## PGA USING OP AMP AND CMOS DAC



The AD526 is a complete single-ended SPGA in monolithic form. Its design includes a FET input op amp, precision laser-trimmed gain setting resistor ladders, JFET analog switches and microprocessor compatible logic. Its dc accuracies are consistent with the levels required for 12 bit systems, while its ac performance exceeds that of many IA based SPGAs.

## AD526 FEATURES

**Digitally Programmable Binary Gains from 1 to 16**  
**Two-Chip Cascade Mode Achieves Binary Gain from 1 to 128 with No Additional Components**

### Gain Error:

0.01% max, Gain = 1, 2, 4 (C Grade)  
 0.02% max, Gain = 8, 16 (C Grade)

### Fast Settling Time

Without Gain Change:

0.01% in 4.5μs (Gain = 16)

With Gain Change:

0.01% in 5.6μs (Gain = 16)

**Low Nonlinearity: ±0.035% FSR max (A Grade)**

### Excellent dc Accuracy:

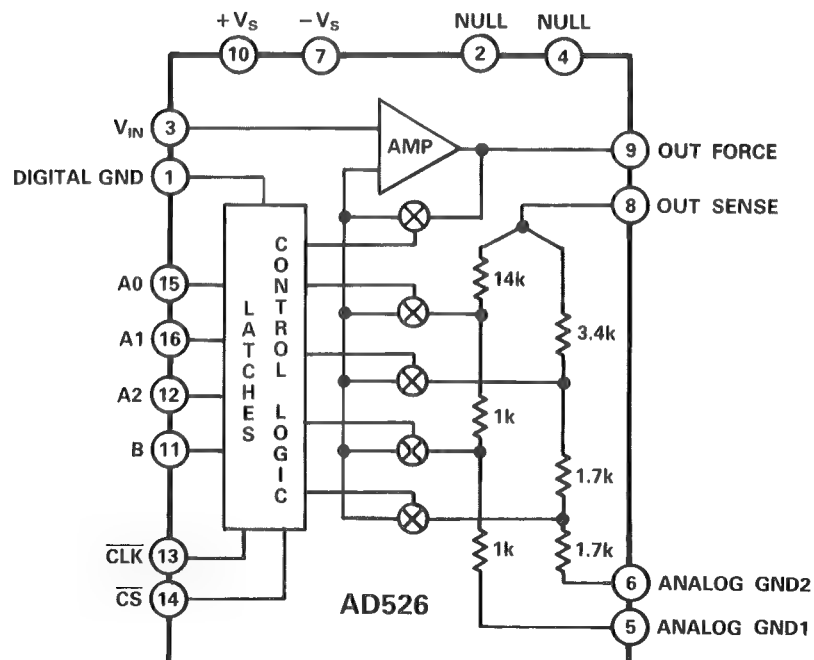
Offset Voltage: 0.7mV max (A Grade)

Max Offset Voltage Over Temperature

0.4mV (C Grade)

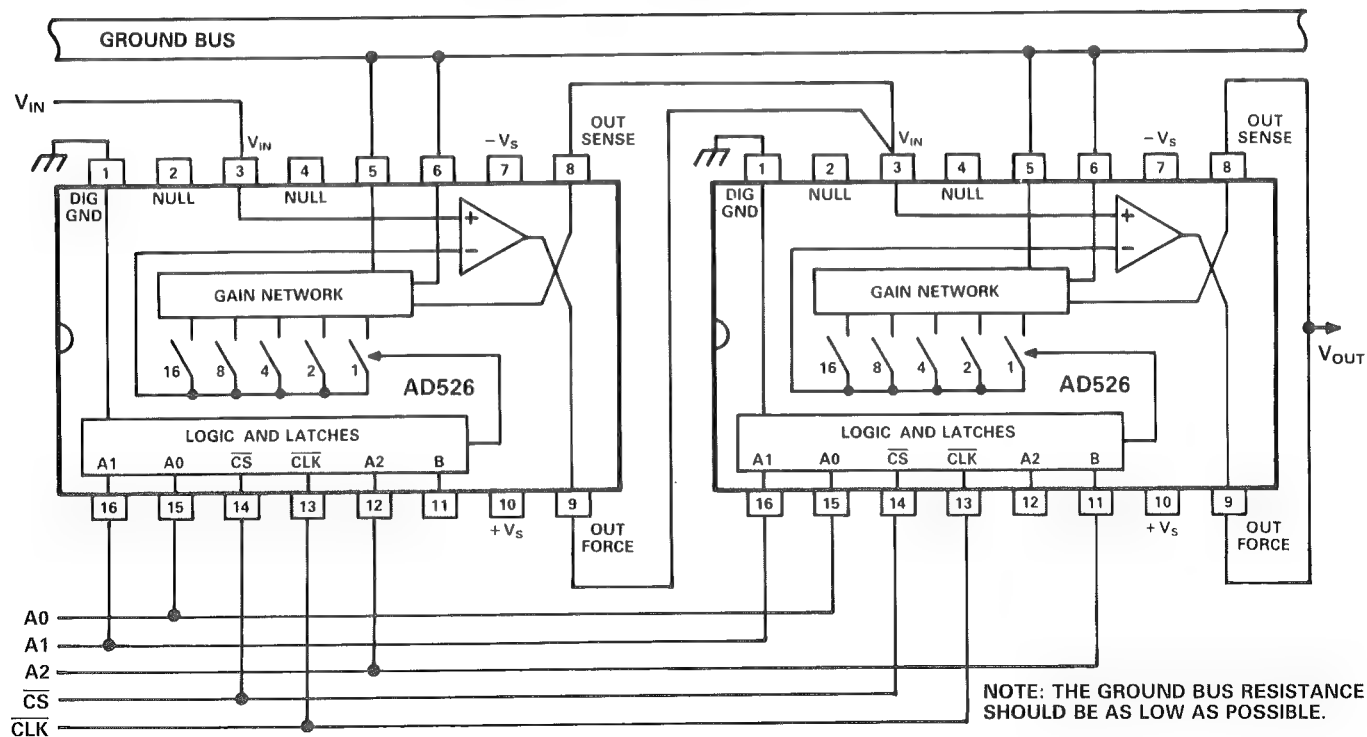
**TTL Compatible Digital Inputs**

## AD526 BLOCK DIAGRAM



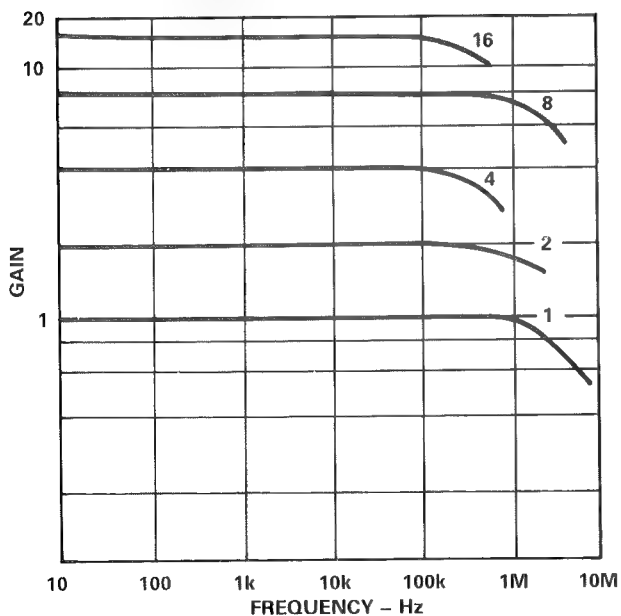
Binary gain settings (1, 2, 4, 8 and 16) make the AD526 ideal for use as dynamic range extension for analog-to-digital converter systems. A single AD526 can extend a 12-bit converters dynamic range to over 85dB. By cascading two AD526s, gains of 32, 64 and 128 can also be made available without using additional external components.

## CASCADED OPERATION

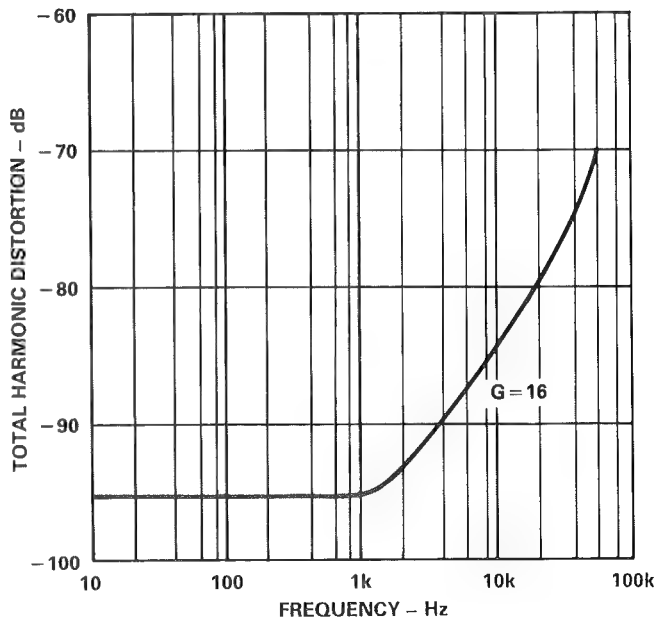


Small signal bandwidths of IA based SPGAs are typically below 1MHz at gains of one and fall lower as gain is increased. The AD526 maintains a small signal bandwidth greater than 1MHz for gains of 1, 2 and 4, while for gains of 8 and 16, the frequency compensation is automatically changed such that amplifier bandwidth is increased and SPGA settling time, slew rate, and bandwidth are improved over a constant compensation scheme. Settling time is typically 4 $\mu$ s regardless of gain, as opposed to 15 $\mu$ s for IA approach.

### AD526 GAIN VS. FREQUENCY



### AD526 TOTAL HARMONIC DISTORTION VS. FREQUENCY

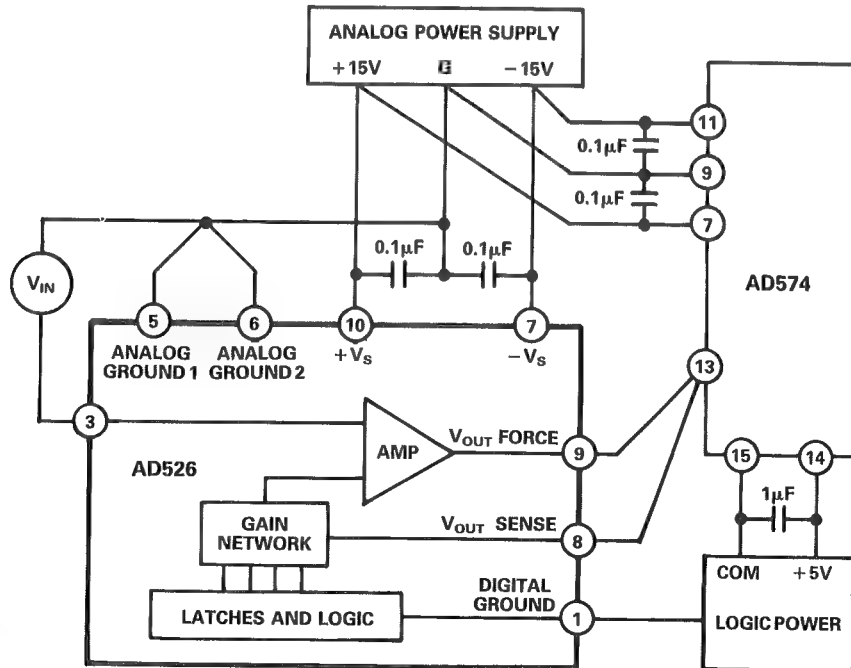


As previously mentioned, the AD526 dc accuracies are constant with 12-bit systems (0.01% gain error, 0.005% nonlinearity error, and 0.5mV offset error; AD526B), therefore it is ideal for use in systems utilizing ADCs such as the AD574A.

In such a system, attention must be paid to signal and ground paths. Logic and signal grounds should be separate, and the signal source reference point must be connected locally to the AD526 ground pins (5 and 6) in order to maintain the gain accuracy of the device. Currents associated with other elements within the system should not be allowed to corrupt this ground connection.

The force and sense outputs of the AD526 are used in the same manner as those of an instrumentation amplifier. They should be connected together at the load to avoid signal drops when driving long distances and/or moderately low impedances. When driving very low impedances, a high current buffer stage can be added inside the loop.

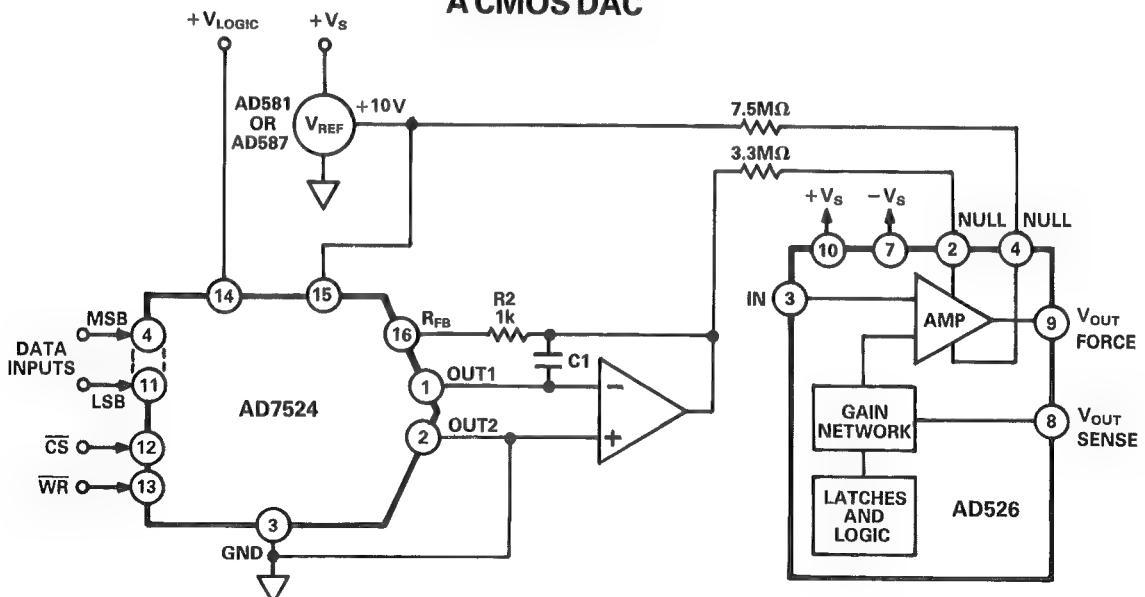
## GROUNDING AND BYPASSING



The AD526 SPGA offers low, constant input offset voltage (250µV; AD526C) over all gain settings. To null this offset, a 20kΩ potentiometer should be used between the null pins (2 and 4) with the wiper tied to  $-V_S$ .

Microprocessor controlled offset nulling can be accomplished with an 8-bit CMOS DAC circuit instead of the trimpot configuration. Its advantage is that it can be implemented as part of an autocalibration scheme, with dipswitches, novram or RAM storing the 8-bit word after its value has been determined. Offset null sensitivity of this circuit is 80µV per LSB at a gain of 16 which guarantees dc accuracy to the 16-bit performance level.

## AD526 OFFSET NULLING USING A CMOS DAC



## 5. ISOLATION AMPLIFIERS

Instrumentation amplifiers are restricted by the requirement that a return path for bias currents must be provided. Furthermore, large common-mode voltages can damage IA input circuitry. When the application involves galvanic or ohmic isolation of input and output circuitry, an Isolation Amplifier is required.

### WHEN AN ISOLATION AMPLIFIER IS REQUIRED

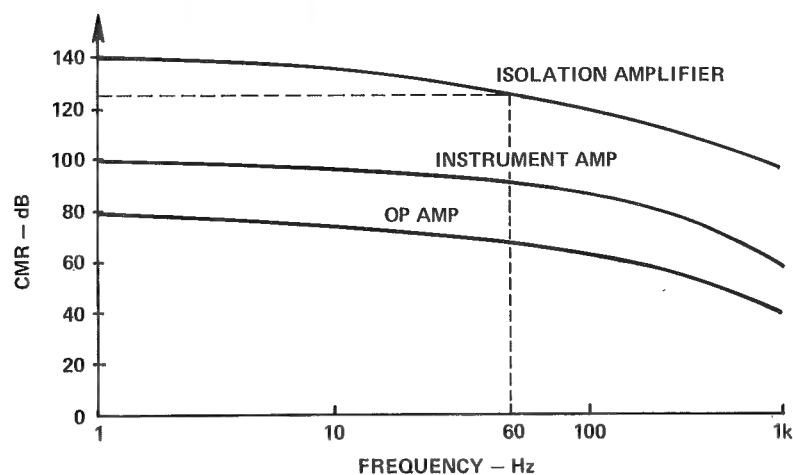
- Measure Low Level Signals in the Presence of High CMV.
- Eliminate Measurement Errors Caused by Disturbances on the Source Ground Network (from High Current Transients, etc.)
- Avoid Ground Loops and Their Attendant Pickup Problems. (No Need to Provide a Return Path for Bias Currents.)
- Protect Processing Circuitry from Damage from Large CMV Levels at Both Input and Output.
- Provide Patient-Safe Interface.

#### Ohmic and Galvanic Source Isolation

The isolation amplifier's floating input design provides complete decoupling between the source and amplifier output and, in most cases, power terminals. This offers other benefits beyond the high common-mode rejection.

Low capacitance and leakage from input to common gives very high CMR virtually independent of source imbalance.

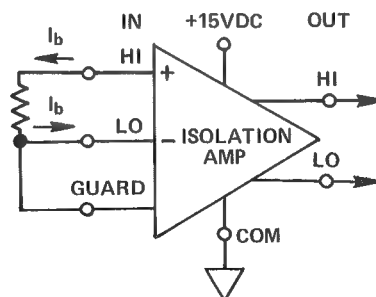
### TYPICAL CMR VS FREQ WITH 1k $\Omega$ SOURCE IMBALANCE FOR VARIOUS TYPES OF DEVICES



#### No Bias Current

The front end circuitry of isolation amplifiers is fully floating and, therefore, no net bias current flows in the input leads. As shown below, the bias current of the LO input is supplied by the HI input. Thus, the isolator does not require connections to the source ground in order to establish the input bias current flow and, therefore, is not affected by disturbances on the source ground system.

### ISOLATORS REQUIRE NO NET BIAS CURRENT





## SELECTING AN ISOLATOR

Isolation amplifiers may be used to advantage in a limitless number of situations, but the vast majority of applications fall into one of three categories: Medical, Industrial (process control) and Instrumentation (data acquisition).

### Medical

Medical amplifiers must first and foremost protect the patient from leakage currents and amplifier fault currents in excess of 10 microamps rms. It is just as important to be sure that the amplifier will not be damaged by 5kV defibrillator pulses; if an amplifier monitoring a patient's heartbeat should fail during defibrillation, the medical team may continue to defibrillate the patient in the belief that the heart has not restarted (while, in fact, the amplifier has failed). Continued defibrillation can kill the patient.

### Industrial

Industrial amplifiers must provide accurate signal gain while rejecting common-mode noise and eliminating ground loops. Industrial malfunctions may cause power-line voltages to be imposed on low voltage signal lines. The industrial isolator should not be destroyed by such mistreatment, but more important, it must protect the expensive computer on the other end of the line from errant high voltage surges.

### Instrumentation

Instrumentation (data acquisition) applications may not involve the extreme hazards of medical or industrial applications, but the precision required may demand the feature of an isolator. Twelve-bit systems require accuracies of  $\pm 0.01\%$  and are therefore quite susceptible to ground loops or common-mode interference. Isolation amplifiers can eliminate ground loops and offer better common-mode rejection than conventional data amplifiers.

## AD202/204 FEATURES

### Low Cost

### Small Size: 4 Channels/Inch

### Low Power: 35mW (AD204)

### High Accuracy: $\pm 0.025\%$ max Nonlinearity (K Grade)

### High CMR: 130dB (Gain = 100 V/V)

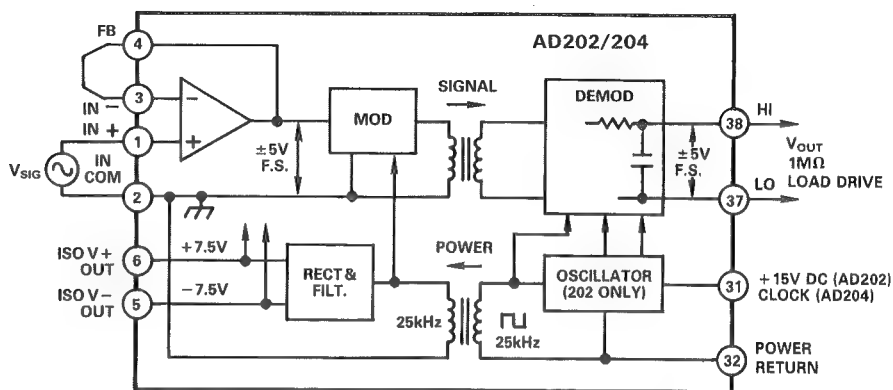
### Wide Bandwidth: 5kHz Full-Power (AD204)

### High CMV Isolation: $\pm 2000$ V pk Continuous (K Grade) (Signal and Power)

### Isolated Power Outputs

### Uncommitted Input Amplifier

AD202/204 BLOCK DIAGRAM



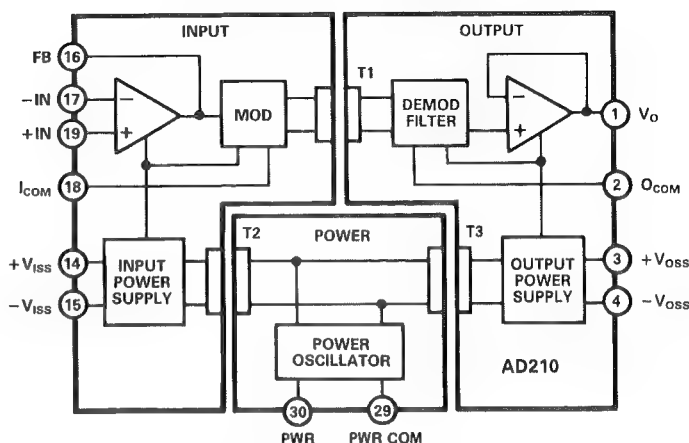
The AD202 and AD204 low cost, miniature isolation amplifiers use an amplitude modulation technique to permit transformer coupling of signals down to dc. Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately  $\pm 5$ V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multichannel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3k $\Omega$  for the AD204 (7k $\Omega$  for the AD202) and varies with signal level and temperature, so it should not be loaded. In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

## AD210 FEATURES

**High CMV Isolation: 2500V rms Continuous**  
 **$\pm 3500\text{V}$  peak Continuous**  
**Small Size: 1.00"  $\times$  2.10"  $\times$  0.350"**  
**Three-Port Isolation: Input, Output, and Power**  
**Low Nonlinearity:  $\pm 0.012\%$  max**  
**Wide Bandwidth: 20kHz Full-Power ( $-3\text{dB}$ )**  
**Low Gain Drift:  $\pm 25\text{ppm}/^\circ\text{C}$  max**  
**High CMR: 120dB ( $G=100\text{V/V}$ )**  
**Isolated Power:  $\pm 15\text{V}$  @  $\pm 5\text{mA}$**   
**Uncommitted Input Amplifier**

AD210 BLOCK DIAGRAM



Referring to the AD210 block diagram above, a  $+15\text{V}$  supply is connected to the power port, and  $\pm 15\text{V}$  isolated power is supplied to both the input and output ports via a  $50\text{kHz}$  carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The full wave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A  $20\text{kHz}$ , three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a  $2\text{k}\Omega$  load.

## 6. TRANSDUCER INTERFACING

Ideally, a transducer should have a high level output, zero source impedance, low noise and be relatively linear, however they are not. Through precious portions of this section we have characterized instrumentation and isolation amplifiers, in this portion we will outline techniques for measuring physical phenomena. The emphasis will be on solutions to problems.

## COMMON TRANSDUCERS SUMMARIZED

### TEMPERATURE

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Thermocouples	Low source impedance, typically $10\Omega$ . Voltage-output devices. Output shift is 10's of microvolts/ $^\circ\text{C}$ . Outputs typically in the millivolts at room temperature.	Low voltage output requires low-drift signal conditioning. Small size and wide temperature range are advantages. Requires reference to a known temperature. Nonlinear response.
Platinum and other RTD's	Resistance changes with temperature. Positive temperature coefficient. Typical impedance ( $0^\circ\text{C}$ ) $20\Omega$ to $2\text{k}\Omega$ . Typical sensitivities $0.1\%/^\circ\text{C}$ to $0.66\%/^\circ\text{C}$ , depending on material.	Highly repeatable. Good linearity over wide ranges. Requires bridge or other network for typical interface.
Thermistors	Resistance changes with temperature. Negative temperature coefficient. Typical impedances ( $25^\circ\text{C}$ ) of $50\Omega$ to $1\text{M}\Omega$ available. Sensitivity at $25^\circ\text{C}$ is about $4\%/^\circ\text{C}$ . Linearized networks available with $0.4\%/^\circ\text{C}$ sensitivity.	Highest sensitivity among common temperature transducers. Inherently nonlinear (exponential function) but accurate linearized networks available.
Semiconductor sensors	Voltage, current, or resistance functions. Voltage types (diodes) require excitation current. Current types (AD590) require excitation voltage. Resistive types (bulk silicon) may use either type of excitation.	Many devices are uncalibrated and require significant signal conditioning. AD590 is calibrated, linear, and requires minimal signal conditioning.

## COMMON TRANSDUCERS SUMMARIZED

### FORCE

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Strain gages (metal)	Resistance shifts with applied strain. Almost always used in bridge configuration. Typical impedance levels of $120\Omega$ and $350\Omega$ . Typical change is 0.1% over the whole range.	Resistance change with strain small compared to initial value of device resistance. Requires high-quality low-level signal conditioning.
Strain-gage bridge, load cell	Voltage output with applied strain. Requires excitation potential or current to drive the bridge. Typical excitation is from 5 to 15 volts.	Small voltage outputs require low-drift signal conditioning with good common-mode rejection to achieve any degree of precision. Output is linear.
Semiconductor strain gages	Bridge types are assembled from individual gages and have a voltage output. Bridge requires excitation, typically 5V to 15V.	More output than metal strain gages, but with increased non-linearity and sensitivity to temperature.
Piezoelectrics	True charge output device. Modeled as voltage source in series with capacitor. Physical input change produces corresponding charge change. AC and transient response only. Typical upper frequency limit is 20 to 50kHz. Typical output is $10^{-7}$ coulombs full-scale.	Requires low-bias-current charge amplifier configurations for signal conditioning. Responds to ac signals only.

### PRESSURE

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Rheostat/potentiometer	Resistance or ratio-of-resistance output. Requires voltage or current excitation. Typical impedance $500\Omega$ to $5k\Omega$ .	High-level easy-to-condition outputs are typical due to significant resistance or ratio
Strain gage	Resistance shift (single gage) or voltage output (strain-gage bridge). Requires excitation potential or current.	Small resistance change. Low-level signal requires good signal-conditioning amplifiers.

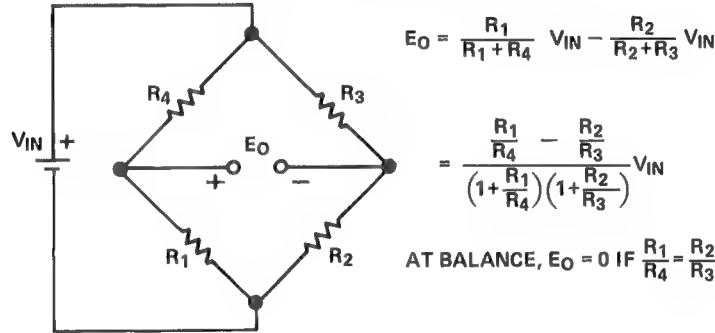
### FLOW

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Pressure-based	See PRESSURE transducers	Pressure types measure flow by measuring $\Delta P$ between static and flow-caused pressure, or pressure drop across a constriction. Differential pressure transducers are used to avoid common-mode pressure errors. Response is nonlinear.
Frequency-output types: paddle wheels, rotary types, vortex types	Digital output derived from frequency output are common. Optical or magnetic pickups provide non-invasive measurements. Photocell has $100\Omega$ to $100M\Omega$ on-to-off ratio. Magnetic employs switching or open-collector transistor.	Some types are directly logic-level compatible. Others require impedance and/or voltage amplification, level-shift, and buffering before signal is usable.

### Bridge Circuits

The figure below shows the common Wheatstone bridge (actually developed by S.H. Christie in 1833). In its simplest form, a bridge consists of four two-terminal elements connected to form a quadrilateral, a source of excitation (voltage or current) connected along one of the diagonals, and a detector of voltage or current comprising the other diagonal. The detector measures the difference between the outputs of two potentiometric dividers connected across the excitation supply.

### BASIC BRIDGE CIRCUIT – VOLTAGE EXCITATION AND VOLTAGE READOUT



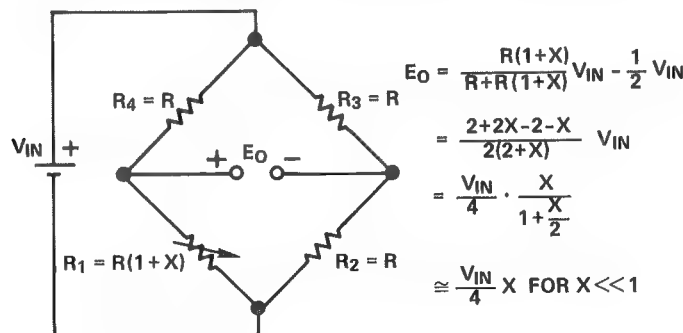
A bridge measures an electrical property of a circuit element indirectly, i.e., by comparison against a similar element. The two principle ways of operating a bridge are as a null detector and as a device that reads a difference directly in voltage or current.

When  $R_1/R_4 = R_2/R_3$ , the resistance bridge shown is at a *null*, irrespective of the mode of excitation (current or voltage, ac or dc), the magnitude of excitation, the mode of readout (current or voltage), or the impedance of the detector. Therefore if the ratio  $R_2/R_3$  is fixed at  $K$ , a null is achieved when  $R_1 = K R_4$ . If  $R_1$  is unknown and  $R_4$  is an accurately determined variable resistance, the magnitude of  $R_1$  can be found by adjusting  $R_4$  until null is achieved. Conversely, in transducer-type measurements,  $R_4$  may be a fixed reference and a null occurs when the magnitude of the measurand is such that  $R_1$  is equal to  $K R_4$ .

Null-type measurements are principally used in feedback systems, involving electromechanical and/or human elements. Such systems, as noted previously, seek to force the active element (strain gage, RTD, thermistor, mechanically coupled potentiometer) to balance the bridge by influencing the parameter being measured. Because the null is independent of the excitation, the null mode may also be used to discriminate between the two polarities of output, i.e., as a comparator. In such applications, the polarity of the off-null signal may be of greater significance than its magnitude (for example, if the level of a tank is below a preset value, a valve is caused to open to fill the tank).

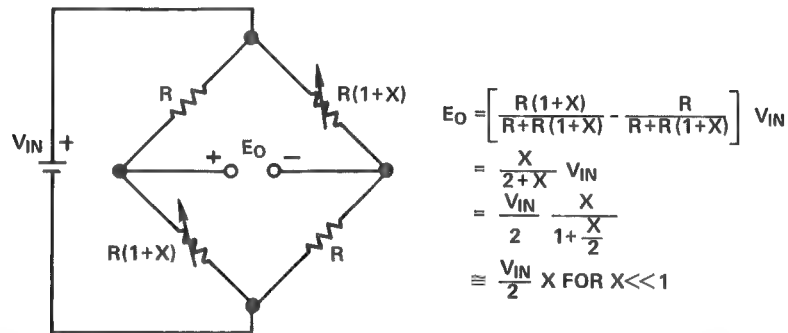
For the majority of transducer applications employing bridges, the deviation of one or more resistors in a bridge from an initial value must be measured as an indication of the magnitude (or a change) of the measurand. The figure below shows a bridge with all resistances nominally equal; but one of them ( $R_1$ ) is variable by a factor,  $(1 + X)$ , where  $X$  is a fractional deviation around zero, as a function of (say) strain. As the equation indicates, the relationship between the bridge output and  $X$  is not linear, but for small ranges of  $X$  it is sufficiently linear for many purposes. For example, if  $V_{IN} = 10V$ , and the maximum value of  $X$  is  $\pm 0.002$ , the output of the bridge will be linear to within 0.1% for a range of outputs from 0 to  $\pm 5mV$ , and to 1% for the range 0 to  $\pm 50mV$  ( $\pm 0.02$  range for  $X$ ).

### BRIDGE USED TO READ DEVIATION OF A SINGLE VARIABLE ELEMENT



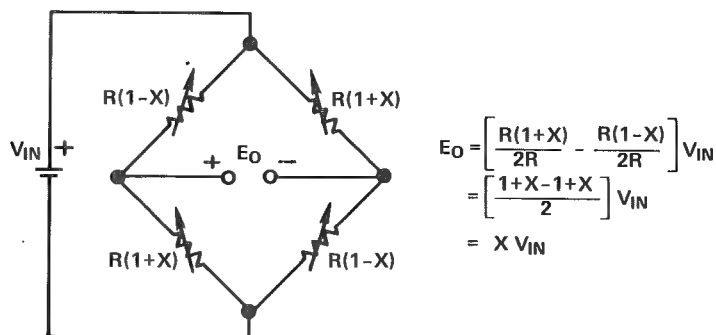
The *sensitivity* of a bridge is the ratio of the maximum expected change in the output value to the excitation voltage. For the examples given in the previous paragraph, the sensitivities are  $\pm 500\mu\text{V/V}$  and  $\pm 5\text{mV/V}$ . The sensitivity can be doubled if two identical variable elements can be used, e.g., at positions  $R_3$  and  $R_1$ , as shown below. An example of such a pair is two identically oriented strain gage resistances aligned in a single pattern. Note that the output of such a pair is doubled, but the nonlinearity remains the same.

### BRIDGE WITH TWO VARIABLE ELEMENTS



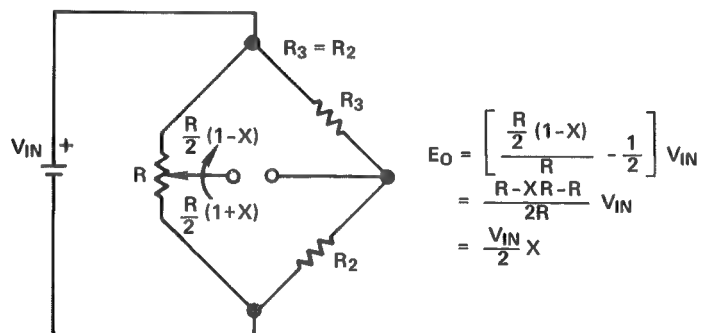
In special cases, another doubling of the output can be achieved. The figure below shows a bridge consisting of four resistors, two of which increase and two of which decrease in the same ratio. Two identical two-element strain gages, attached to opposite faces of a thin carrier to measure its bending, could be electrically configured in this way. The output of such a bridge would be four times the output for a single-variable-element bridge; furthermore, the complementary nature of the resistance changes would result in a linear output.

### ALL ELEMENTS VARIABLE

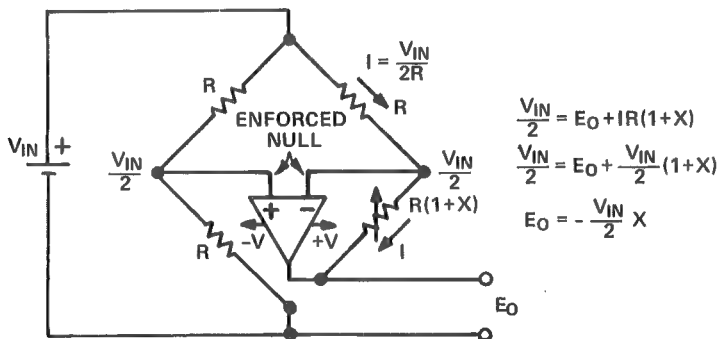


The next figure shows bridge employing a zero-centered potentiometer to constitute two adjacent arms; the position of the potentiometer is a measure of the physical phenomenon. Since it is a two-variable-element version, its output is twice that of the single-variable-element bridge, and being complimentary in nature, it is linear.

### LINEAR POTENTIOMETER AS VARIABLE ARM

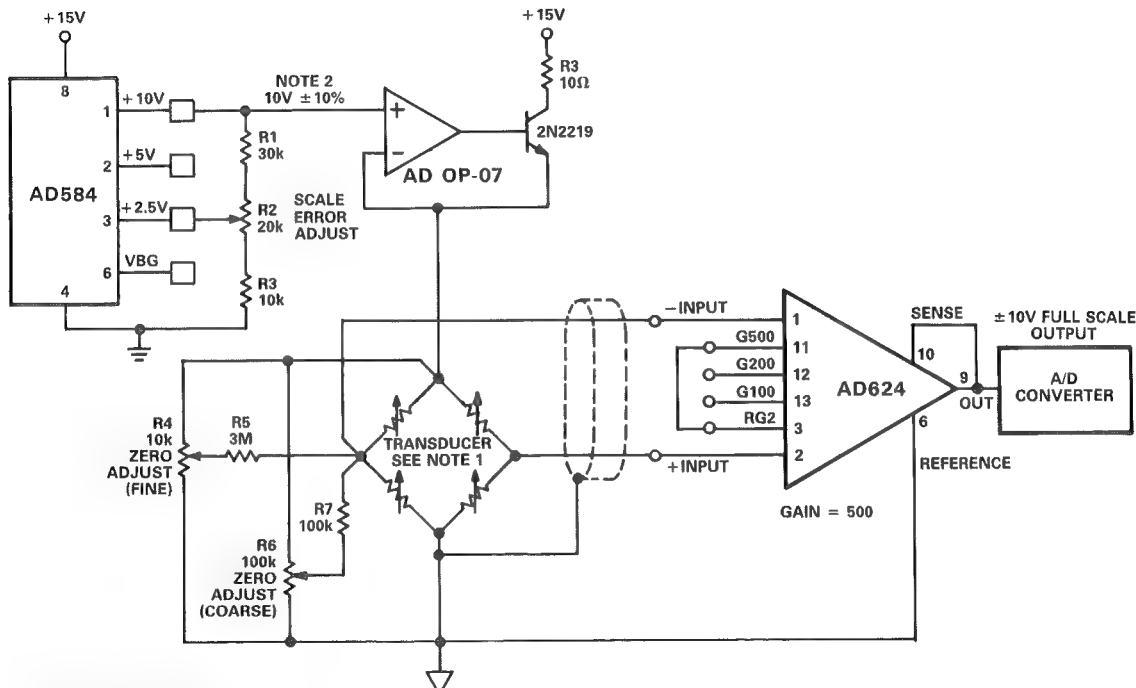


Manufacturers of transducers employing bridges address the nonlinearity issue in a variety of ways, including keeping the resistive swings in the bridge small, shaping complementary nonlinear response into the active elements of the bridge, using resistive trims for first-order corrections, and a variety of proprietary magical techniques. A bridge can, of course, be linearized by making it less sensitive (e.g., by making the initial ratios,  $R_4/R_1$  and  $R_3/R_2$ , large), but the tradeoff of sensitivity for linearity is painful.



The figure above shows an active bridge in which an op amp produces a null by adding a voltage in series with the variable arm. That voltage is equal in magnitude and opposite in polarity to the incremental voltage across  $R_x$ , and it is inherently linear with  $X$ . Since it is an op amp output, it can be used as a low-impedance output point for the bridge measurement. This active bridge has a gain of two over the standard one-active-element bridge, and the output is linear, even for large values of  $X$ .

The circuit below shows an example of how an AD624 can be used to condition the differential output voltage of a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type. The addition of an auto gain/auto tare cycle would enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

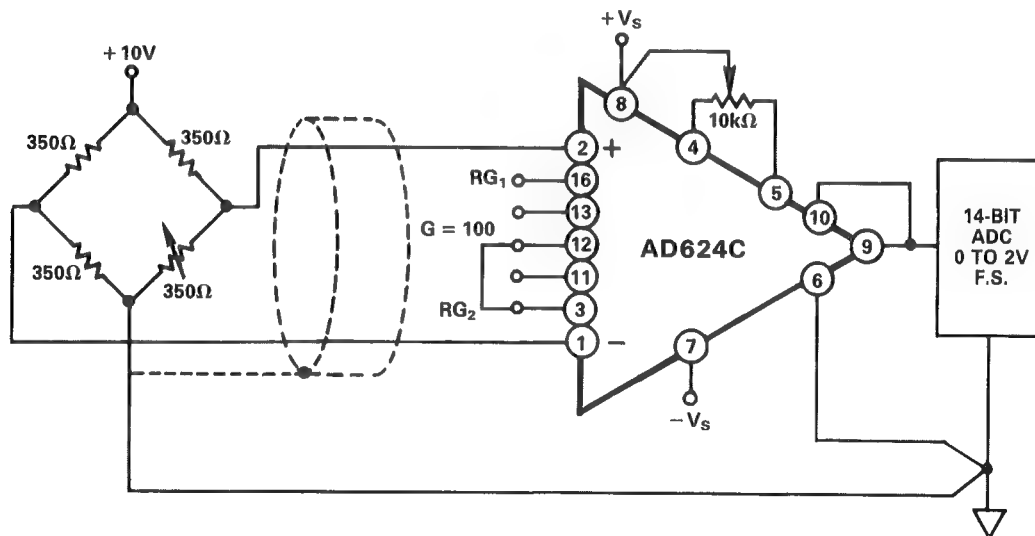


- NOTES**
1. LOAD CELL TEDEA MODEL 1010 10KG. OUTPUT  $2\text{mV/V} \pm 10\%$ .
  2. R1, R2 and R3 SELECTED FOR AD584. OUTPUT  $10\text{V} \pm 10\%$ .

## Error Budget Analysis

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. The figure shows a differential transducer, unbalanced by  $\approx 5\Omega$ , supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Therefore the largest change in temperature,  $\Delta T$ , within the operating range is from ambient to  $+85^{\circ}\text{C}$  ( $85^{\circ}\text{C} - 25^{\circ}\text{C} = 60^{\circ}\text{C}$ ).

## TYPICAL BRIDGE APPLICATION



In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of an auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

## ERROR BUDGET ANALYSIS OF AD624CD IN BRIDGE APPLICATION

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at $T_A = 25^{\circ}\text{C}$	Effect on Absolute Accuracy at $T_A = 85^{\circ}\text{C}$	Effect on Resolution
Gain Error	$\pm 0.1\%$	$\pm 0.1\% = 1000\text{ppm}$	1000ppm	1000ppm	—
Gain Instability	$10\text{ppm}/^{\circ}\text{C}$	$(10\text{ppm}/^{\circ}\text{C})(60^{\circ}\text{C}) = 600\text{ppm}$	—	600ppm	—
Gain Nonlinearity	$\pm 0.001\%$	$\pm 0.001\% = 10\text{ppm}$	—	—	10ppm
Input Offset Voltage	$\pm 25\mu\text{V}$ , RTI	$\pm 25\mu\text{V}/20\text{mV} = \pm 1250\text{ppm}$	1250ppm	1250ppm	—
Input Offset Voltage Drift	$\pm 0.25\mu\text{V}/^{\circ}\text{C}$	$(\pm 0.25\mu\text{V}/^{\circ}\text{C})(60^{\circ}\text{C}) = 15\mu\text{V}$ $15\mu\text{V}/20\text{mV} = 750\text{ppm}$	—	750ppm	—
Output Offset Voltage <sup>1</sup>	$\pm 2.0\text{mV}$	$\pm 2.0\text{mV}/20\text{mV} = 1000\text{ppm}$	1000ppm	1000ppm	—
Output Offset Voltage Drift <sup>1</sup>	$\pm 10\mu\text{V}/^{\circ}\text{C}$	$(\pm 10\mu\text{V}/^{\circ}\text{C})(60^{\circ}\text{C}) = 600\mu\text{V}$ $600\mu\text{V}/20\text{mV} = 300\text{ppm}$	—	300ppm	—
Bias Current – Source Imbalance Error	$\pm 15\text{nA}$	$(\pm 15\text{nA})(5\Omega) = 0.075\mu\text{V}$ $0.075\mu\text{V}/20\text{mV} = 3.75\text{ppm}$	3.75ppm	3.75ppm	—
Offset Current – Source Imbalance Error	$\pm 10\text{nA}$	$(\pm 10\text{nA})(5\Omega) = 0.050\mu\text{V}$ $0.050\mu\text{V}/20\text{mV} = 2.5\text{ppm}$	2.5ppm	2.5ppm	—
Offset Current – Source Resistance – Error	$\pm 10\text{nA}$	$(10\text{nA})(175\Omega) = 3.5\mu\text{V}$ $3.5\mu\text{V}/20\text{mV} = 87.5\text{ppm}$	87.5ppm	87.5ppm	—
Offset Current – Source Resistance – Drift	$\pm 100\text{pA}/^{\circ}\text{C}$	$(100\text{pA}/^{\circ}\text{C})(175\Omega)(60^{\circ}\text{C}) = 1\mu\text{V}$ $1\mu\text{V}/20\text{mV} = 50\text{ppm}$	—	50ppm	—
Common Mode Rejection 5V dc	115dB	$115\text{dB} = 1.8\text{ppm} \times 5\text{V} = 9\mu\text{V}$ $9\mu\text{V}/20\text{mV} = 444\text{ppm}$	450ppm	450ppm	—
Noise, RTI (0.1–10Hz)	$0.22\mu\text{V}$ p-p	$0.22\mu\text{V}$ p-p/20mV = 10ppm	—	—	10ppm
Total Error			3793.75ppm	5493.75ppm	20ppm

<sup>1</sup>Output offset voltage and output offset voltage drift are given as RTI figures.

The preceding table lists all applicable error sources and their corresponding effects on accuracy. Initial errors are defined as those errors that can be reduced to a negligible amount by performing an initial calibration.

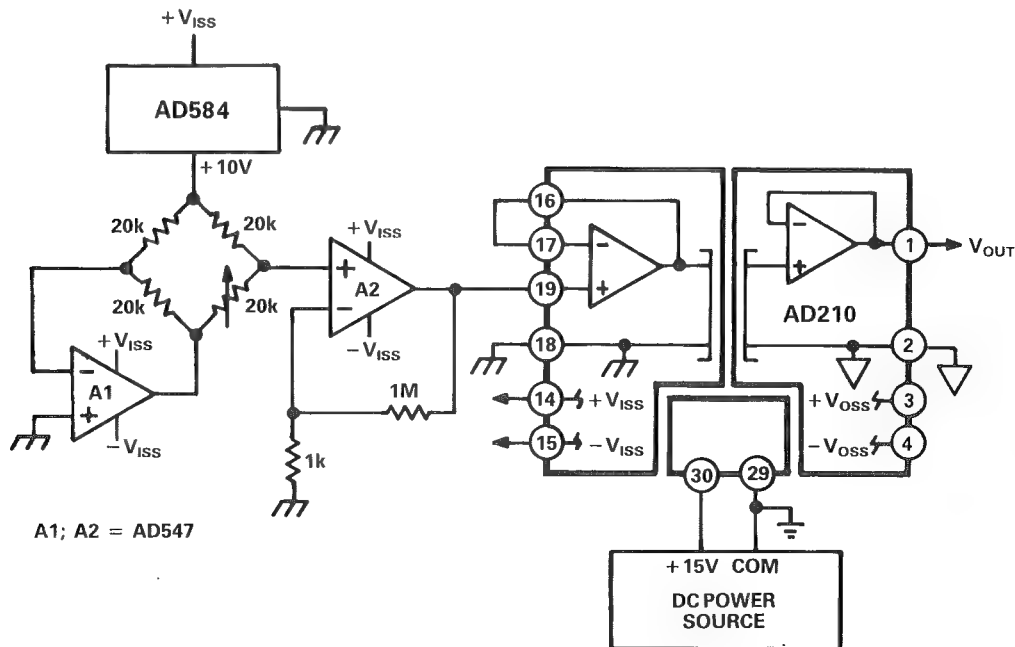
Reducible errors include these initial errors along with other errors that occur during normal operation that may be corrected by an adaptive or “intelligent” system. For example, changes in gain or offset may be measured during an auto-zero/auto-gain cycle by measuring two unknown voltages (a precision reference and ground, for example).

Irreducible errors are errors which can not be readily corrected either at initial calibration or in use.

### Isolated Industrial Applications

The circuit below illustrates one possible configuration for isolated conditioning of a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguring of the AD210's input amplifier.  $\pm V_{ISS}$  provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

### ISOLATED BRIDGE CIRCUIT



### Bridge Linearization

If one arm of a Wheatstone bridge varies from its nominal value by a factor,  $(1 + 2w)$ , the voltage or current output of the bridge will be (with appropriate polarities and scale factors):

$$y = w/(1 + w)$$

Linear response requires very small values of  $w$  (to make the denominator essentially independent of  $w$ ) and, as a consequence, preamplification.

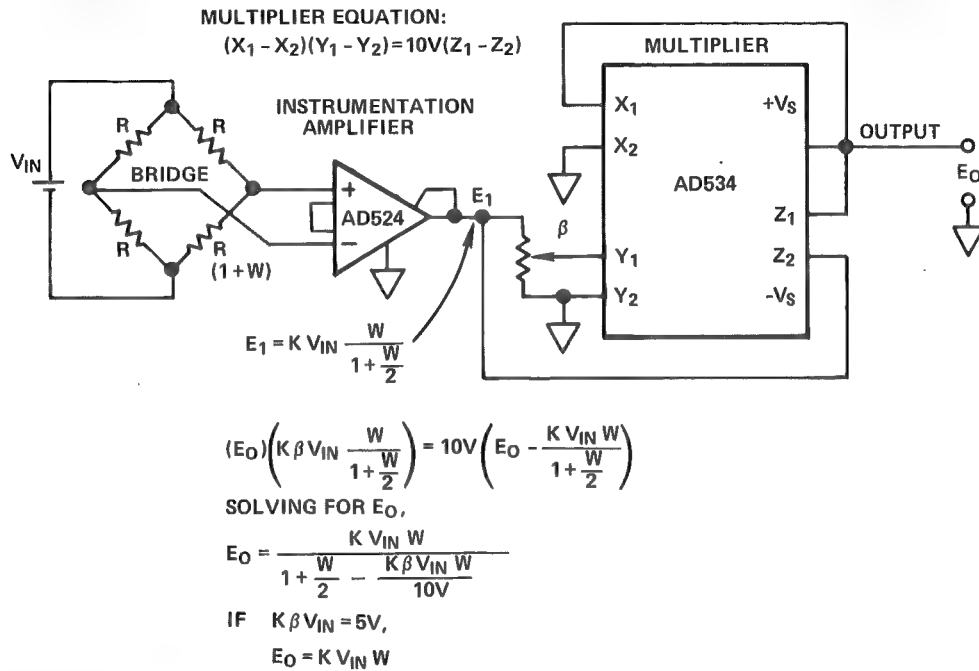
The circuit shown enables large-deviation bridges to be used without losing linearity or resorting to high attenuation. The circuit computes the inverse of the bridge function, i.e.,

$$w = y/(1 - y)$$

Depending on which arm of the bridge varies, it may be necessary to reverse the polarity of the X connections. Any resistive, linearly responding transducer (one or more legs of the bridge proportional to the phenomenon being measured) may profit from the application of this circuit. Examples include position servos, linear thermistors, platinum-resistance-wire sensors, pressure transducers and strain gages.



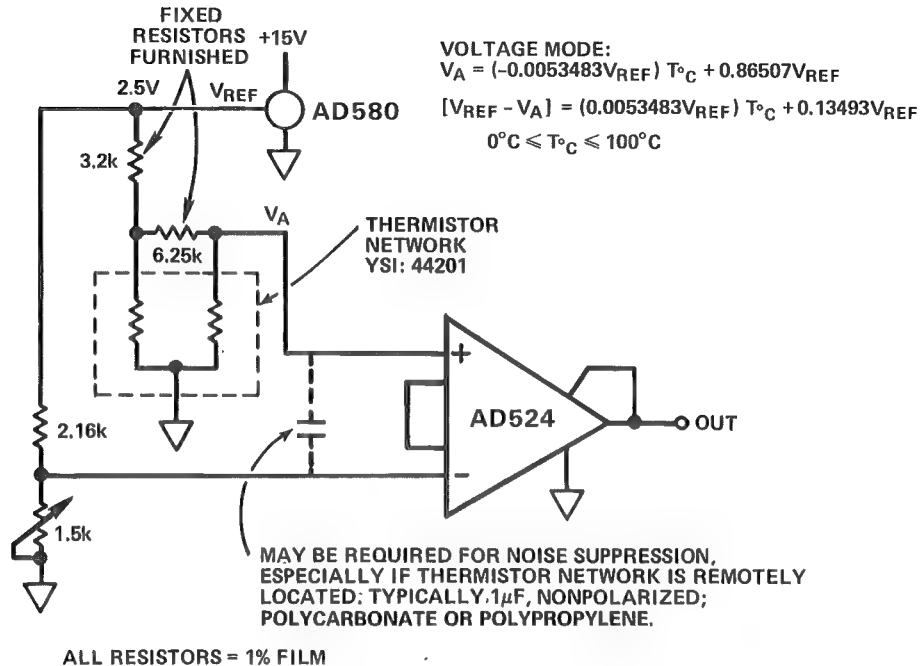
## BRIDGE LINEARIZATION USING ANALOG MULTIPLIER



### Thermistor Interface

In the figure, a thermistor is used in the potentiometric mode. Both the sensor and the offset network are supplied by a 2.5V reference. The differential of the voltages is read out by an instrumentation amplifier, which may be connected for the desired gain and output configuration.

## INSTRUMENTING LINEARIZED THERMISTORS VOLTAGE MODE



### Thermocouple Applications

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable

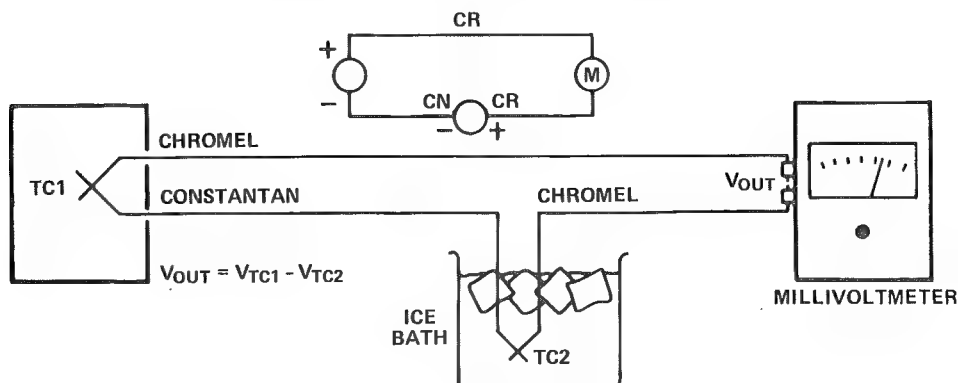
function of temperature. In general, these voltages are small. The following table lists a number of standard thermocouples, their useful temperature range, and the voltage swing over that range; it can be seen that the average change of voltage with temperature ranges from 7 to about  $75\mu\text{V}/^\circ\text{C}$ .

## SOME COMMON THERMOCOUPLES

Junction Materials	Typical Useful Temp Range ( $^\circ\text{C}$ )	Voltage Swing Over Range (mV)	ANSI Designation
Platinum-6% Rhodium — Platinum-30% Rhodium	38 to 1800	13.6	B
Tungsten-5% Rhenium — Tungsten-26% Rhenium	0 to 2300	37.0	(C)
Chromel — Constantan	0 to 982	75.0	E
Iron — Constantan	-184 to 760	50.0	J
Chromel — Alumel	-184 to 1260	56.0	K
Platinum — Platinum-13% Rhodium	0 to 1593	18.7	R
Platinum — Platinum-10% Rhodium	0 to 1538	16.0	S
Copper — Constantan	-184 to 400	26.0	T

Since every pair of dissimilar metals in contact constitutes a thermocouple (including copper/solder, about  $3\mu\text{V}/^\circ\text{C}$  and Kovar/rhodium), and since a useful electrical circuit requires at least two contacts in series, measurements with thermocouples must be implemented in a manner which minimizes undesired contributions of incidental thermocouples and provides a suitable reference.

### SIMPLE TEMPERATURE MEASURING CIRCUIT USING AN ICE BATH AT THE REFERENCE JUNCTION. THERMOCOUPLE MEASUREMENTS ARE INHERENTLY DIFFERENTIAL.



Because thermocouples are low-level devices, signal conditioning is not a trivial matter. The millivolt-level signals call for low-drift relatively expensive electronics if resolutions better than  $1^\circ\text{C}$  are required. Linearity in many types is poor, but the relationships are predictable and repeatable, so either analog or digital techniques can be used for linearizing downstream.

Providing a suitable temperature reference and minimizing the effects of unwanted thermocouples may prove challenging. Techniques include physical references (ice-point cells at  $+0.01^\circ\text{C}$ , which are accurate and easy to construct but unwieldy to maintain); ambient-temperature reference junctions (acceptable so long as the ambient temperature range in the vicinity of the reference junction is smaller than the desired resolution of the temperature being measured); and electronic cold-junction compensators, which provide an artificial reference level and compensate for ambient temperature variations in the vicinity of the reference junction (this technique requires careful attention to both the electronics and the physical configuration at that location).

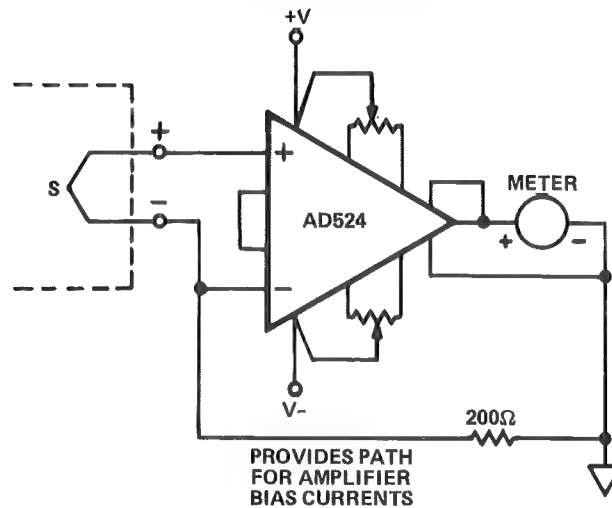
#### Ambient-Referenced Thermocouples

As we have noted, thermocouples require cold-junction compensation if they must resolve temperature changes with precision better than the ambient temperature range at the cold junction. However, for high-temperature measurements to within a few percent, the cold junction may often be profitably left at room ambient.

Suppose, for example, that a Type S thermocouple is used to measure temperatures of the order of  $1500^\circ\text{C}$  within a furnace, and the ambient temperature of the cold junction is  $25^\circ\text{C} \pm 15^\circ\text{C}$ . Since the sensitivity of the thermocouple is  $12\mu\text{V}/^\circ\text{C}$  at  $1500^\circ\text{C}$ , and a change from  $10^\circ\text{C}$  to  $40^\circ\text{C}$  at the cold junction produces a change of  $180\mu\text{V}$  in the net output voltage, the equivalent  $\Delta T$  at the active junction is  $15^\circ\text{C}$  for a full-scale change at the cold junction or 1% of  $1500^\circ\text{C}$ .

In the figure, an instrumentation amplifier is used to reject common-mode noise. If there is not conductive return path from the thermocouple, resistance may be used (as shown) to provide a path for the amplifiers bias currents.

## THERMOCOUPLE PREAMPLIFIER USING AD524



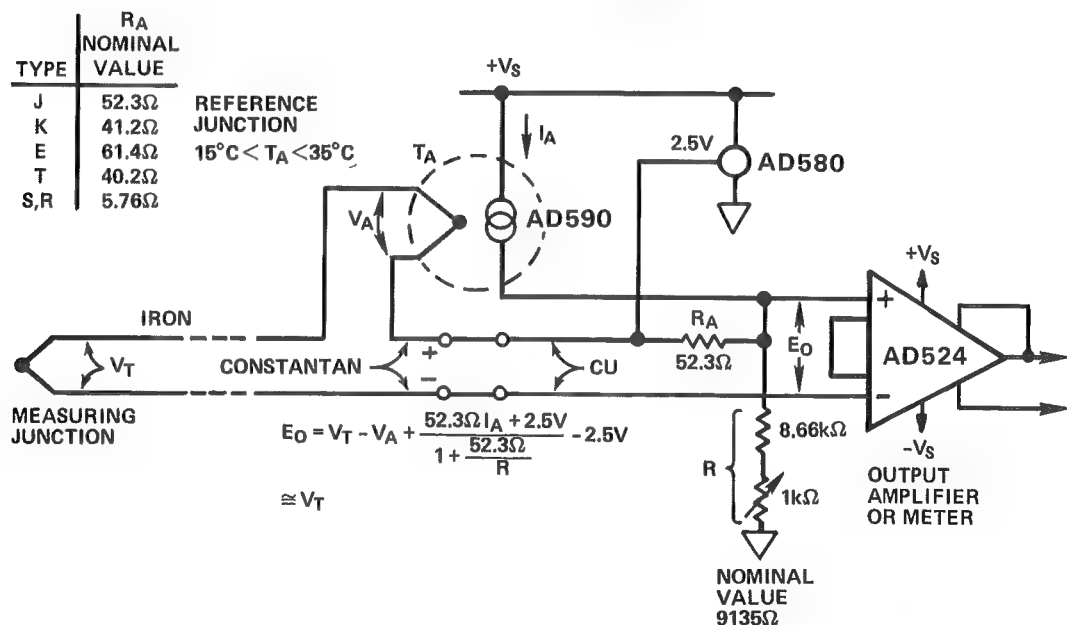
### Cold-Junction Compensation

If ambient temperature variation of the cold junction can cause significant error in the output of the thermocouple pair, there are two alternatives: maintain the cold junction at constant temperature, by some such technique as an ice bath or a thermostatically controlled oven, or subtract a voltage that is equal to the voltage developed across the cold junction at any temperature in the expected ambient range.

The figure shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple-iron(+)-constantan-is compensated for by a voltage developed in series by the temperature sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting  $R_T$  for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within  $\pm 0.5^\circ\text{C}$ , for temperatures between  $+15^\circ\text{C}$  and  $-35^\circ\text{C}$ . Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of  $R_T$  and  $R_A$ . If an instrumentation amplifier is used, gain and offset specifications should be appropriate for the temperature being measured, the required precision, and the sensitivity of the thermocouple employed.

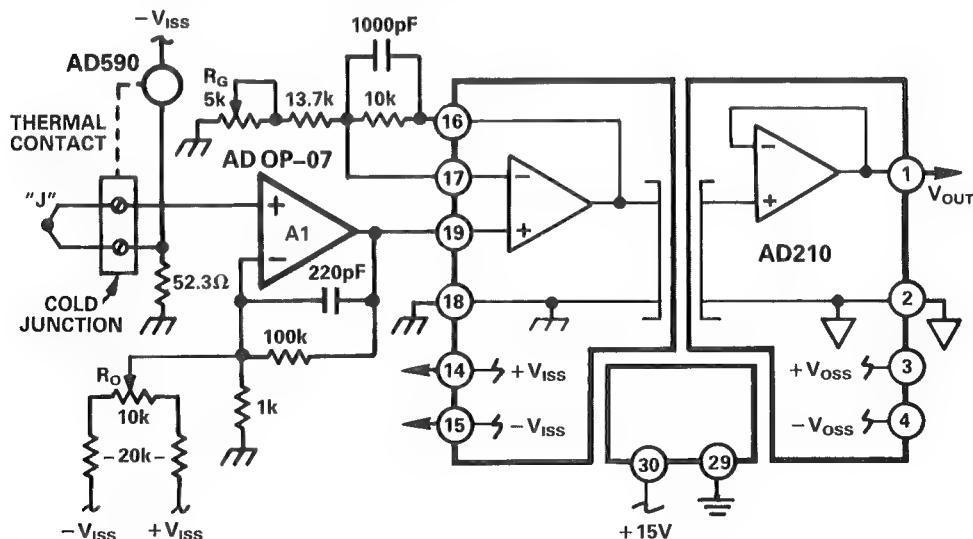
## COLD-JUNCTION COMPENSATION



### Isolated Temperature Measurement and Cold-Junction Compensation

The circuit shown below provides amplification, isolation and cold junction compensation for a standard J type thermocouple. The AD590 temperature sensor accurately monitors the input terminal (cold junction). Ambient temperature changes from 0 to +40°C sensed by the AD590, are cancelled out at the cold junction. Total circuit gain equals 183; 100 and 1.83, from A1 and the AD210 respectively. Calibration is performed by replacing the thermocouple junction with plain thermocouple wire and a millivolt source set at 0.0000V (0°C) and adjusting  $R_O$  for  $V_{OUT}$  equal to 0.000V. Set the millivolt source to +0.02185V (400°C) and adjust  $R_G$  for  $V_{OUT}$  equal to +4.000V. This application circuit will produce a nonlinearized output of about +10mV/°C for a 0 to +400°C range.

### ISOLATED THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION



## 7. SPECIALIZED SIGNAL CONDITIONING CIRCUITS

A large portion of this section has been dedicated to instrumentation and isolation amplifiers and as the title suggests, they are special purpose amplifiers. However, we have found that although they are a specialized class of amplifiers, instrumentation and isolation amplifiers can be quite versatile. They can be configured to interface with transducers such as strain gages, load cells, thermocouples, RTDs and thermistors to name a few. The drawback to this is that additional external circuitry is quite often required (i.e., cold junction compensation for thermocouple, or excitation voltage/current for bridge circuits).

This segment will cover a number of highly specialized signal conditioning circuits which will be complete solutions in specific transducer interfacing applications.

### MONOLITHIC THERMOCOUPLE SIGNAL CONDITIONER

## AD594/AD595 FEATURES

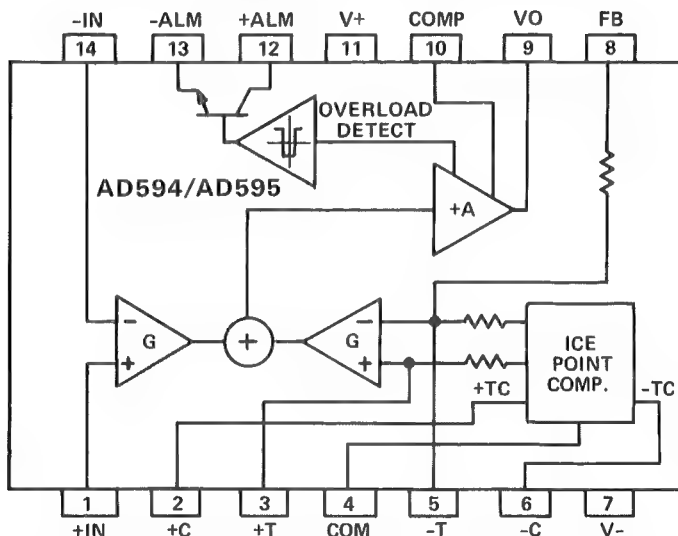
- Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples
- Low Impedance Voltage Output 10mV/°C
- Internal Ice Point Compensation
- Wide Power Supply Range: +5V to ±15V
- Low Power: 1mW
- Thermocouple Failure Alarm
- Laser Wafer Trimmed to 1°C Calibration Accuracy
- Set Point Mode Operation
- Self Contained Centigrade Thermometer Operation
- High Impedance Differential Input

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone centigrade transducer with a low-impedance voltage output.

### Functional Description

The AD594 behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in the figure below.

### AD594/AD595 BLOCK DIAGRAM



In normal operation the main amplifier output (pin 9) is connected to the feedback network (pin 8). Thermocouple signals applied to the floating input stage (pins 1 and 14) are amplified by gain  $G$  of the differential and are further amplified by gain  $A$  in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes the feedback to be driven to reduce this difference signal to a small value. The two differential amplifiers are made to match and have identical gains,  $G$ . As a result, the feedback signal that must be applied to the right hand differential amplifier will precisely match the thermocouple input signal when the difference signal has been reduced to zero. The feedback network is trimmed so that the effective gain to the output results in a voltage of  $10\text{mV}/^{\circ}\text{C}$  of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right-hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD594/AD595. This signal disturbs the differential input so that the amplifier output must adjust to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also  $10\text{mV}/^{\circ}\text{C}$ . As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between  $0^{\circ}\text{C}$  and the AD594/AD595 temperature. If the thermocouple reference junction is maintained at the AD594/AD595 temperature, the output of the AD594/AD595 will correspond to the reading that would have been obtained from amplification of a signal from a thermocouple referenced to an ice bath.

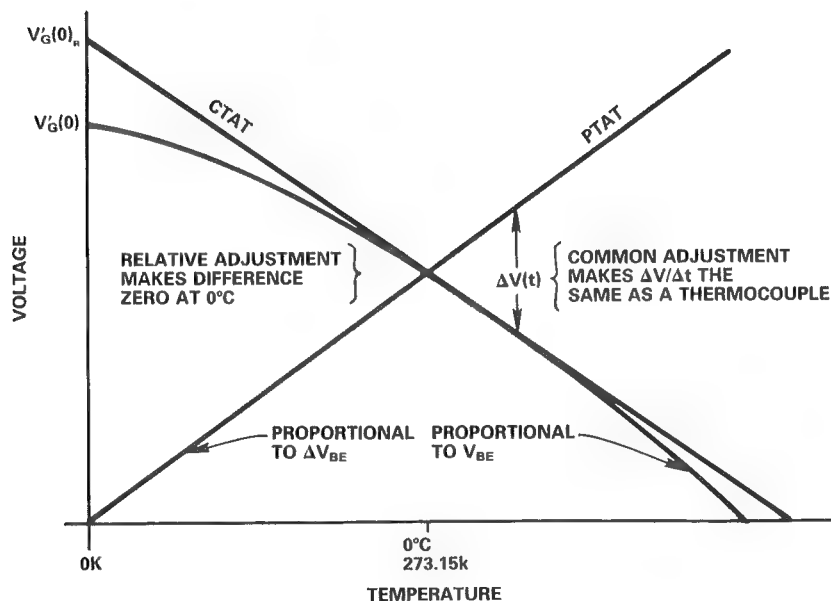
In order to operate properly the AD594/AD595 must have the thermocouple input within both the normal mode signal and common-mode operating range. A normally connected thermocouple within the common-mode operating range will meet these requirements. If one or both thermocouple input terminals are opened, however, an amplifier overload will result. The AD594/AD595 includes an input overload detector which switches on an alarm "transistor". This "transistor" is actually a current limited output buffer, but can be used, up to the limit as a switch transistor for either pull-up or pull-down operation of external alarms.

### Cold Junction Reference Compensation

It is commonly known that the characteristics of bipolar junction transistors are temperature sensitive, and it is a usual object of linear design to suppress this sensitivity. In the case of the AD594/AD595, however, certain well behaved and repeatable temperature dependent parameters are exploited to produce the cold junction compensation voltage. When two transistors are operated at different emitter current densities, the difference in their base-emitter voltages will be *proportional to absolute temperature* or PTAT. The base-emitter voltage of a single transistor falls with rising temperature in a way that can be extrapolated to a known voltage at absolute zero. This voltage *complement* a PTAT voltage with respect to the known bandgap voltage and is referred to as CTAT.

Although these two voltages are predictably related to absolute temperature, their difference can be related to Celsius temperature as shown below.

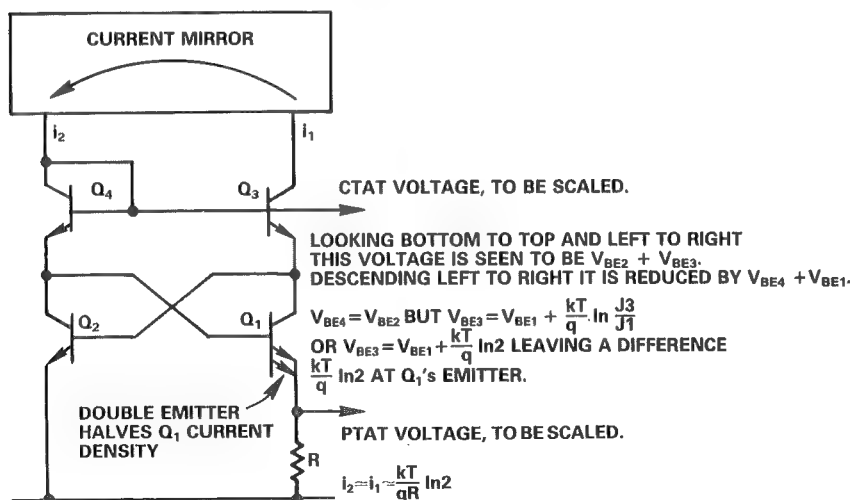
### ICE POINT COMPENSATION FROM THE DIFFERENCE OF A PTAT AND A CTAT VOLTAGE



Two temperature sensitive voltages can be derived from the transistor base-emitter characteristics and can be scaled so that their difference approximates the output of an ice referenced thermocouple measuring the IC temperature. This difference is zero at zero Celsius and increases more-or-less linearly with temperature. These voltages are produced by four transistors in the AD594/AD595. A current mirror is used to force a pair of series connected transistors (Q2, Q4 in the figure below) to operate at the same current as another series connected pair (Q1, Q3). Three of these transistors are the same size and therefore operate at equal current densities. Consequently, they have the same base-emitter voltage. The fourth transistor is larger than the others so that at the same current it operates at lower current density. This implies that it has a lower base-emitter voltage. The base-emitter junctions of the four transistors connect in a loop which is completed by a resistor. Two of the voltages are connected to subtract from the others so that the net voltage across resistor is just the difference between the base-emitter voltages of the differently sized transistors.

As noted before, this voltage will be PTAT and is scaled to the proper magnitude by a thin film network in the AD594/AD595. It is also possible to extract the sum of the two base-emitter voltages from this loop. This sum is CTAT and when properly scaled makes up the other temperature sensitive voltage for the Ice Point Compensation.

### A CROSS-CONNECTED TRANSISTOR QUAD PROVIDES CTAT VOLTAGE IN THE FORM OF $2V_{BE}$ s AND PTAT VOLTAGE FROM THE DIFFERENCE OF $V_{BE}$ s.



## Applications

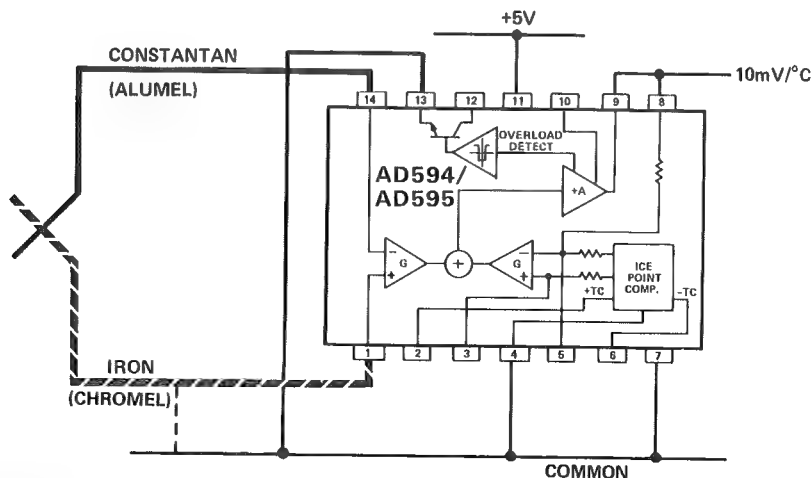
### Single Supply Operation

The AD594/AD595 is completely self contained with the interconnections shown below and will provide a direct output from type J and K thermocouples measuring from 0 to +300°C. The measuring thermocouple wires connect to pins 1 and 14 either directly or through intervening connections. The connections at which the thermocouple wires terminate form the reference junction. This junction should be kept at the same temperature as the AD594/AD595 since this is the junction compensated by the ice point reference in the AD594/AD595. If the thermocouple is not directly connected to pins 1 and 14, the intervening connections must both be made of the same material.

In this single supply application the V- connection at pin 7 is strapped to power and signal common, pin 4. When the alarm is unused, pin 13 must connect to either pin 4 and pin 7 (common or V-). The positive 5 volt supply connects to pin 11. Any convenient supply voltage from +5 to +30 volt may be used, however, the lower the supply voltage the lower the power consumption. It is important to minimize power consumption so that self heating of the circuit can be neglected.

The output is taken from pin 9, with the precalibrated feedback network (pin 8) strapped to the output to provide a 10mV/°C nominal output scale.

### BASIC CONNECTION, SINGLE SUPPLY OPERATION



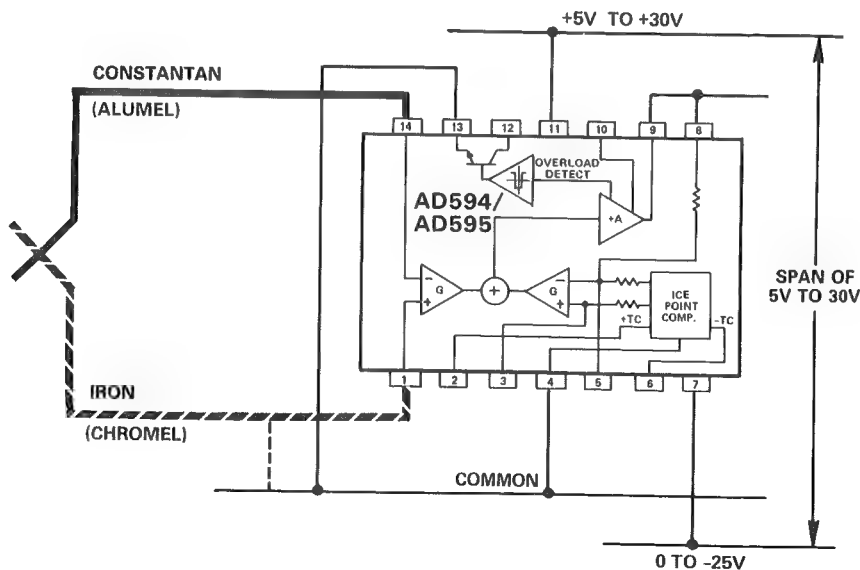
### Dual Supply Operation

The AD594/AD595 requires dual supplies when operating with thermocouples at negative temperatures in order to allow the output voltage to assume negative values.

As shown in the figure below, the AD594/AD595 can operate on a total supply span between pins 11 and 7 from 5 to 30 volts. Also, at least 5 volts is required between pins 11 and 4 for proper operation of the circuit.

Since the output can swing to within 2 volt of the positive supply, a +15 volt supply will allow operation of the AD595 circuit at the maximum recommended type K thermocouple temperature of 1250°C. A negative

### DUAL SUPPLY OPERATION



These flexible power supply requirements allow the AD594/AD595 to be included in most systems without the need for special power supplies or level translators.

The AD594/AD595 contain a temperature reference which is internally offset to zero Celsius for use as cold junction compensation for the thermocouple. Without the thermocouple attached, this reference indicates the temperature of the IC and the self-contained fixed-gain amplifier can be made to scale up this signal for a 10mV/°C output. This arrangement as shown is a three-terminal (voltage output) temperature sensor referred to zero. Note that if negative temperature indications are desired, a negative supply should be connected to pin 7 of the device.

Extracting the cold junction compensation voltage is possible using the circuit shown below. This voltage provides a low impedance drive signal for compensating one or more reference junctions that are at the same ambient temperature as the AD594/AD595.

**AD594: OUTPUT**  
52  $\mu\text{V}/^\circ\text{C}$

**AD595: OUTPUT**  
40  $\mu\text{V}/^\circ\text{C}$

**ICE POINT COMPENSATION VOLTAGE FOR TYPE J/K AT AMBIENT TEMP.**

**AD594/AD595**

**OVERLOAD DETECT**

**ICE POINT COMP.**

**+TC**

**-TC**

**CONNECT NEGATIVE SUPPLY FOR NEGATIVE OUTPUT WHEN  $V_A = 0$**

**V-**

**10k $\Omega$**

**$\approx 10\text{k}\Omega$  (ADD FOR NEGATIVE TEMPERATURES IF  $V_A > 0$ )**

**100 $\Omega$**

**+5V**

**V<sub>A</sub>**

**(ZERO TO + CM RANGE)**



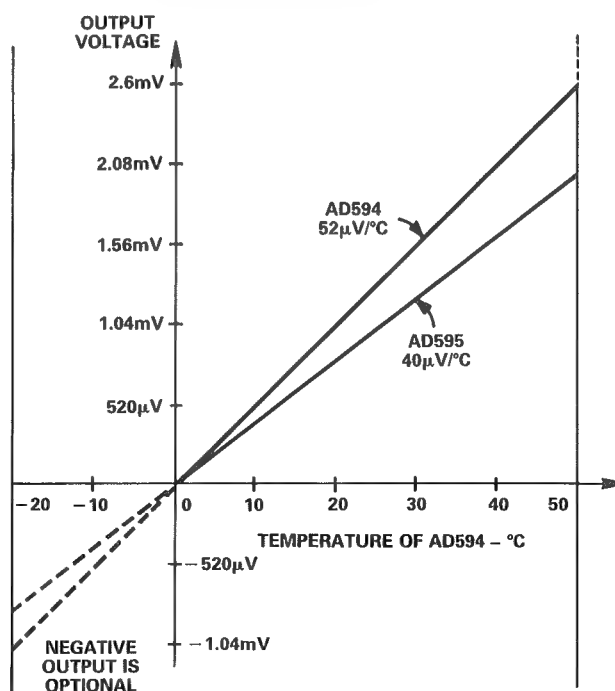
In practice, the feedback path at pin 8 is grounded, and the main circuit's control loop is completed by way of the thermocouple inputs (at pins 1 and 14). The exact values of the feedback resistors are not critical, since their only function is to frequency stabilize the loop by providing some attenuation in the feedback path.

Moreover, since the signal is derived across a differential input it may be either ground referenced or referred to an arbitrary voltage ( $V_a$ ) within the common-mode range of the amplifier.

A positive  $V_a$  voltage will permit the output amplifier to be negative with respect to the compensation point and provide negative Celsius temperatures.

The figure below illustrates output voltages versus temperature with factory calibrated compensations of  $52\mu\text{V}/^\circ\text{C}$  and  $40\mu\text{V}/^\circ\text{C}$  from the AD594 and AD595 respectively.

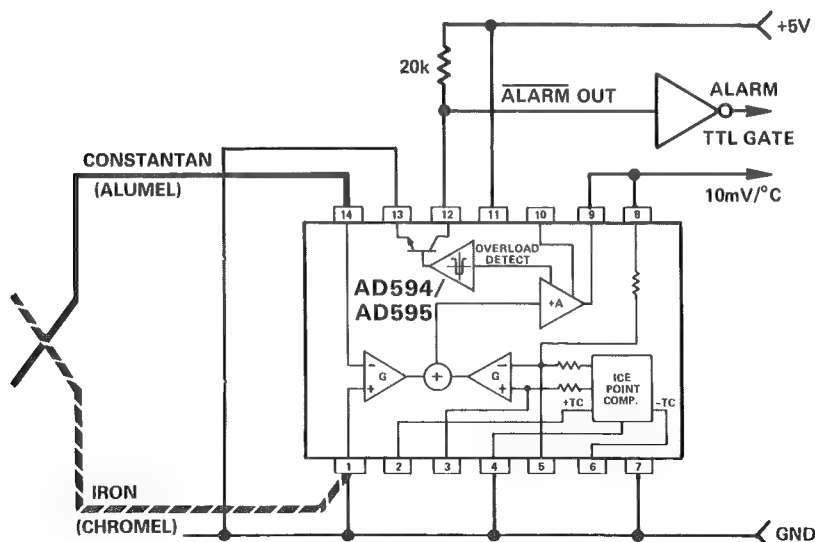
### ICE POINT COMPENSATION VOLTAGE VS. TEMPERATURE



### Alarm Circuit

In all applications of the AD594/AD595 the  $-\text{ALM}$  connection, pin 13, should be constrained so that it is not more positive than  $(V+) - 4\text{V}$ . This can be most easily achieved by connecting pin 13 to either common at pin 4 or  $V-$  at pin 7. For most applications that use the alarm signal, pin 13 will be grounded and the signal will be taken from  $+\text{ALM}$  on pin 12. A typical application is shown below.

### USING THE ALARM TO DRIVE A TTL GATE ("GROUNDED" EMITTER CONFIGURATION)

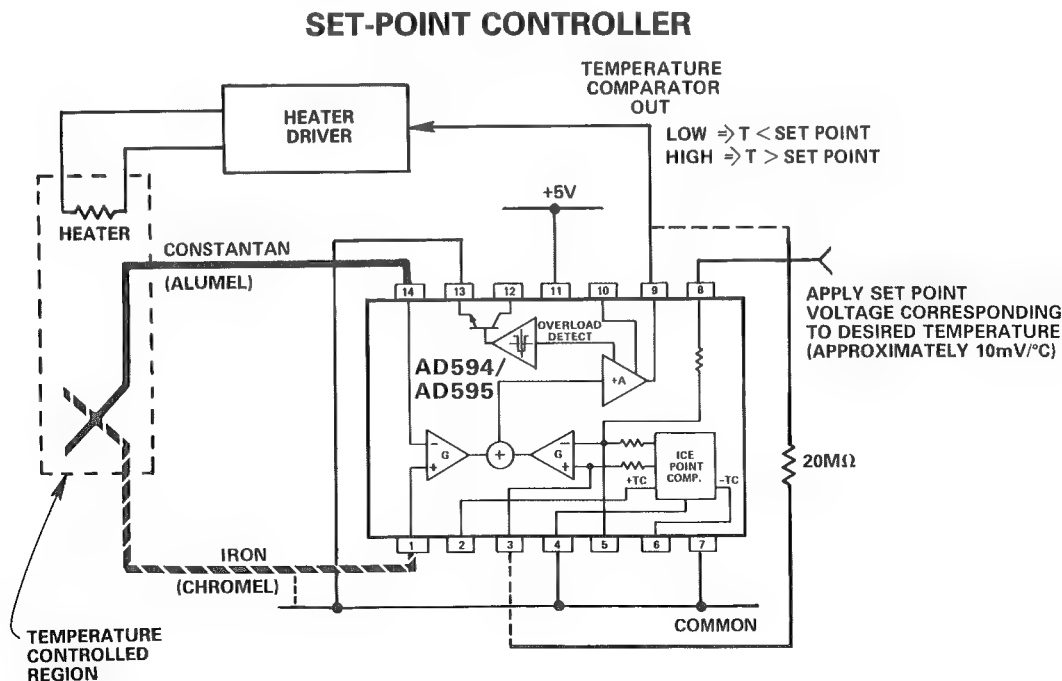


In this configuration the alarm transistor will be off in normal operation and the 20K pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM pin will be driven low. As shown above, this signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

The output alarm transistor is current limited to 20mA so a series limiting resistor is not required. The transistor, however, will operate in a high dissipation mode and the temperature of the circuit will rise well above ambient. The cold junction compensation will be affected whenever the alarm circuit is activated. The time required for the chip to return to ambient temperature will depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment and the alarm duration.

### Set-Point Controller

The AD594/AD595 can readily be connected as a set-point controller as shown below.



The thermocouple is used to sense the unknown temperature and provide a thermal EMF to the input of the AD594/AD595. The signal is cold junction compensated, amplified to 10mV/°C and compared to an external set-point voltage applied by the user to the feedback resistor at pin 8. If the set-point temperature range is within the operating range (−55°C to +125°C) of the AD594/AD595, the chip can be used as the transducer for the circuit by shorting the inputs together and utilizing the nominal calibration of 10mV/°C. This is analogous to the centigrade thermometer configuration as shown previously.

In operation if the set-point voltage is above the measurement voltage the output swings low to approximately zero volts. Conversely, when the temperature rises above the set-point voltage the output switches to the positive limit to about 4 volts with a +5 volt supply. The figure shows the set-point comparator configuration complete with a heater element driver circuit being controlled by the AD594/AD595 toggled output. Hysteresis can be introduced by injecting a current into the positive input of the feedback amplifier when the output is toggled high. With an AD594, about 200nA into the +T terminal provides 1°C of hysteresis. When using a single +5 volt supply with an AD594, a 20MΩ resistor from  $V_O$  to +T will supply the 200nA of current when the output is forced high (about 4V). To widen the hysteresis band, decrease the value of the positive feedback resistance connected to  $V_O$ .

## AD693 FEATURES

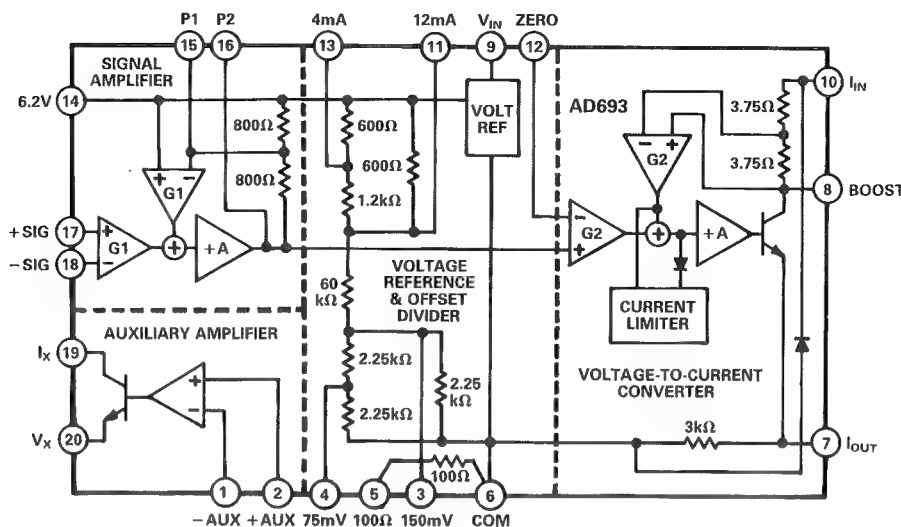
**Instrumentation Amplifier Front End**  
**Loop-Powered Operation**  
**Precalibrated 30mV or 60mV Input Spans**  
**Independently Adjustable Output Span and Zero**  
**Precalibrated Output Spans:** 4-20mA Unipolar  
   0-20mA Unipolar  
    $12 \pm 8$ mA Bipolar  
**Precalibrated 100 $\Omega$  RTD Interface**  
**6.2V Reference with Up to 3.5mA of Current Available**  
**Uncommitted Auxiliary Amp for Extra Flexibility**  
**Optional External Pass Transistor to Reduce Self-Heating Errors**

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4-20mA, two-wire current loop. An on-chip reference and auxiliary amplifier are provided for transducer excitation. Alternatively, the device may be locally powered for three-wire applications when 0-20mA operation is desired.

## Functional Description

The operation of the AD693 can be understood by dividing the circuit into four functional parts as shown below. First, an instrumentation amplifier front-end buffers and scales the low-level input signal. This amplifier drives the second section, a V/I converter, which provides the 4-to-20mA loop current. The third section, a voltage reference and resistance divider, provides application voltages for setting the various "live zero" currents. In addition to these three main sections, there is an on-chip auxiliary amplifier which can be used for transducer excitation.

## AD693 FUNCTIONAL BLOCK DIAGRAM

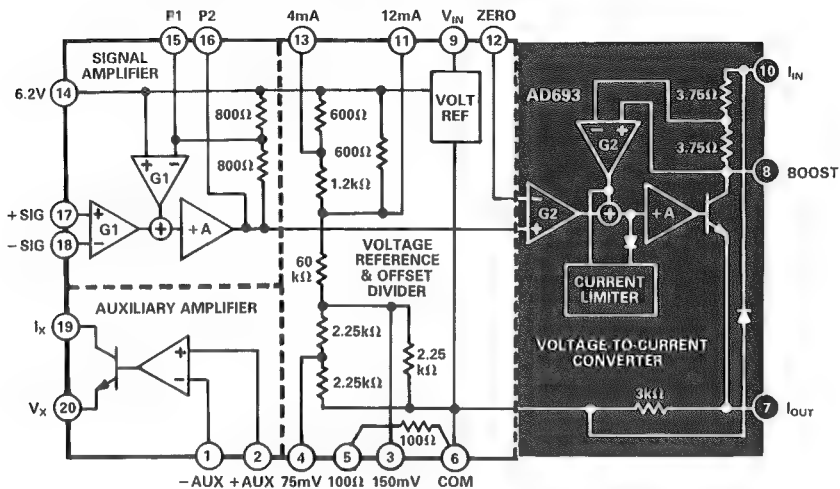


## Voltage-to-Current (V/I) Converter

The output NPN transistor for the V/I section sinks loop current when driven by a high gain amplifier at its base. The input for this amplifier is derived from the difference between the input signal and the loop current sampling resistor between  $I_{IN}$  and Boost. The signal across this resistor is compared to the input of the left preamp and servos the loop current until both signals are equal. Accurate voltage-to-current transformation is thereby assured. The preamplifiers employ a special design which allows the active feedback amplifier to operate from the most positive point in the circuit,  $I_{IN}$ .

The V/I stage is designed to have a nominal transconductance of 0.2666 A/V. Thus, a 75mV signal applied to the inputs of the V/I (pin 16, noninverting; pin 12, inverting) results in a full-scale output current of 20mA.

## AD693 VOLTAGE-TO-CURRENT CONVERTER



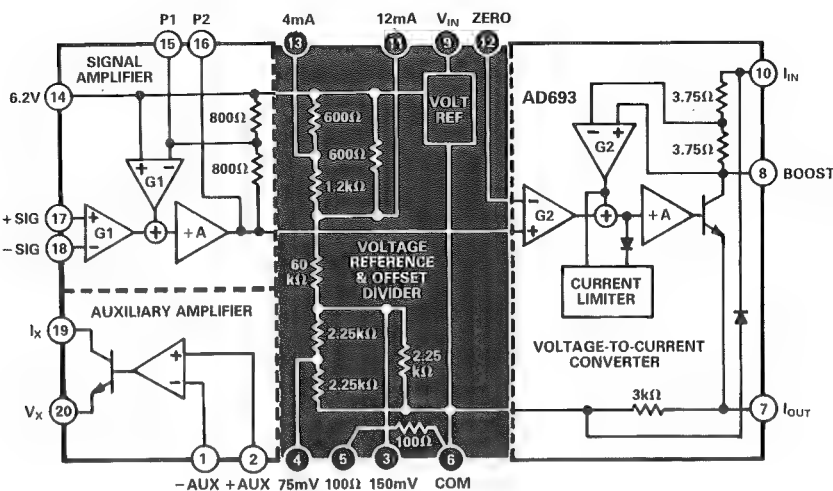
### Voltage Reference and Divider

A stabilized bandgap voltage reference and laser-trimmed resistor divider provide for both transducer excitation as well as precalibrated offsets for the V/I converter. When not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

The 4mA and 12mA taps on the resistor divider correspond to  $-15\text{mV}$  and  $-45\text{mV}$ , respectively, and result in a live zero of 4mA or 12mA of loop current when connected to the V/I converter's inverting input (pin 12). Arranging the zero offset in this way makes the zero signal output current independent of input span. When the input to the signal amp is zero, the noninverting input of the V/I is at 6.2V.

Since the standard offsets are laser trimmed at the factory, adjustment is seldom necessary except to accommodate the zero offset of the actual source.

## AD693 VOLTAGE REFERENCE & OFFSET DIVIDER

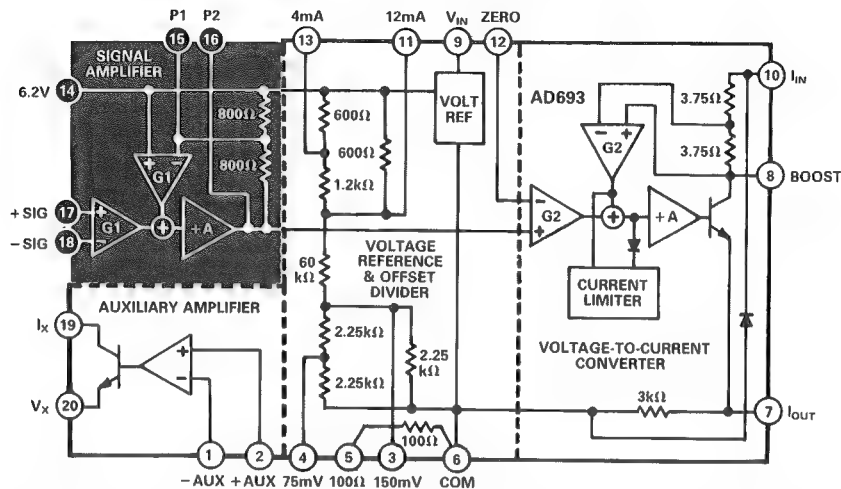


### Signal Amplifier

The signal amplifier is an instrumentation amplifier used to buffer and scale the input to match the desired span. Inputs applied to the signal amplifier (at pins 17 and 18) are amplified and referred to the 6.2V reference output in much the same way as the level translation occurs in the V/I converter. Signals from the two preamplifiers are subtracted, the difference is amplified, and the result is fed back to the upper preamp to minimize the difference. Since the two preamps are identical, this minimum will occur when the voltage at the upper preamp just matches the differential input applied to the signal amplifier at the left.

Since the signal which is applied to the V/I is attenuated across the two 800Ω resistors before driving the upper preamp, it will necessarily be an amplified version of the signal applied between pins 17 and 18. By changing this attenuation, you can control the span referred to the signal amplifier. To illustrate: a 75mV signal applied to the V/I results in a 20mA loop current. Nominally, 15mV is applied to offset the zero to 4mA leaving a 60mV range to correspond to the span. And, since the nominal attenuation of the resistors connected to pins 16, 15 and 14 is 2.00, a 30mV input signal will be doubled to result in 20mA of loop current.

## AD693 SIGNAL AMPLIFIER



Shorting pins 15 and 16 results in unity gain and permits a 60mV input span. Other choices of span may be implemented with user supplied resistors to modify the attenuation.

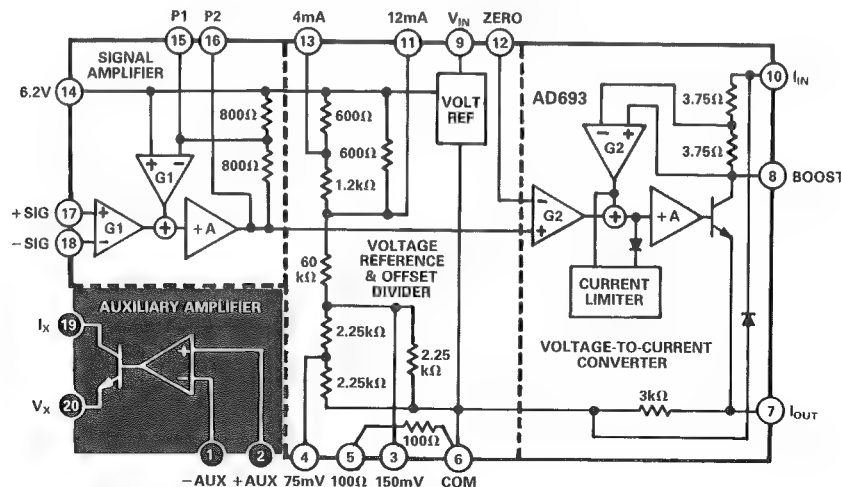
The signal amplifier is specially designed to accommodate a large common-mode range. Common-mode signals up to and beyond the 6.2V reference are easily handled as long as  $V_{IN}$  is sufficiently positive. The signal amplifier is biased with respect to  $V_{IN}$  and requires about 3.5 volts of headroom. The extended range will be useful when measuring sensors driven, for example, by the auxiliary amplifier which may go above the 6.2V potential. In addition, the PNP input stage will continue to operate normally with common-mode voltages of several hundred millivolts, negative, with respect to common. This feature accommodates self-generating sensors, such as thermocouples, which may produce small negative normal-mode signals as well as common-mode noise on "grounded" signal sources.

### Auxiliary Amplifier

The auxiliary amplifier is included in the AD693 as a signal conditioning aid. It can be used as an op amp in noninverting applications and has special provisions to provide a controlled current output. Designed with a differential input stage and an unbiased Class A output stage, the amplifier can be resistively loaded to common with the self-contained 100Ω resistor or with a user supplied resistor.

As a functional element, the auxiliary amplifier can be used in dynamic bridges and arrangements such as RTD signal conditioning. It can be used to buffer, amplify and combine other signals with the main signal amplifier. The auxiliary amplifier can also provide other voltages for excitation if the 6.2V of the reference is unsuitable. Configured as a simple follower, it can be driven from a user supplied voltage divider or the precalibrated outputs of the AD693 divider (pins 3 and 4) to provide a stiff voltage output at less than the 6.2V level, or by incorporating a voltage divider as feedback around the amplifier, one can gain-up the reference to levels higher than 6.2V. If large positive outputs are desired,  $I_X$ , the auxiliary amplifier output current supply, should be strapped to either  $V_{IN}$  or Boost. Like the signal amplifier, the auxiliary amplifier requires about 3.5V of headroom with respect to  $V_{IN}$  at its input and about 2V of difference between  $I_X$  and the voltage to which  $V_X$  is required to swing.

## AD693 AUXILIARY AMPLIFIER



The output stage of the auxiliary amplifier is actually a high gain Darlington transistor where  $I_X$  is the collector and  $V_X$  is the emitter. Thus, the auxiliary amplifier can be used as a V/I converter when configured as a follower and resistively loaded.  $I_X$  functions as a high-impedance current source whose current is equal to the voltage at  $V_X$  divided by the load resistance. For example, using the onboard  $100\Omega$  resistor and the  $75\text{mV}$  or  $150\text{mV}$  application voltages, either a  $750\Omega\text{A}$  or a  $1.5\text{mA}$  current source can be set up for transducer excitation.

The  $I_X$  terminal has a voltage compliance within  $2\text{V}$  of  $V_X$ . If the auxiliary amplifier is not used, then pin 2, the noninverting input, should be grounded.

### Reverse Voltage Protection Feature

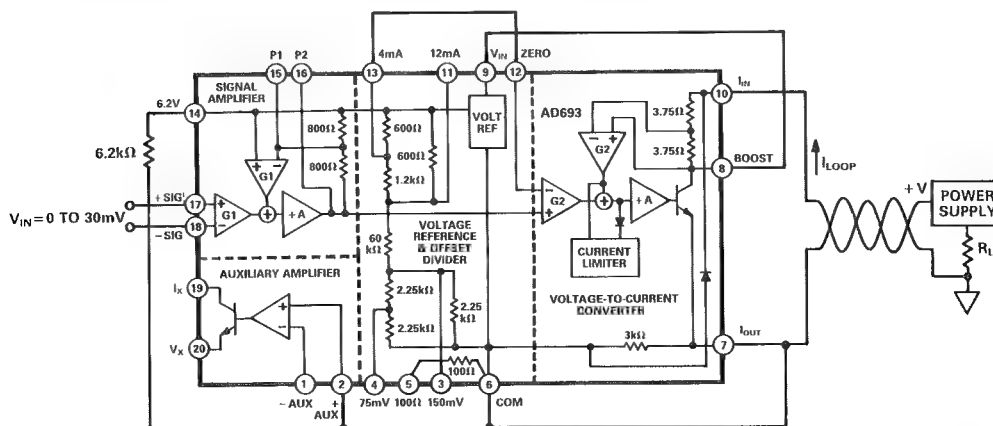
In the event of a reverse voltage being applied to the AD693 through a current-limited loop (limited to  $200\text{mA}$ ), an internal shunt diode protects the device from damage. This protection mode avoids the compliance voltage penalty which results from a series diode that must be added if reversal protection is required in high current loops.

### Applications

#### Basic Operation

The figure below shows the minimal connections for basic operation:  $0\text{--}30\text{mV}$  input span,  $4\text{--}20\text{mA}$  output span in the two-wire, loop-powered mode. Loop power may be  $+12$  to  $+36$  volts.

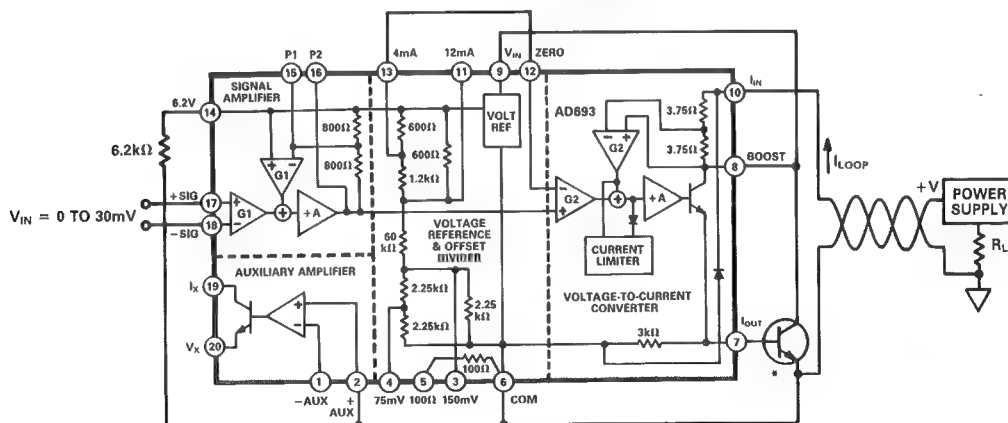
### MINIMAL CONNECTION FOR $0\text{--}30\text{mV}$ UNIPOLAR INPUT, $4\text{--}20\text{mA}$ OUTPUT



### Using an External Pass Transistor

The emitter of the NPN output section,  $I_{OUT}$ , of the AD693 is usually connected to common and the negative loop connection (pins 6 and 7). Provision has been made to reconnect  $I_{OUT}$  to the base of a user supplied NPN transistor as shown below. This permits the majority of the power dissipation to be moved off chip to enhance performance, improve reliability, and extend the operating temperature range. An internal hold-down resistor of about  $3\text{K}$  is connected across the base emitter of the external transistor.

### USING AN EXTERNAL PASS TRANSISTOR TO MINIMIZE SELF-HEATING ERRORS



\*THE AD693 IS TESTED WITH A 2N3440 AT THE FACTORY. RECOMMENDED TRANSISTOR TYPES ARE GIVEN IN THE DATA SHEET TEXT.

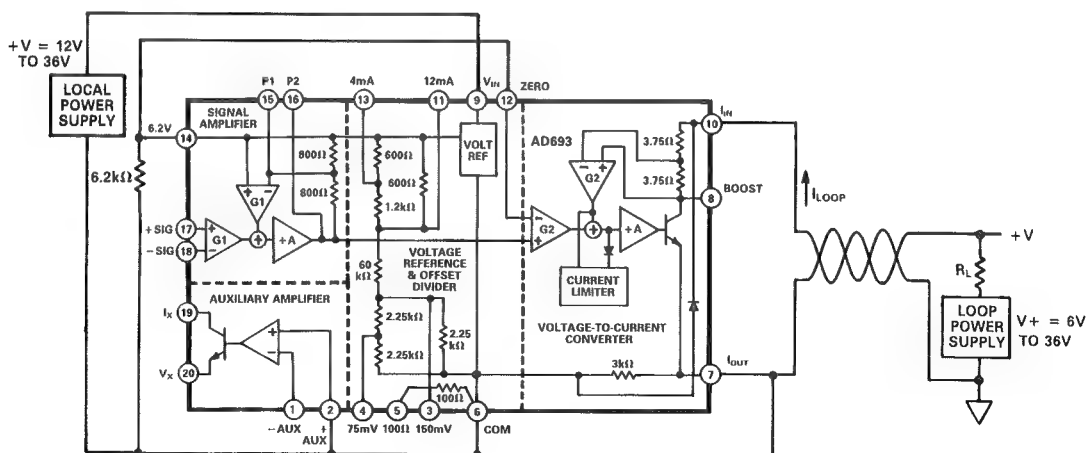
The external pass transistor selected should have a  $BV_{CEO}$  greater than the intended supply voltage with a sufficient power rating for continuous operation with 25mA current at the supply voltage.  $F_T$  should be in the 10MHz to 100MHz range and  $\beta$  should be greater than 10 at a 20mA emitter current. Some transistors that meet this criteria are the 2N1711 and 2N2219A. Heat sinking the external pass transistor is suggested.

The pass transistor option may also be employed for other applications as well. For example,  $I_{OUT}$  can be used to drive an LED connected to common, thus providing a local monitor of loop fault conditions without reducing the minimum compliance voltage.

### Local-Powered Operation

The AD693 is designed for local-powered, three-wire systems as well as two-wire loops. All its usual ranges are available in three-wire operation, and in addition, the 0-to-20mA range can be used. The 0-20mA convention offers slightly more resolution and may simplify the loop receiver, two reasons why it is sometimes preferred.

## LOCAL POWERED OPERATION WITH 0-20mA OUTPUT

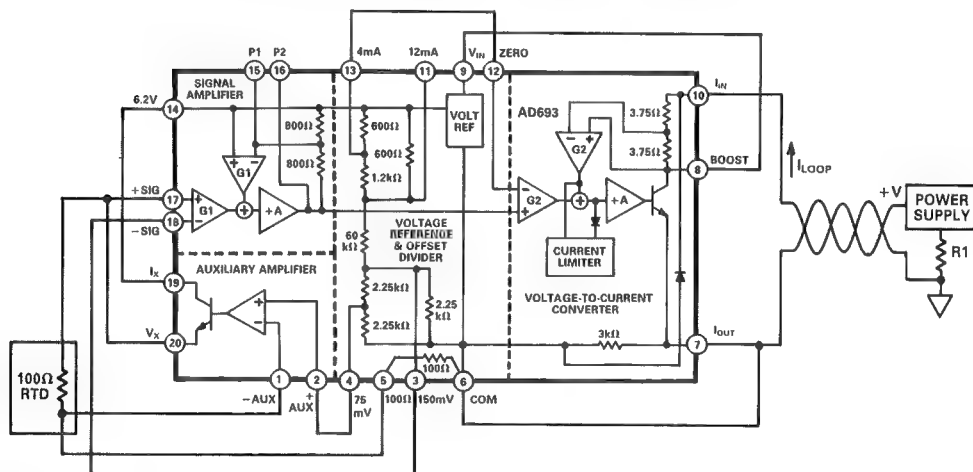


The arrangement, illustrated above, results in a 0-20mA transmitter where the precalibrated span is 37.5mV. Connecting P1 to P2 will double the span to 75mV. Sensor input and excitation is unchanged from the two-wire mode except for the 25% increase in span. Many sensors are ratiometric so that an increase in excitation can be used instead of a span adjustment.

In the local-powered mode, increases in excitation are made easier. Voltage compliance at the  $I_{IN}$  terminal is also improved; the loop voltage may be permitted to fall to 6 volts at the AD693, easing the tradeoff between loop voltage and loop resistance. Note that the load resistor,  $R_L$ , should meter the current into pin 10,  $I_{IN}$ , so as not to confuse the loop current with the local supply current.

### Interfacing Platinum RTDs

## 0-TO-104°C DIRECT THREE-WIRE 100Ω RTD INTERFACE, 4-20mA OUTPUT



The AD693 has been specially configured to accept inputs from 100Ω Platinum RTDs (Resistance Temperature Detectors). Referring to the above circuit, the RTD and the temperature stable 100Ω resistor form a feedback network around the auxiliary amplifier resulting in a noninverting gain of  $(1 + R_t/100\Omega)$ , where  $R_t$  is the temperature dependent resistance of the RTD. The noninverting input of the auxiliary amplifier (pin 2) is then

driven by the 75mV signal from the voltage divider (pin 4). When the RTD is at 0, its 100 $\Omega$  resistance results in an amplifier gain of +2 causing  $V_X$  to be 150mV. The signal amplifier compares this voltage to the 150mV output (pin 3) so that zero differential signal results. As the temperature (and therefore, the resistance) of the RTD increases,  $V_X$  will likewise increase according to the gain relationship. The difference between this voltage and the zero degree value of 150mV drives the signal amp to modulate the loop current. The AD693 is precalibrated such that the full 4-20mA output span corresponds to 0 to 104°C range in the RTD. (This assumes the European Standard of  $\alpha = 0.00385$ ) A total of 6 precalibrated ranges for three-wire (or two-wire) RTDs are available using only the pin strapping options as shown below.

## PRECALIBRATED TEMPERATURE RANGE OPTIONS USING A EUROPEAN STANDARD 100 $\Omega$ RTD AND THE AD693

Temperature Range	Pin Connections
0 to +104°C	12 to 13
0 to +211°C	12 to 13, and 15 to 16
+25°C to +130°C	12 to 14
+51°C to +266°C	12 to 14, and 15 to 16
-50°C to +51°C	12 to 11
-100°C to +104°C	12 to 11 and 15 to 16

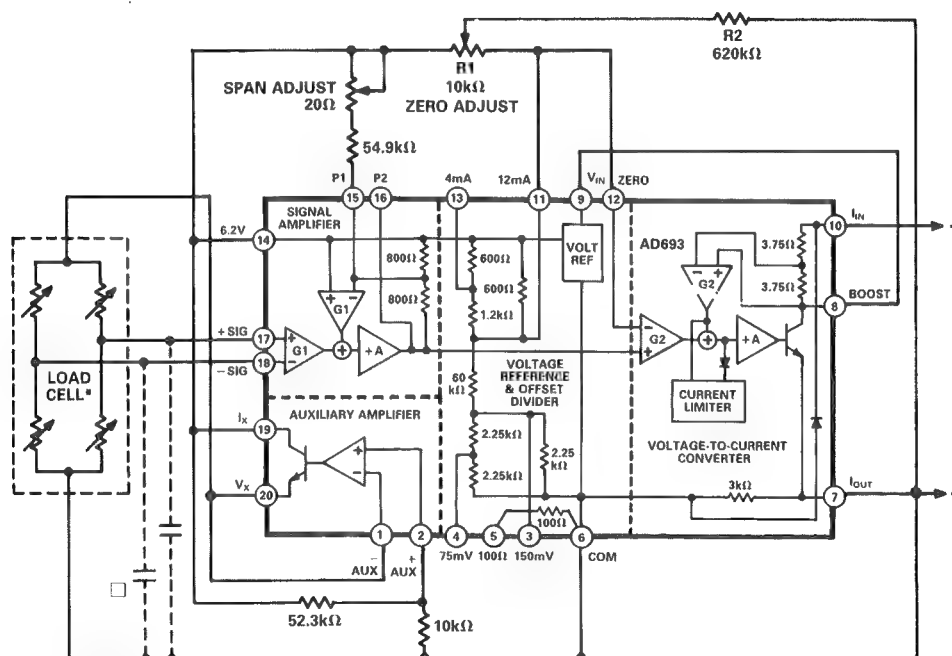
A variety of other temperature ranges can be realized by using different application voltages. For example, loading the voltage divider with a 1.5k $\Omega$  resistor from pin 3 to pin 6 (common) will approximately halve the original application voltages and allow for doubling of the range of resistance (and therefore, temperature) required to fill the two standard spans. Likewise, increasing the application voltages by adding resistance between pins 14 and 3 will decrease the temperature span.

The configuration for a three-wire RTD shown can accommodate two-wire sensors by simply joining pins 1 and 5 of the AD693.

### Interfacing Load Cells

The availability of the on-chip voltage reference, auxiliary amplifier and 3mA of excitation current make it easy to adapt the AD693 to a variety of load cells and strain gages.

## UTILIZING THE AUXILIARY AMPLIFIER TO DRIVE A LOAD CELL, 12mA $\pm$ 8mA OUTPUT



\*350 $\Omega$ , 2mV/V  
E.G., SENSOTEC MODEL 41  
AL DESIGN MODEL ALD-UTC

□ OPTIONAL INPUT FILTER  
(SEE TEXT)



The circuit above illustrates a generalized approach in which the full flexibility of the AD693 is required to interface to a low resistance bridge. For a high impedance transducer the bridge can be directly powered from the 6.2V reference.

Component values in this example have been selected to match the popular standard of 2mV/V sensitivity and 350Ω bridge resistance. Load cells are generally made for either tension and compression, or compression only; use of the 12mA zero tap allows for operation in the tension and compression mode. An optional zero adjustment is provided with values selected for ±2% FS adjustment range.

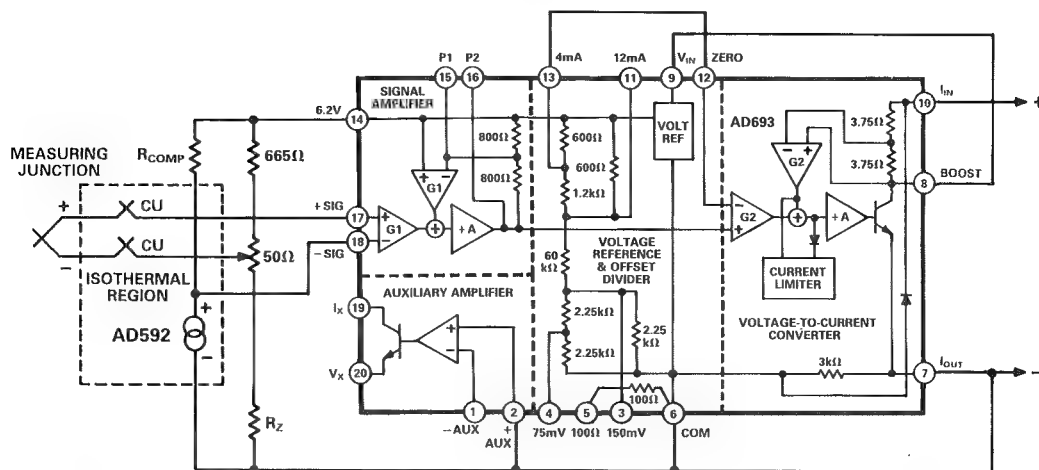
Because of the low resistance of most foil bridges, the excitation voltage must be low so as not to exceed the available 4mA zero current. About 1V is derived from the 6.2V reference and an external voltage divider; the auxillary amp is then used as a follower to make a stiff drive for the bridge. Similar applications with higher resistance sensors can use proportionally higher voltage.

Finally, to accommodate the 2mV/V sensitivity of the bridge, the full scale span of the signal amplifier must be reduced. Using the load cell in both tension and compression with 1V of excitation, therefore, dictates that the span be adjusted to 4mV. By substituting in the expression,  $R_{S1} = 400\Omega / [(30\text{mV}/\text{Span}) - 1]$ , the nominal resistance required to achieve this span is found to be 61.54Ω. Calculate the minimum resistance required by subtracting 10% from 61.54Ω to allow for the internal resistor tolerance of the AD693, leaving 55.38Ω. The standard value of 54.9Ω is used with a 20Ω potentiometer for full-scale adjustment.

### Thermocouple Interface

The AD693 can be used with several types of thermocouple inputs to provide a 4-20mA current loop output corresponding to a variety of measurement temperature ranges. Cold junction compensation (CJC) can be implemented using the AD590 or AD592 and a few resistors as shown below.

## THERMOCOUPLE INPUTS WITH COLD JUNCTION COMPENSATION



From the table below, simply choose the type of thermocouple and the appropriate average reference junction temperature to select values for  $R_{COMP}$  and  $R_Z$ . The CJC voltage is developed across  $R_{COMP}$  as a result of the AD592 1μA/K output and is added to the thermocouple loop voltage. The 50Ω potentiometer is biased by  $R_Z$  to provide the correct zero adjustment range appropriate for the divider and also translates the Kelvin scale of the AD592 to °Celsius. To calibrate the circuit, put the thermocouple in an ice bath (or use a thermocouple simulator set to 0) and adjust the potentiometer for a 4mA loop current.

## THERMOCOUPLE APPLICATION – COLD JUNCTION COMPENSATION TABLE

POLARITY	MATERIAL	TYPE	AMBIENT TEMP	RCOMP	RZ	30mV TEMP RANGE	60mV TEMP RANGE
+	IRON	J	25°	51.7Ω	301K	546°C	1035°C
−	CONSTANTAN		75°	53.6Ω	294K		
+	NICKEL-CHROME	K	25°	40.2Ω	392K	721°C	—
−	NICKEL-ALUMINUM		75°	42.2Ω	374K		
+	NICKEL-CHROME	E	25°	60.4Ω	261K	413°C	787°C
−	COPPER-NICKEL		75°	64.9Ω	243K		
+	COPPER	T	25°	40.2Ω	392K	USE WITH GAIN>2	
−	COPPER-NICKEL		75°	45.3Ω	340K		

The span of the circuit in °C is determined by matching the signal amplifier input voltage range to its temperature equivalent via a set of thermocouple tables referenced to 0°C. For example, the output of a properly referenced type J thermocouple is 60mV when the hot junction is at 1035°C. The table lists the maximum measurement temperature for several thermocouple types using the preadjusted 30mV and 60mV input ranges.

More convenient temperature ranges can be selected by determining the full-scale input voltages via standard thermocouple tables and adjusting the AD693 span. For example, suppose only a 300°C span is to be measured with a type K thermocouple. From a standard table, the thermocouple to a 16mA span at the output, a gain of 5 (or more precisely  $60\text{mV}/12.207\text{mV} = 4.915$ ) will be needed. To achieve the 12.207mV span a resistance of 270Ω is required from P1 to 6.2V. Adding a 50Ω potentiometer will allow ample adjustment range.

With the connection illustrated, the AD693 will give a full-scale indication with an open thermocouple.

## COMPLETE STRAIN GAGE AND BRIDGE TRANSDUCER SIGNAL CONDITIONERS

### 1B31 FEATURES

#### Low Cost

#### Complete Signal-Conditioning Solution

#### Small Package: 28-Pin Double DIP

#### Internal Half-Bridge Completion Resistors

#### Remote Sensing

#### High Accuracy

Low Drift:  $\pm 0.25\mu\text{V}/^\circ\text{C}$

Low Noise:  $0.3\mu\text{V}$  p-p

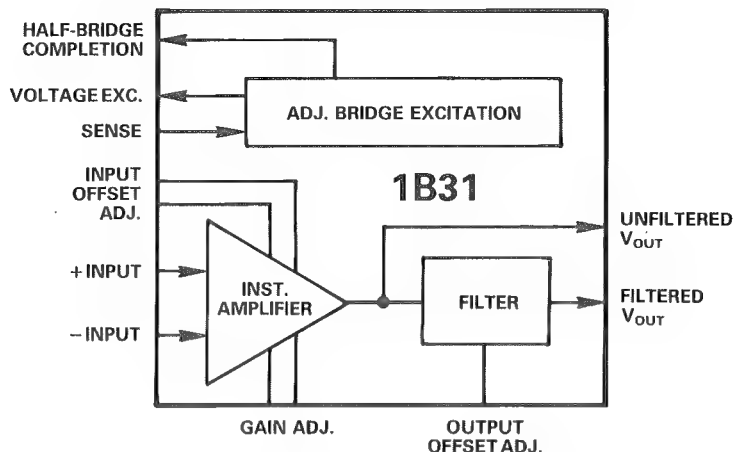
Low Nonlinearity:  $\pm 0.005\%$  max

High CMR: 140dB min (60Hz,  $G = 1000\text{V}/\text{V}$ )

Programmable Bridge Excitation: +4V to +15V

Adjustable Low Pass Filter:  $f_c = 10\text{Hz}$  to  $20\text{kHz}$

### 1B31 BLOCK DIAGRAM

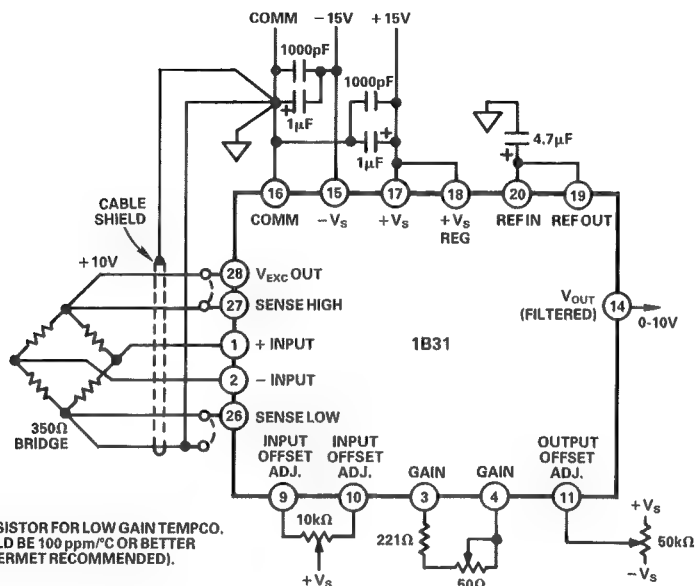


Model 1B31 is based on a two-stage amplifier design and an adjustable voltage regulator section, as shown above. The front end is a low noise, low drift, instrumentation amplifier (IA) that is optimized to amplify low level transducer signals (from 2mV full scale) riding an high common-mode voltages ( $\pm 9.5\text{V}$ ). The gain of the IA is programmed by a single resistor (1V/V to 2500V/V) and the input offset nulled by an external potentiometer across the offset adjust pins 9 and 10. The inverted signal ( $V_{-INPUT} - V_{+INPUT}$ ) is brought out to pin 8 for applications such as vibration and torque testing where the unfiltered output is required.

The signal is also fed to an inverting Butterworth filter with a fixed gain of  $-2\text{V}/\text{V}$ . This two-pole filter is preset with a 1kHz corner frequency which can be adjusted downwards to 10Hz by using two external capacitors or upwards to 20kHz by three resistors. This stage also provides a convenient means of adjusting output offset voltage ( $\pm 10\text{V}$ ) by connecting a 50kΩ potentiometer to pin 11.

The bridge excitation section is an adjustable output, regulated supply with an internally provided reference voltage (+6.8V). It is configured as a gain stage with the output preset at +10V. The excitation voltage is adjusted by connecting resistors between pins 21 and 26, and between pins 19 and 20. Sense lines are provided to compensate for lead-wire resistance by effectively bringing the leads into the feedback loop.

For half-bridge applications, two tracking thin film resistors ( $20\text{k}\Omega$ ,  $\pm 5\text{ppm}/^\circ\text{C}$  max) are connected from  $V_{\text{EXC OUT}}$  (pin 28) to SENSE LOW (pin 26).



## Basic Operation

The figure above shows the 1B31 configured for basic operation. The differential gain,  $G$ , is determined by the equation:

$$G = 1 + (80\text{k}\Omega/R_G)$$

where  $R_G$  is connected between the GAIN terminals (pins 3 and 4) of the 1B31. For best performance, a low temperature coefficient (5ppm/°C)  $R_G$  is recommended. For fine span adjustment, a 50Ω potentiometer may be connected in series with  $R_G$ .

Input offset can be nulled with a 10k $\Omega$  potentiometer between pins 9 and 10 and tapped to +V<sub>S</sub> (if not used leave pins open). The output can be offset over the  $\pm 10V$  range to compensate for dead load of source imbalance by using a 50k $\Omega$  potentiometer connected between the supply rails and tapped to pin 11 (pin 11 should be grounded if not used).

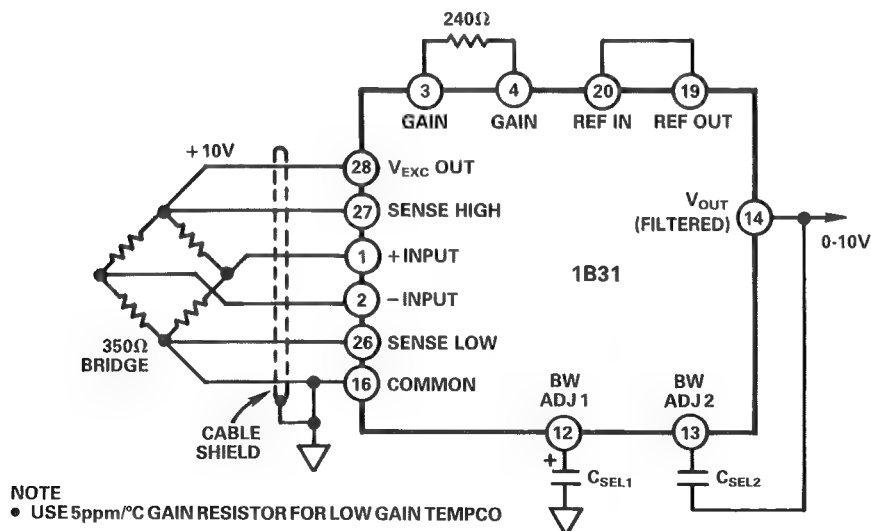
### Filter Cutoff Frequency Programming

The low pass filter cutoff frequency is internally set at 1kHz. It may be decreased from 1kHz by the addition of two external capacitors connected as shown below (from pin 12 to common and between pins 13 and 14). The values of capacitors required from a desired cutoff frequency,  $f_c$ , below 1kHz are obtained by the equations:

$$C_{SEL1} = 0.015 \mu F [(1 \text{ kHz} / f_C) - 1]$$

$$C_{SEL2} = 0.0022 \mu F [(1 \text{ kHz}/f_C) - 1]$$

## NARROW BANDWIDTH APPLICATION



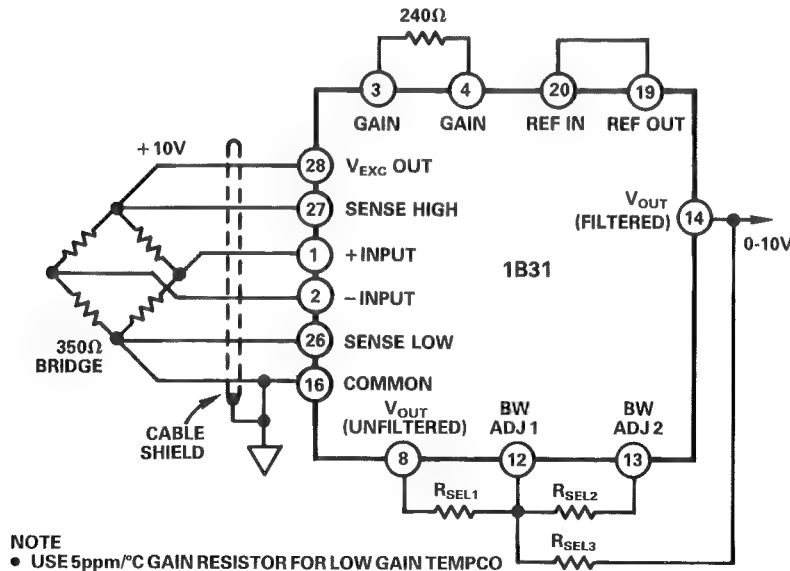
The cutoff frequency may also be increased from 1kHz to 20kHz by the addition of three external resistors, connected as shown in the circuit below. The equations for determining the resistor values are:

$$R_{SEL1} = 20k\Omega / [(f_C/1kHz) - 1]$$

$$R_{SEL2} = 16k\Omega / [(f_C/1kHz) - 1]$$

$$R_{SEL3} = 40k\Omega / [(f_C/1kHz) - 1]$$

### WIDE BANDWIDTH APPLICATION



The table below gives the nearest resistor and capacitor values for several common filter cutoff frequencies.

### FILTER CUTOFF FREQUENCY VS $R_{SEL}$ AND $C_{SEL}$

$f_C$ (Hz)	$C_{SEL1}$ ( $\mu F$ )	$C_{SEL2}$ ( $\mu F$ )	
10	1.5	0.2	
50	0.27	0.039	
100	0.15	0.02	
200	0.056	0.0082	
500	0.015	0.0022	
	$R_{SEL1}$ (k $\Omega$ )	$R_{SEL2}$ (k $\Omega$ )	$(R_{SEL3})$ (k $\Omega$ )
2000	20	16.2	40.2
5000	4.99	4.12	10.0
10000	2.21	1.78	4.42
20000	1.05	0.866	2.21

#### Voltage Excitation Programming

The excitation voltage is preset to +10V. To increase  $V_{EXC}$  up to +15V a resistor must be connected between EXC ADJ and SENSE LOW (pins 21 and 26) as shown below.

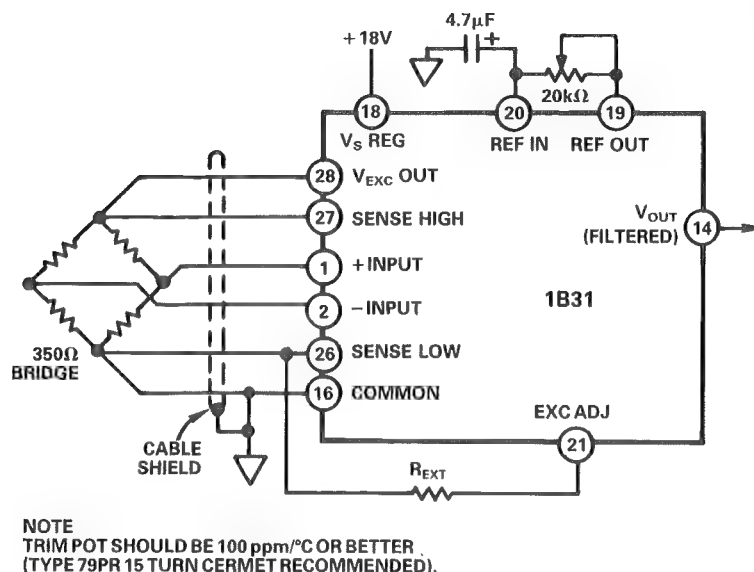
The + $V_S$  (REG) input (pin 18) must be raised to +18V to satisfy the +3V min input-output voltage differential of the regulator. For a desired  $V_{EXC}$  the resistor value,  $R_{EXT}$ , is determined by the equations:

$$R_T = (10k\Omega \times V_{REF OUT}) / (V_{EXC} - V_{REF OUT}); V_{REF OUT} = 6.8V$$

$$R_{EXT} = (20k\Omega \times R_T) / (20k\Omega - R_T)$$

The +10V to +15V range can be covered by a 20k $\Omega$  potentiometer between pins 19 and 20.

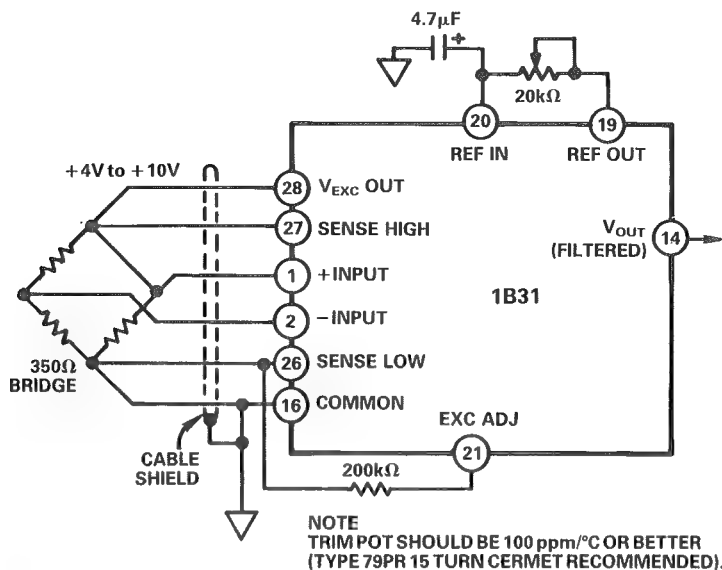
## CONSTANT VOLTAGE EXCITATION: +10V TO +15V RANGE



Similarly, to decrease  $V_{EXC}$  down to +4V, a 200kΩ resistor and a 20kΩ potentiometer should be connected as shown in the diagram below.

A 4.7μF tantalum capacitor from REF IN (pin 20) to COMMON (pin 16) is recommended in all cases to lower the voltage noise at the reference input.

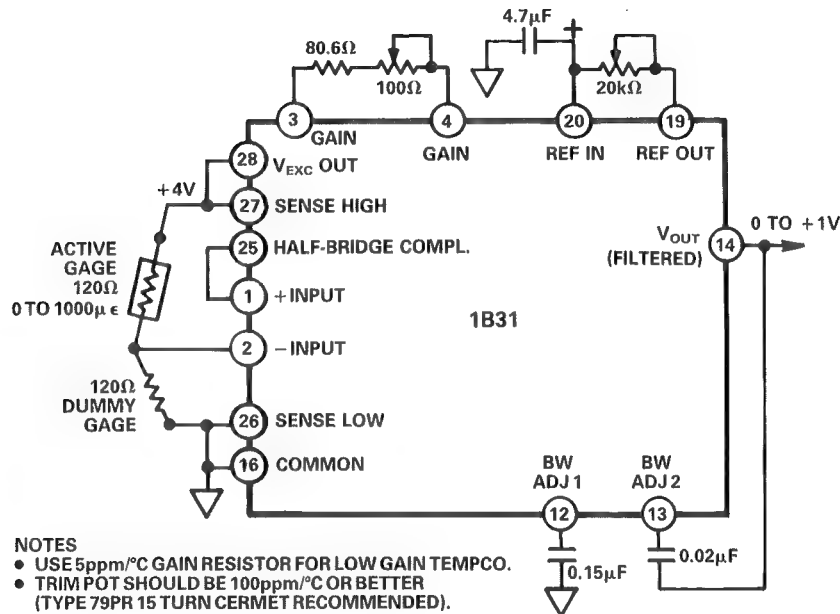
## CONSTANT VOLTAGE EXCITATION: +4V TO +10V RANGE



### Using the Internal Half-Bridge

The figure below shows a 1B31 in a strain measurement system. A single active gage (120Ω, Gage Factor = 2) is used in a bridge configuration to detect fractional changes in a gage resistance caused by strain. An equivalent resistance dummy gage mounted adjacent to the active gage provides temperature compensation. The rest of the bridge is completed by the 1B31 internal half-bridge network which consists of two 20kΩ, 1% thin-film resistors tracking to within 5ppm/°C. Bridge excitation is set at +4V to avoid self-heating errors from the strain gage. System calibration produces a +1V output for an input of 1000 microstrains. The filter cutoff frequency is set at approximately 100Hz.

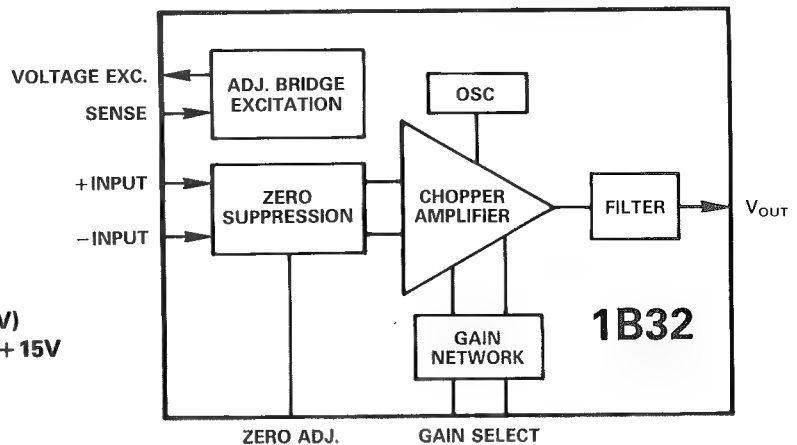
## STRAIN GAGE APPLICATION USING INTERNAL HALF-BRIDGE



## 1B32 BLOCK DIAGRAM

### 1B32 FEATURES

**Low Cost**  
**Complete Signal-Conditioning Solution**  
**Small Package: 28-Pin Double DIP**  
**Internal Thin-Film Gain Network**  
**High Accuracy**  
 Low Input Offset Tempco:  $\pm 0.07 \mu\text{V}/^\circ\text{C}$   
 Low Gain Tempco:  $\pm 2 \text{ppm}/^\circ\text{C}$   
 Low Nonlinearity:  $\pm 0.005\%$  max  
 High CMR: 140dB min (60Hz,  $G = 1000\text{V/V}$ )  
**Programmable Bridge Excitation: +4V to +15V**  
**Remote Sensing**  
 Low Pass Filter ( $f_c = 4\text{Hz}$ )

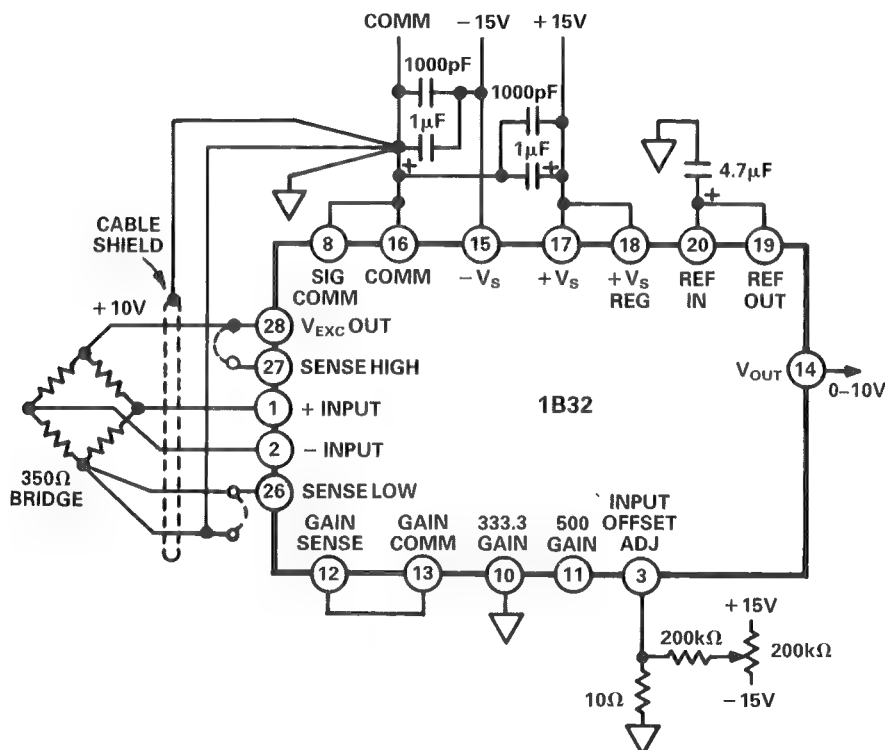


The 1B32 is based on a switched capacitor, chopper stabilized amplifier followed by an active filter and an adjustable voltage regulator section for excitation. The ultralow drift chopper samples the difference between the +INPUT and -INPUT at 190Hz. The signal is modulated, amplified and then demodulated. This stage introduces a pole with a 20dB/decade rolloff from 4Hz. The high-level signal is then filtered by a two-pole active filter with a 4Hz cutoff frequency to give a  $\pm 10\text{V}$  output. The clock signal for the chopper is generated by an on-board oscillator.

The gain of the 1B32 can be pin-strapped by an internal resistor network. Standard gains of 333.3 and 500 can be achieved by this method with gain tempco of  $\pm 6 \text{ppm}/^\circ\text{C}$  max. Finally, the offset adjust of the amplifier is input referred, and requires a voltage input similar to the differential input voltage to implement wide range suppression.

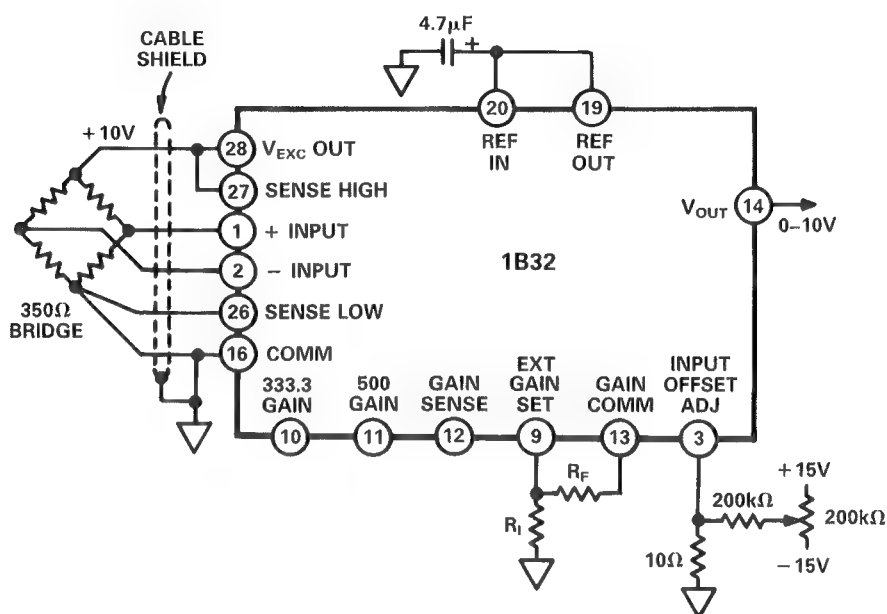
The adjustable bridge excitation section is essentially identical to that of the 1B31.

## INTERNAL GAIN STRAPPING



The figure above shows a typical circuit configuration for the 1B32. As previously stated, the differential gain of the 1B32 can be either pin-strapped or programmed externally with two resistors. The internal thin-film network provides gain of 500 and 333.3 for standard load cell sensitivities of 2mV/V and 3mV/V. As shown above, this is achieved by connecting GAIN SENSE (pin 12) to GAIN COMM (pin 13) and grounding either pin 10 or pin 12. The gain tempco using the internal network is an excellent  $\pm 2\text{ppm}/^\circ\text{C}$  typ ( $\pm 6\text{ppm}/^\circ\text{C}$  max).

## EXTERNAL GAIN STRAPPING



To program gain externally, two resistors are connected as shown in the figure above. The gain equation is:

$$G = 1 + R_F/R_I$$

The gain strapping pins (10 and 11) and GAIN SENSE (pin 12) are left unconnected, effectively floating the internal network.

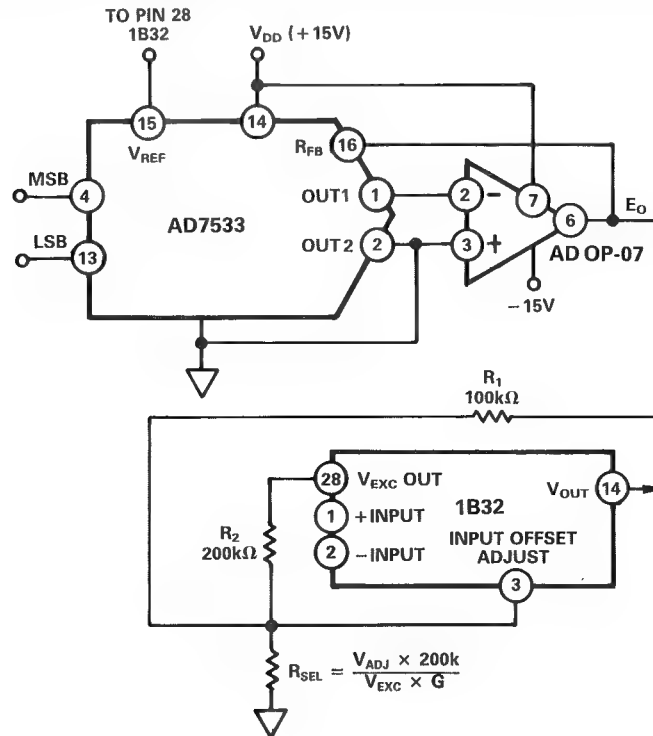
The input-referred offset adjust has the same sensitivity as the inputs of the 1B32. The voltage level at INPUT OFFSET ADJ (pin 3) is gained by the same factor as the input signal to provide a  $\pm 10V$  output adjust. The figures above show an external network and potentiometer set up for a  $\pm 7.5mV$  span at the input, which will give a  $\pm 2.5V$  output adjust capability when gain is set at 333.3 ( $7.5mV \times 333.3 = 2.5V$ ). Wider ranges can be chosen with the appropriate resistor and potentiometer values. If offset adjustment is not required, pin 3 must be grounded.

Voltage excitation programming for the 1B32 is done in the same manner as that of the 1B31.

#### Digital Output Offset Adjustment

A 10-bit multiplying DAC such as the AD7533 can be used to control the output offset of the 1B32 as shown below. The DAC is configured for unipolar operation with an AD OP-07 generating a voltage output. This 0-10V output is attenuated by  $R_1$  and  $R_{SEL}$  and superimposed on another fixed voltage derived from  $V_{EXC}$ . Thus the voltage at pin 3 (INPUT OFFSET ADJUST) is insensitive to the tempco of the excitation voltage since it is also used as the reference of the DAC. For best performance  $R_1$  and  $R_2$  should track to  $\pm 5ppm/^{\circ}C$ . As an example, a  $\pm 5V$  output adjustment can be obtained by using  $R_{SEL} = 200\Omega$  for  $G = 500$  and  $V_{EXC} = 10V$ .

### OUTPUT OFFSET ADJUST USING A 10-BIT DAC

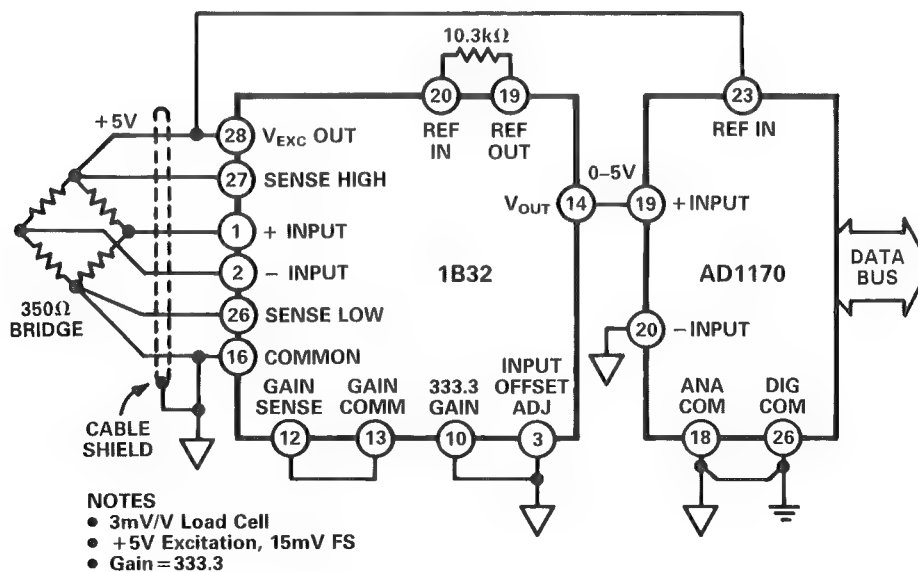




### Pressure Transducer Data Acquisition System

A two device solution for microcomputer based data acquisition using a 1B32 and an AD1170 18-bit A/D converter is shown below. A 3mV/V pressure transducer (e.g. Dynisco 800 series) is interfaced to a 1B32 configured with a gain of 333.3, to provide a 0 to 5V output. The regulated excitation is +5V, and is used as the reference input for the AD1170 to produce ratiometric operation. This configuration yields very high CMR enhanced by the 1B32 low pass filter and the integrating conversion scheme of the AD1170.

### AUTO-CALIBRATING DATA ACQUISITION USING 1B32 AND AD1170



In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer. The full-scale output of the 1B32 and transducer can be normalized to the AD1170 full scale through the electronic calibration command ECAL. Both the offset and full scale correction data will then be stored nonvolatile memory to eliminate the need for the trim process after each power-up. The AD1170 eliminates a potentiometer or software overhead which might otherwise be needed for these functions.

# **ANALOG SIGNAL PROCESSING**



## **ANALOG COMPUTATION & SIGNAL PROCESSING**

This section of our seminar considers techniques for analog computation and signal processing. By exploiting the basic physics of semiconductor devices it is possible to design circuits which perform a wide variety of mathematical operations, including addition, subtraction, multiplication, division as well as trigonometrical, logarithmic, and exponential functions. Such circuits perform in the analog domain and frequently offer real advantages over more conventional digital computation.

### **BENEFITS OF ANALOG DATA PROCESSING**

There is a widely-held belief that analog techniques are obsolete and that every possible electronic operation can today best be performed by digital techniques. This is far from the true state of affairs and there are many operations which are still best performed in the analog domain.

## **ANALOG SIGNAL PROCESSING HAS REAL ADVANTAGES OVER DIGITAL COMPUTATION**

Analog signal processing can out-perform digital processing on accuracy, cost, complexity, speed, and various combinations of these.

## **IN SOME CIRCUMSTANCES ANALOG SIGNAL PROCESSING IS**

- **Faster**
- **Cheaper**
- **More Accurate**
- **Simpler**

## **THAN DIGITAL PROCESSING**



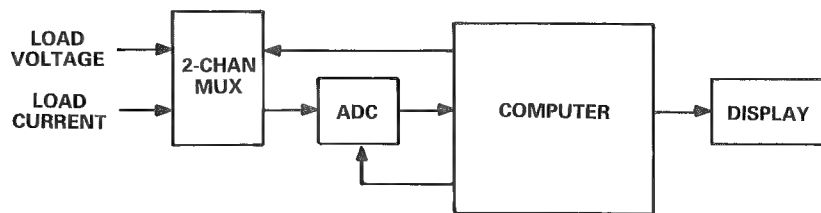
Operations where analog computation is often preferable to digital include those where both the input and output signals must be analog, where limited amounts of processing are required and no digital circuitry is present, where the signal is differentiated to produce a rate signal, where fast signals must be processed in real time, where large dynamic ranges are involved, and where complex or transcendental functions must be evaluated.

## ANALOG SIGNAL PROCESSING HAS ADVANTAGES WHERE:

- Inputs and Outputs Are Both Analog
- No Digital Circuitry is Available
- Signals are Being Differentiated
- Fast Real-Time Results are Required
- There are Wide Dynamic Ranges of Input
- Complex and Transcendental Functions are Being Computed

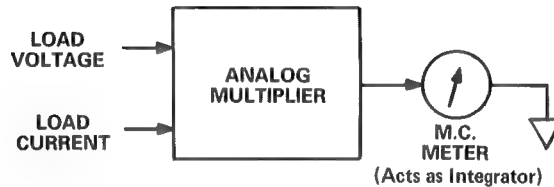
It is important that each case is judged on its merits. The dedicated analog engineer can solve almost any processing problem in a purely analog manner—the dedicated bit-freak in a digital way. The balanced approach is to consider each problem in its own terms and make a decision based on all the factors present. For example a simple ac power meter integrates and displays the product of voltage and current at a load and may be constructed very easily with a single analog multiplier—whereas a digital power meter would require conversion of both voltage and current at the digital form (with considerable attention to the timing of the conversions since the relative phase of the two signals is of critical importance) and then a digital multiplication followed by output to a display. If I had nothing and simply wanted a power meter I should use the analog approach (which needs only a multiplier and a meter), but if I already had a computer, a display driven by it, and a multiplexed ADC with spare capacity, I would be foolish to do so since the cost of adding a power monitor facility to my existing hardware and software would be minimal.

### DIGITAL POWER MONITOR



NOTE: CONVERSION TIMING MUST PRESERVE PHASE INFORMATION

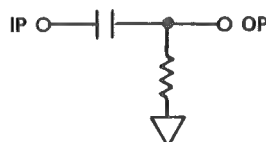
### ANALOG POWER METER



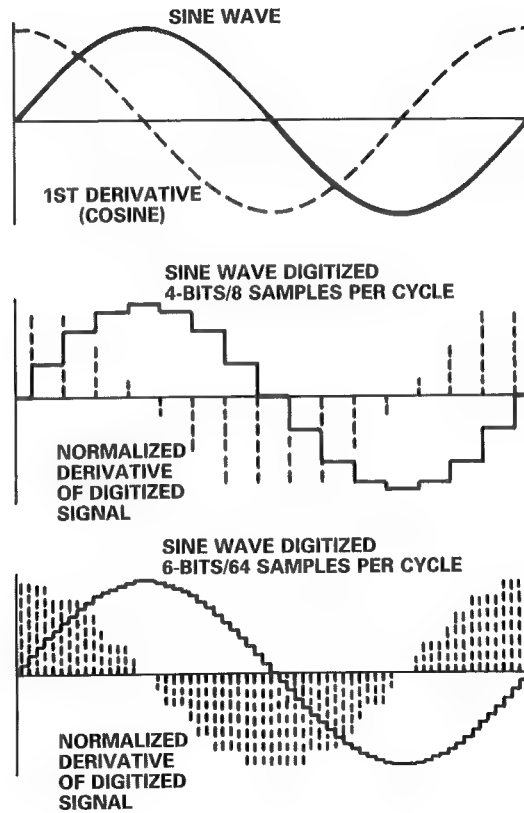
If the computer were busy, though, even if the final result were required in digital form it might make sense to compute the power with an analog multiplier and then convert its output rather than convert and then compute—simply to save CPU time. This is more likely to be useful where more complex computations are involved but could be significant even for simple multiplication.

The first derivative of a varying analog signal can be computed with a capacitor and a resistor.

### ANALOG DIFFERENTIATION

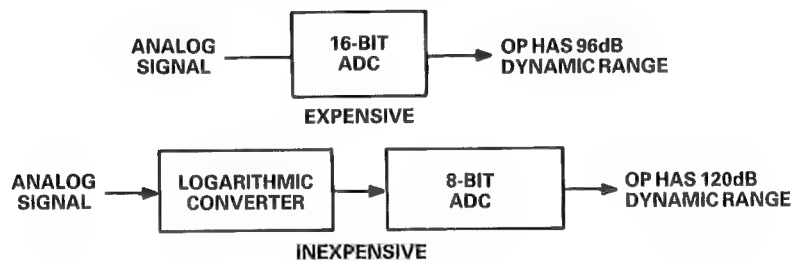


If the analog signal is first digitized not only must a more complex method be used to obtain the derivative but the digitizing must be done at high resolution in both time and amplitude—which is expensive.



Digitizing a signal with wide dynamic range is also expensive. If such a signal is digitized with a 16-bit ADC (which is a very expensive device) the ratio of an LSB to full-scale is 96dB whereas if the signal is first applied to a logarithmic converter (frequently misnamed a logarithmic amplifier) then a dynamic range approaching 120dB is practical with an 8-bit ADC.

### ANALOG PROCESSING IS LESS EXPENSIVE AT HIGH DYNAMIC RANGE



## ANALOG COMPUTATION CIRCUITRY

The operation of any analog computational circuits depends on the logarithmic properties of silicon junctions. An ideal logarithmic diode has the current voltage relationship:

$$I = I_0 \left( e^{\frac{qV}{kT}} - 1 \right) \quad \text{or} \quad V = \frac{kT}{q} \ln \left( \frac{I}{I_0} + 1 \right) \approx \frac{kT}{q} \ln \left( \frac{I}{I_0} \right)$$



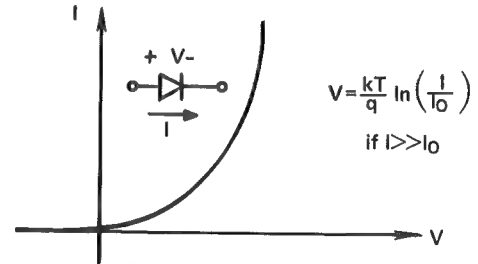
### AN "IDEAL LOGARITHMIC DIODE" HAS THE CURRENT-VOLTAGE RELATIONSHIP:

$$I = I_0 (e^{qV/kT} - 1)$$

where:

$I$  is the current through the diode  
 $V$  is the voltage across the diode  
 $q$  is a constant equal to the unit charge,  $1.60219 \times 10^{-19}$  coulombs  
 $k$  is Boltzmann's constant,  $1.38062 \times 10^{-23}$  joules/° Kelvin  
 $T$  is the absolute temperature (in ° Kelvin)  
 $I_0$  is the extrapolated current for  $E_0 = V = 0$  Volts

### DIODE CURVE



These equations clearly tell us that the current in a diode increases exponentially with voltage or, conversely, the voltage increases logarithmically with current. What they do not show so clearly is that  $I_0$ , the theoretical diode current at zero voltage, is temperature dependent and so the variation of a diode's behavior with temperature is by no means as simple as the equation would suggest— i.e., the voltage is not proportional to absolute temperature at a fixed current. There are several approximations concerning the logarithmic behavior of diodes which are worth remembering:

### DIODE APPROXIMATIONS

$$\frac{kT}{q} = 26\text{mV (exact at } 28.58^\circ\text{C)}$$

$$\frac{kT}{q} \ln(10) = 60\text{mV (exact at } 29.25^\circ\text{C)}$$

This simplifies the diode expression to:

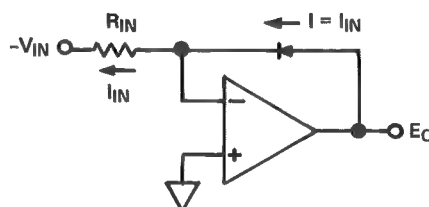
$$V = 60\text{mV} \log \frac{I}{I_0}$$

or  $V$  increases 60mV every time current increases by a factor of 10

$$\frac{d}{dT} \frac{kT}{q} = 0.34\%/^\circ\text{C @ } 25^\circ\text{C}$$

If we were to place an ideal logarithmic diode in the feedback path (output to inverting input) of an operational amplifier and apply a current to the inverting input the output voltage would be the logarithm of the input current times a temperature varying constant.

### DIODE LOG CONVERTER



$$E_O = \frac{kT}{q} \ln \left( \frac{I_{IN}}{I_0} \right) \approx 0.06 \log \frac{V_{IN}}{R_{IN} I_0}$$

if  $I_{IN} \gg I_0$

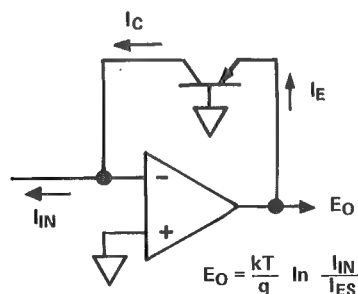
It is unfortunate that real diodes are not ideal logarithmic diodes. In a real diode the bulk resistivity,  $R_B$ , of the silicon limits the logarithmic accuracy at high currents and diffusion currents in surface inversion layers and generation-recombination effects in space-charge regions cause a scale factor error,  $m$ , at low currents. We thus find that:

$$E_O = m \frac{kT}{q} \ln \left( \frac{I}{I_O} \right) + IR_B \text{ (m varies with current)}$$

Even with similar diodes  $m$  can vary (it is never less than 1 and may be as high as 4), as does the value of  $E_O$  at which  $m$  changes. General purpose diodes are thus impractical as logarithmic diodes for dynamic ranges of more than 100:1 (2 decades).

Luckily we can replace the diode with a grounded-base transistor and get a dynamic range of 1000000:1 (6 decades) or more—the only disadvantage of such a circuit is that the signals can only have a single polarity (so does the logarithm function—but a “bipolar logarithmic converter” might have practical applications).

## TRANSISTOR LOG CONVERTER



From the Ebers and Moll equations\* it may be shown that:

$$E_O = \frac{kT}{q} \ln \left( \frac{I_{IN}}{I_{ES}} \right) - \frac{kT}{q} \ln (\alpha n) \text{ where } I_{IN} \gg I_{ES}$$

Where  $I_{ES}$  is the emitter saturation current and  $\alpha n$  is the forward current-transfer ratio ( $\alpha n$  is NOT the grounded-base current gain).

Since  $I_{ES}$  is less than a picoampere, and  $\alpha n$  is nearly unity over a wide range of currents, in the silicon planar transistors used to manufacture logarithmic converters the effect of the second term may generally be disregarded and the equation simplifies to:

$$E_O = \frac{kT}{q} \ln \left( \frac{I_{IN}}{I_{ES}} \right)$$

Such logarithmic converters are temperature sensitive.  $kT/q$  has a TC of 0.34%/°C around 25°C, and  $I_{ES}$  doubles for every 10°C temperature rise (and varies with device size and geometry). However if we have two transistors matched for  $V_{BE}$ , which is relatively simple to do on an integrated circuit, the ratio of their  $\alpha I_{ES}$  tends to be stable with temperature:

$$\frac{kT}{q} \ln \left( \frac{I_1}{\alpha I_{ES1}} \right) - \frac{kT}{q} \ln \left( \frac{I_2}{\alpha I_{ES2}} \right) = \frac{kT}{q} \ln \left( \frac{I_1}{I_2} \right) + \ln \left( \frac{\alpha I_{ES2}}{\alpha I_{ES1}} \right)$$

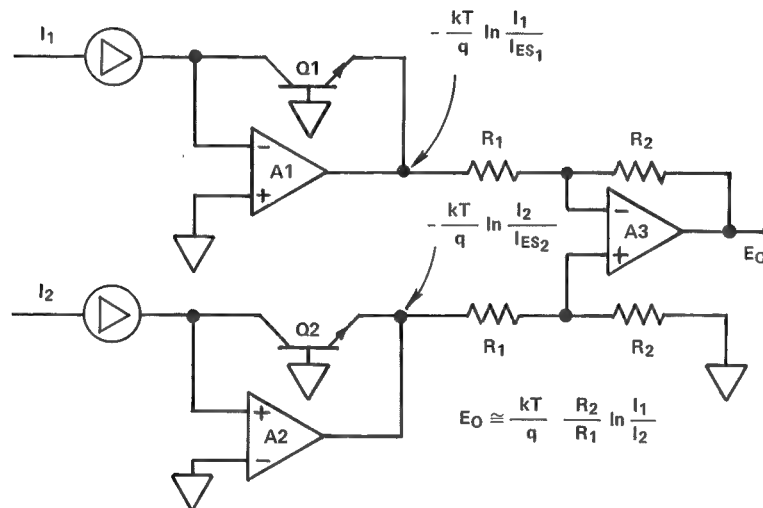
$$\ln \left( \frac{\alpha I_{ES2}}{\alpha I_{ES1}} \right) \text{ term is zero if } \alpha I_{ES1} = \alpha I_{ES2}.$$

\*See “Nonlinear Circuits Handbook”, Daniel H Sheingold, ed, Analog Devices 1974 for a detailed derivation.



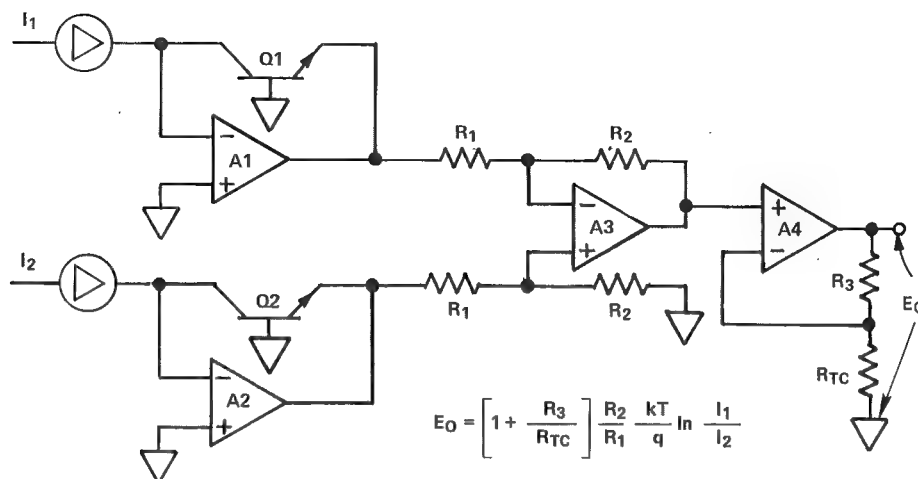
If transistors Q1 and Q2 are identical the circuit below will compensate for  $I_{ES}$  variation and give us an output voltage which is proportional to  $kT/q$  times the logarithm of the ratio of its input currents.

### LOG RATIO CIRCUIT WITH TEMPERATURE-COMPENSATED $I_{ES}$



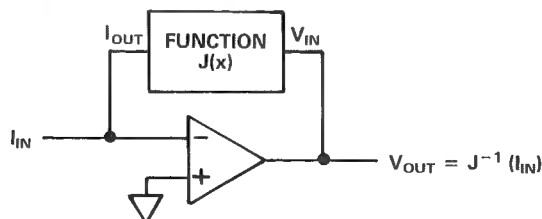
By adding a second amplifier with temperature varying gain it is possible to compensate for  $kT/q$  as well—such an amplifier uses a thermistor in its feedback path and if a suitable thermistor is chosen (and it is maintained at the same temperature as the transistors Q1 & Q2) the final circuit shown will have a logarithmic ratio response which is more or less stable over temperature. A suitable thermistor is the Q-81 from Tel Labs Inc. [154G, Harvey Road, Londonderry, NY 03053. (603) 625-8994 Twx: (710) 220-1884]. Like the simple logarithmic converter these log ratio circuits will work with signals of one polarity only.

### LOG RATIO CIRCUIT WITH COMPENSATION FOR BOTH $I_{ES}$ AND $kT/q$



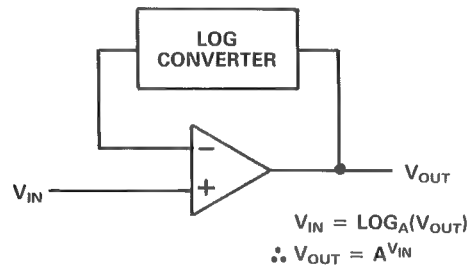
A basic technique in the design of analog computation circuits is that inverse function generators may be produced by using a function generator in the feedback path of an operational amplifier.

### INVERSE FUNCTION GENERATOR MAY BE BUILT FROM A FUNCTION GENERATOR AND AN OPERATIONAL AMPLIFIER



This only works for a monotonic function, of course, or over a range of values where a function remains monotonic—otherwise the negative feedback becomes positive feedback and the circuit either oscillates or latches up. The logarithm is a monotonic function and therefore an operational amplifier with a logarithmic converter in its feedback path will act as an antilogarithmic converter, or exponentiator.

### LOGARITHMIC CONVERTER IN A FEEDBACK PATH YIELDS AN ANTILOGARITHMIC CONVERTER (OR EXPONENTIATOR)

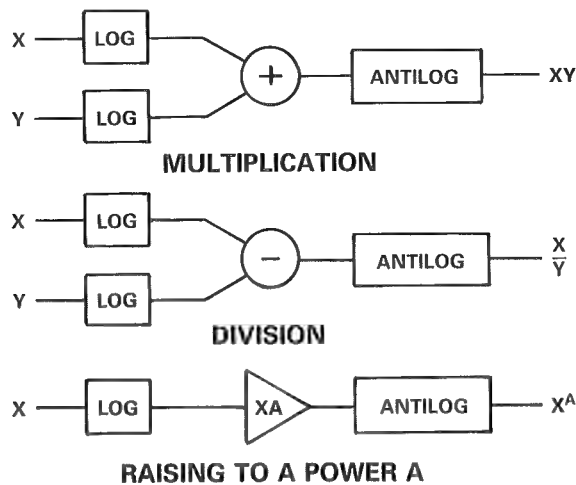


If the logarithm and antilogarithm functions are performed on the same chip it is reasonable to assume that the temperature of the logging transistor in both circuits is the same and therefore not only is  $I_{ES}$  compensation unnecessary—so is  $kT/q$  compensation. Remember the basic properties of logarithms and antilogarithms:

$$\log(x) + \log(y) = \log(xy) \quad \log(x) - \log(y) = \log(x/y) \quad a \log(x) = \log(x^a) \quad \text{antilog}(\log(x)) = x$$

it is obviously possible to combine several log and antilog circuits on a chip, together with summing circuitry and amplifiers, to make temperature-stable circuitry capable of multiplication, division, and power computations.

### COMPUTATION WITH LOG AND ANTILOG CIRCUITS



The AD538 is just such a chip. It contains three logarithmic and one antilogarithmic circuits, together with an adder, a subtractor, and an amplifier whose gain,  $M$ , may be set to values between 0.2 and 5. It has three inputs  $X$ ,  $Y$ , and  $Z$  and its transfer function is:

$$E_O = Y \left( \frac{Z}{X} \right)^M$$

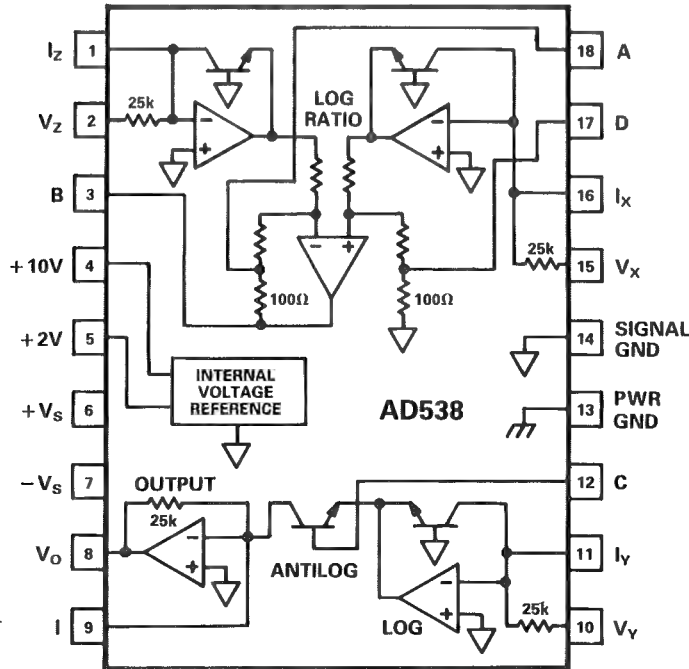
Since any of  $X$ ,  $Y$ ,  $Z$ , and  $M$  may be set to unity it can be used as a multiplier, or a divider, or for raising to powers (squarer, square rooter, cuber, cube rooter, etc.) It is particularly valuable as a divider with a wide denominator range but, of course, will only work with unipolar values of  $X$ ,  $Y$  and  $Z$ .

## AD538 FEATURES

$$V_{OUT} = V_Y \left( \frac{V_Z}{V_X} \right)^m \quad \text{Transfer Function}$$

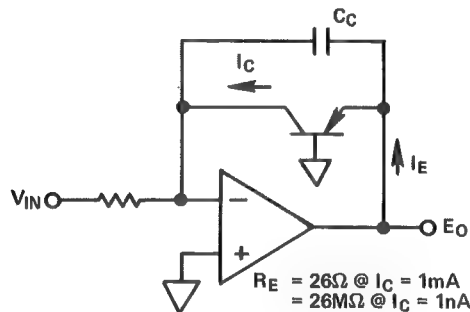
**Wide Dynamic Range (Denominator) – 1000:1**  
**Simultaneous Multiplication and Division**  
**Resistor-Programmable Powers & Roots**  
**No External Trims Required**  
**Low Input Offsets < 100 $\mu$ V**  
**Low Error  $\pm 0.25\%$  of Reading (100:1 Range)**  
**+2V and +10V On-Chip References**  
**Monolithic Construction**

## AD538 FUNCTIONAL BLOCK DIAGRAM



This type of logarithmic converter has another disadvantage as well as its unipolar inputs (although the AD538 is not very seriously affected by it)—its bandwidth varies with signal amplitude.

## LOG CONVERTER COMPENSATION PROBLEM

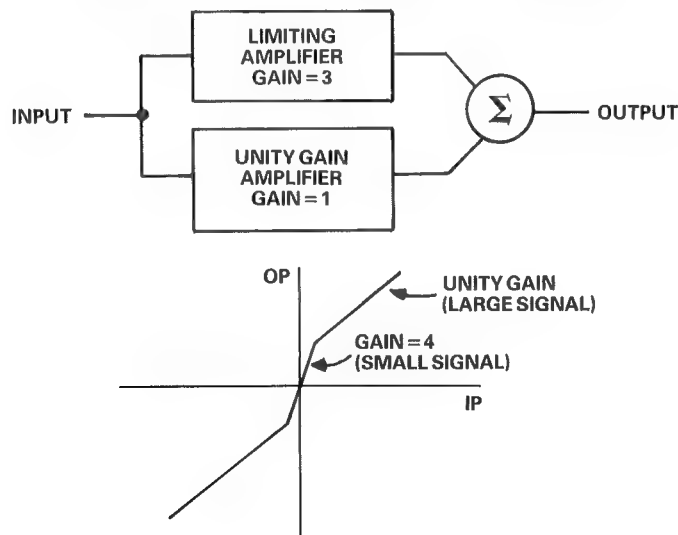


The problem results from the variation of emitter resistance,  $R_E$ , with current in the grounded-base transistor. This resistance is inversely proportional to the emitter current, being approximately  $26\Omega$  at  $1\text{mA}$ . The bandwidth of the circuit is inversely proportional to the product of  $R_E C_C$  (which may be an external compensation capacitor or merely stray capacity) and is thus proportional to the transistor current. Thus if the logarithmic converter works over  $120\text{dB}$  dynamic range its bandwidth will vary by  $1,000,000:1$ —which can be inconvenient.

Adding some extra resistance (usually a few kilohms) between the amplifier output and the emitter will improve the situation at higher currents and the use of fully integrated logarithmic converters with very low values of  $C_C$  can also help but the maximum bandwidth of such circuits is rarely more than 100kHz and frequently much less. At higher frequencies other techniques must be used.

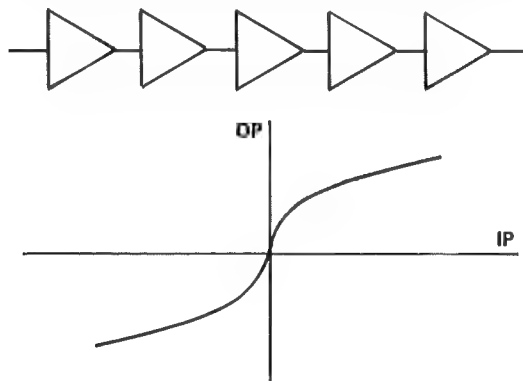
A conceptually simple technique offering wide bandwidth and large dynamic range (and sometimes known as a "true log amplifier") uses a number of similar amplifiers in cascade. Each amplifier consists of a limiting amplifier and a unity gain amplifier whose outputs are summed.

### STRUCTURE AND PERFORMANCE OF "TRUE LOG AMPLIFIER" ELEMENT



When a small signal is applied to the amplifier both halves contribute to the output and the gain, in the amplifier shown, is 4 times (12dB)—when the signal is increased the limiting amplifier goes into its limiting region and contributes a fixed amount to the output and the gain drops to unity (0dB). If a number of such stages are cascaded the gain of the strip to small signals is the product of the gains of all the stages, but as the input is increased the last stage limits and the gain drops by 12dB, then the next stage limits and the gain drops by a further 12dB, and so on until all the stages have limited and the gain is unity. If we plot the transfer characteristic of such a strip of cascaded amplifiers we find that it consists of a series of straight lines but approximates quite closely to a logarithmic law.

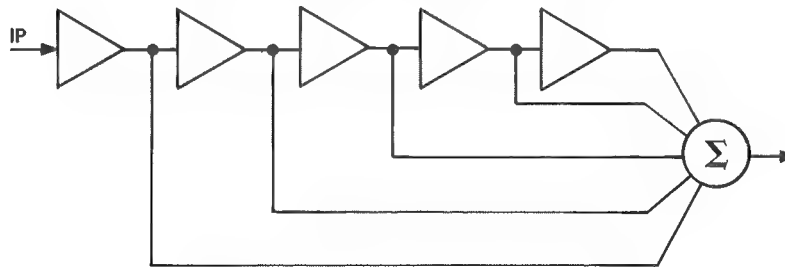
### LOG AMPLIFIER FORMED BY CASCADING SEVERAL STAGES



In practice, if the limiting amplifier limits “softly” (i.e., does not step suddenly from full gain to zero gain but does so over a small change of input), the approximation to a logarithmic response can be within 0.1dB. Practical logarithmic converters of this type are quite often used in the intermediate frequency (IF) sections of radar receivers and can be made with dynamic ranges of up to 100dB (100000:1). The response is not truly logarithmic, of course—it is symmetrical about zero, while the function  $\ln(x)$  is indeterminate for negative values of  $x$ , and it is also not logarithmic for very small positive values of input when a true logarithmic function would give rise to a negative output. Such logarithmic converters are also, usually, ac coupled and work for inputs between a few MHz and a few hundred MHz which is fine for radar receivers but less so for analog computation. There are several variants of the basic concept.

If we replace the complex stages consisting of a limiting amplifier, a unity gain amplifier, and a summing circuit with a simple limiting amplifier and use a single summing circuit to sum all the amplifier outputs we have a logarithmic converter which is functionally equivalent to the one we have just described, but simpler.

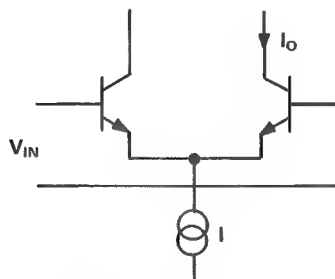
### LOG AMPLIFIER FORMED WITH LIMITING AMPLIFIERS



This architecture is also used in radar systems, with ac coupled amplifiers and current output detectors making the connection from each amplifier output to the summing point (it is slightly easier to sum currents than voltages, especially at high frequencies). It is known as a “successive detection” logarithmic amplifier (though the term “logarithmic amplifier” is somewhat of a misnomer and “logarithmic converter” better describes the function). The ac coupling of logarithmic converters developed for radar IF strips makes them almost useless for low frequency or dc analog computation (the use of capacitors integrated on the chips of such limiting amplifiers results in low frequency limits well over 1MHz in many cases), and the difficulties of combining low offsets with high frequency performance have prevented the technique being used at dc or LF.

Logarithms and antilogarithms are by no means the only functions that may be generated with silicon transistors. The basic long-tailed pair of transistors (which consists of two similar transistors with a current fed to their joined emitters and a differential signal applied between their bases) has hyperbolic tangent transconductance. With suitable circuitry this can be modified to approximate a sinusoidal characteristic over the range  $-90^\circ$  to  $+90^\circ$ .

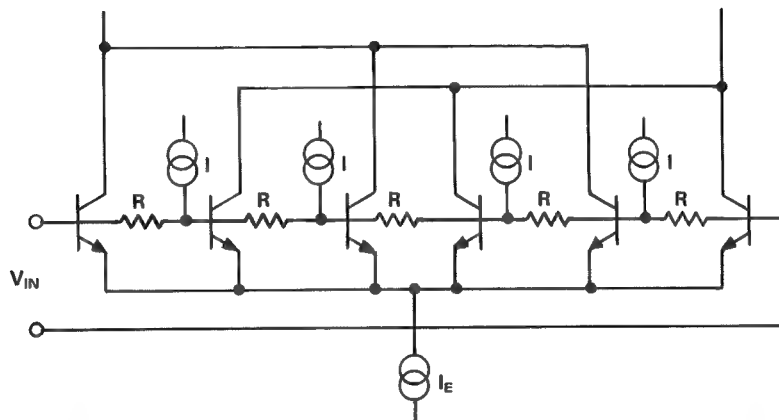
### TRANSFER CHARACTERISTIC



A LONG-TAILED PAIR OF TRANSISTORS HAS A HYPERBOLIC TANGENT TRANSFER CHARACTERISTIC

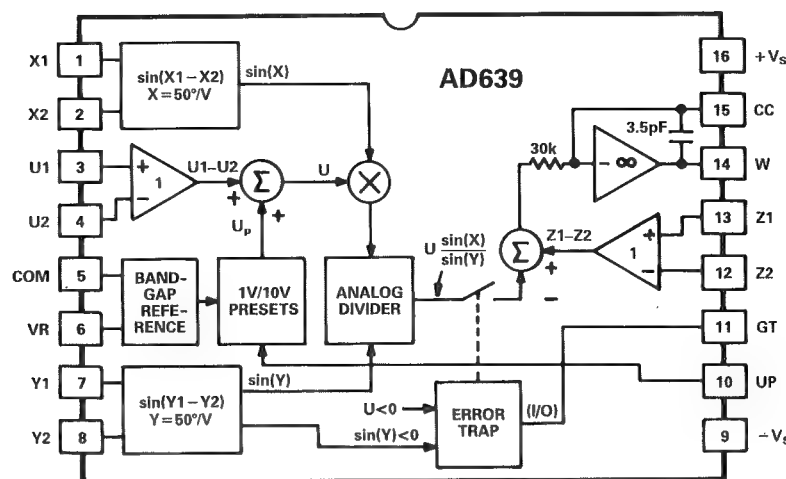
Gilbert\* has shown that it is possible to design a temperature-compensated sine-shaper circuit having a dynamic range of over  $1000^\circ$  by cross-connecting six transistors, five equal resistors, and four equal current sources in what is basically an extension of a long-tailed pair.

### 1000° SINE FUNCTION CIRCUIT



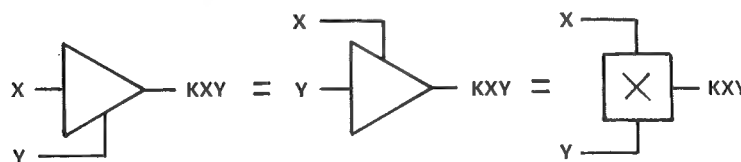
The AD639 contains two such sine-shaper circuits with fully differential inputs having  $50^\circ/V$  scaling, plus a voltage reference of  $1.8V$  ( $= 90^\circ$ ), a divider, a scaling circuit with fully differential input, and an output amplifier. It may be configured to compute sine, cosine, tangent, secant, cosecant, and cotangent and, using the function generator in the feedback of the amplifier as mentioned above, to compute the inverse functions as well.

### AD639 BLOCK DIAGRAM



The properties of a long-tailed pair of transistors are also used in transconductance multipliers. A transconductance multiplier is a circuit which may be considered as an amplifier with signal-controlled gain—there are two input ports and the gain from one to the output is proportional to the signal at the other. Since the gain from the other to the output is self-evidently proportional to the signal at the one there seems little to be gained by representing the multiplier as an amplifier with a gain-control terminal and so we represent it as a multiplying black box.

### A MULTIPLIER MAY BE CONSIDERED AS AN AMPLIFIER WITH GAIN PROPORTIONAL TO CONTROL INPUT



\*IEEE Journal of Solid-State Circuits, SC-17 No:6, December 1982: "A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and their Inverses".

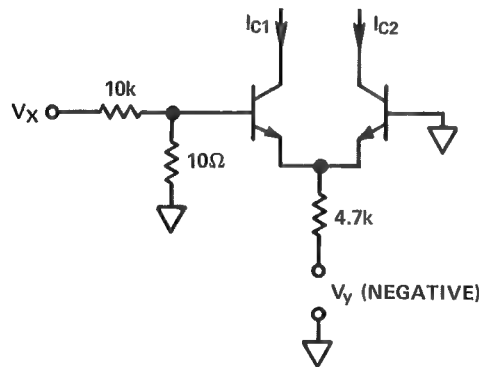
There is a linear relationship between the collector current of a silicon junction transistor and its transconductance (gain) which is given by the following equation:

$$\frac{dI_C}{dV_{BE}} = \frac{q}{kT} I_C$$

where  $I_C$  = collector current  
 $V_{BE}$  = base-emitter voltage  
 $q$  = electron charge ( $1.60219 \times 10^{-19}$ )  
 $k$  = Boltzmann's constant ( $1.38062 \times 10^{-23}$ )  
 $T$  = absolute temperature ( $K = ^\circ C + 273.15$ )  
 $q/kT$  =  $1/(25.69\text{mV})$  at  $25^\circ\text{C}$

We can exploit this relationship in a long-tailed pair of transistors to construct a multiplier:

### BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT



$$I_{C1} - I_{C2} = \Delta I_C = \frac{q}{kT} \left( \frac{V_Y + V_{BE}}{4.7 \times 10^3} \right) \left( \frac{10}{10,010} \right) V_X$$

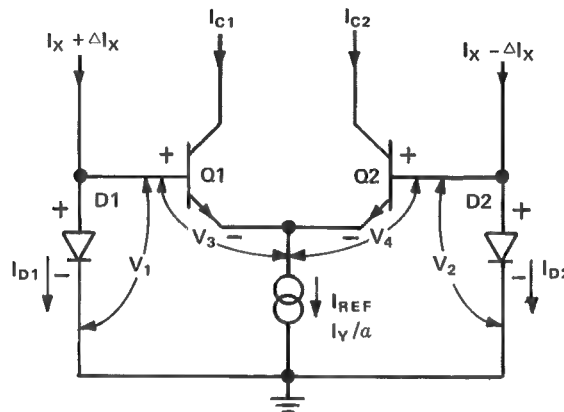
$$= 8.3 \times 10^{-6} (V_Y + 0.6) V_X \text{ @ } 25^\circ\text{C}$$

it is, alas, a rather poor multiplier for a number of reasons:

1. The Y input is offset by the  $V_{BE}$  which changes nonlinearly with  $V_Y$ .
2. the X input is nonlinear because of the exponential relationship between  $I_C$  and  $V_{BE}$ .
3. The scale factor is temperature variable ( $-0.34\%$  at  $25^\circ\text{C}$ ).

We can improve its performance by utilizing the logarithmic properties of diodes in quite a simple circuit.

### LINEARIZED 2-QUADRANT MULTIPLIER (PRINCIPLE)



This circuit has a differential current input as its X input and a current as its Y input. Since the differential X currents flow in two diodes the diode voltages, being logarithmic, compensate for the exponential  $V_{BE}/I_C$  relationship and, moreover, the  $q/kT$  scale factor in the transconductance function is exactly compensated by the  $kT/q$  scale factor in the diode response. This gives the circuit, which is known as the "Gilbert Cell" after its inventor\*, the linear transfer function:

$$\Delta I_C = \frac{\Delta I_X \cdot I_Y}{2I_X}$$

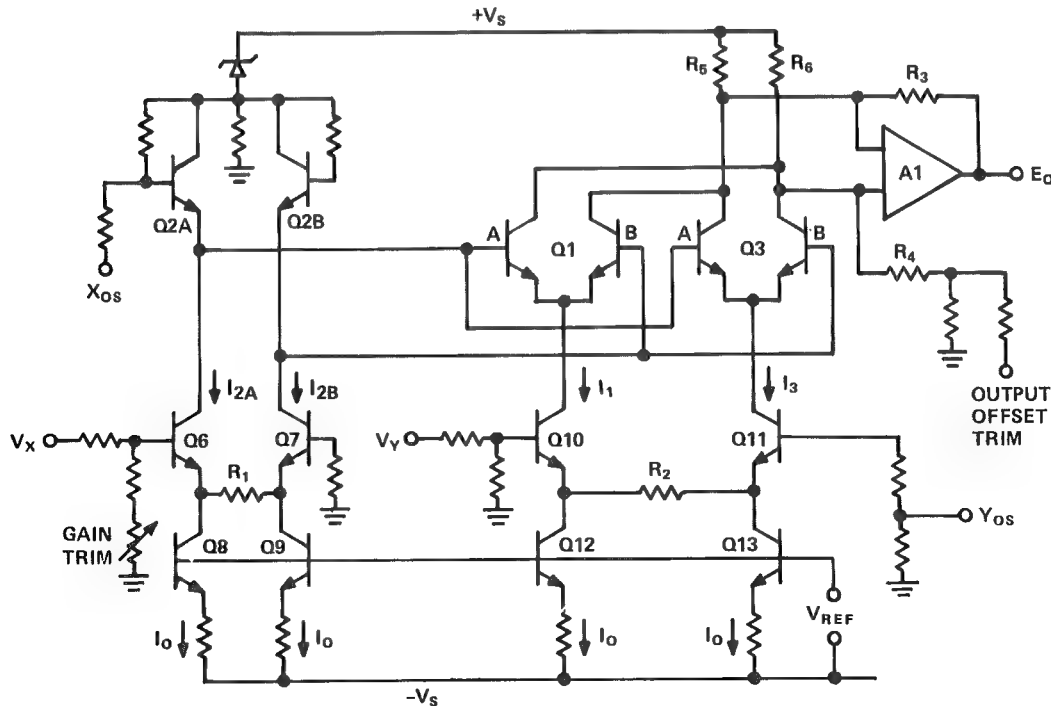
\*For further details see the "Nonlinear Circuits Handbook", Analog Devices, pp 217-221.

As it stands the circuit has a number of inconvenient features:

1. Its X input is a differential current,
2. Its Y input is a unipolar current—so the whole cell is only a two-quadrant multiplier, and
3. Its output is a differential current.

By cross-coupling two such cells, by using two long-tailed transistor pairs as input voltage-to-current converters, and by using a subtractor amplifier to convert the differential current output to a single-ended voltage output we can overcome all these inconveniences.

## 4-QUADRANT VARIABLE-TRANSCONDUCTANCE MULTIPLIER



In the circuit illustrated Q1 and Q3 are the two Gilbert cells, Q2A and Q2B form the linearization diodes (the base-emitter junction of a transistor is, of course, a diode and in applications of this type has a better diode performance than a simple diode), and the amplifier A1 acts as a differential current to single-ended voltage converter. Such transconductance multipliers have many advantages:

## ADVANTAGES OF THE VARIABLE-TRANSCONDUCTANCE MULTIPLIER

- 1) Good accuracy. Overall errors as small as  $\pm 0.1\%$  accuracy (AD534L)
- 2) Wide bandwidth. Bandwidths of 30MHz or more can be realized independent of input signal level (unlike log-antilog)
- 3) Simplicity and low cost.

The four-quadrant transconductance multiplier relies on the matching of a number of transistors in geometry, temperature, and current. This makes it a practical circuit in monolithic IC form but considerably harder to make with discrete components. Even the best IC process will leave some residual mismatches and these manifest themselves as dc errors—if the circuit is manufactured so that such error may be trimmed a very high performance indeed is possible. The errors, and their effects, are as follows:

## TRIMMABLE ERRORS IN MULTIPLIERS

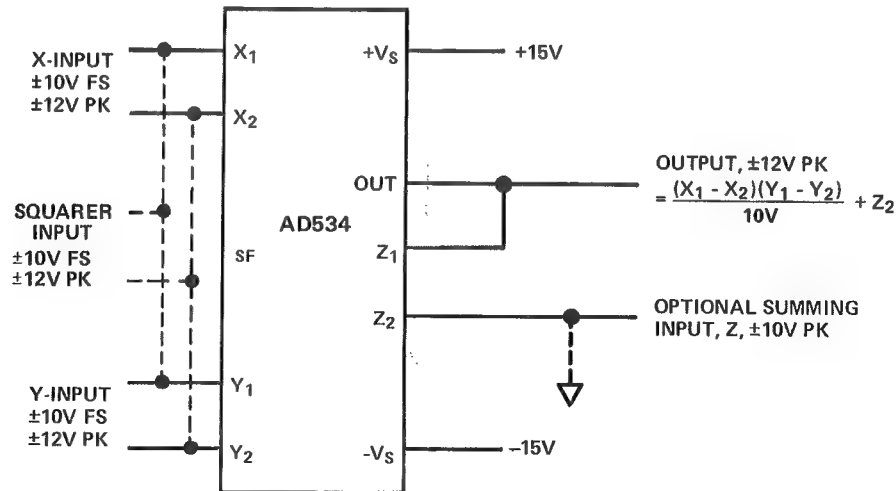
X-Input Voltage Offset:	Y Feedthrough
Y-Input Voltage Offset:	X Feedthrough
Z-Input (output amplifier) Voltage Offset:	dc output offset voltage
Resistor Mismatch:	Gain Error



Early transconductance multipliers were trimmed by the user but since there are four parameters requiring trimming and second-order effects will always make the trims more or less interactive the process is quite complex. As in so many other products Analog Devices' ability to fabricate integrated circuits with accurate, stable, laser-trimmed resistors reduces customer trims from a dire necessity to an unnecessary. The AD534 is the industry standard transconductance multiplier and is trimmed during manufacture to give very high performance.

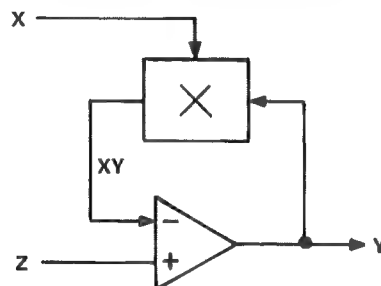
Because the structure of the transconductance multiplier is necessarily differential internally it is generally differential externally (one of a pair of differential inputs can always be grounded if a single-ended input is required) and this enables additional computation to be performed. Applications are better described in the applications section of this part of the seminar but one feature of the AD534 architecture should be explained at once—the summing inputs. It would be quite convenient if the connections to the summing (Z) inputs in the standard multiplier configuration were made internally.

## BASIC MULTIPLIER CONNECTION



This would only interfere with multiplier operation when a Kelvin voltage-sensing connection was required—which is not common with computation circuits like multipliers. However such an internal connection would prevent the output of the multiplier being fed back to the Y input and a separate input being applied to Z. This places the multiplier in the feedback path of its own internal amplifier and, as we noticed earlier, when a function generator is placed in a feedback loop the whole system becomes an inverse function generator—in this case a divider.

## A MULTIPLIER IN A FEEDBACK LOOP MAKES A DIVIDER

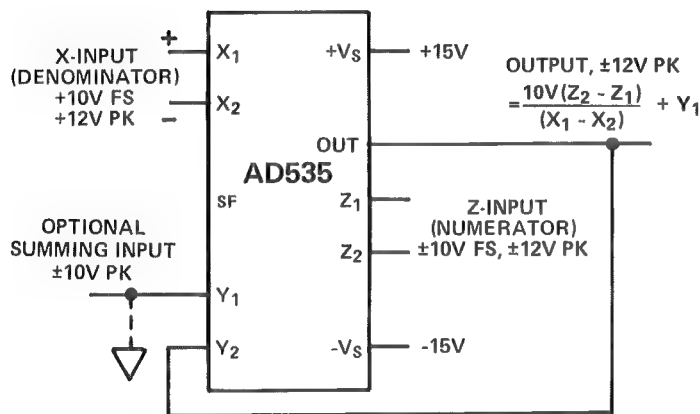


NEGATIVE FEEDBACK FORCES

$$\begin{aligned}
 XY &= Z \\
 \therefore Y (= \text{OUTPUT}) &= \frac{Z}{X} \\
 \therefore \text{CIRCUIT IS A DIVIDER!}
 \end{aligned}$$

The AD534 acts very successfully as a divider but if the error calculations are checked it turns out that a different trim algorithm is required to optimize divider performance from that required to optimize multiplication. The AD534 is therefore manufactured in a version which is factory trimmed as a divider—this circuit is known as the AD535. The chips are identical, only the trim algorithms differ.

## THE AD535 DIVIDER



### FEATURES

Pretrimmed to  $\pm 0.5\%$  max Error, 10:1 Denominator Range  
 $\pm 2.0\%$  max Error, 50:1 Denominator Range  
 All Inputs (X, Y and Z) Differential  
 Low Cost, Monolithic Construction

### APPLICATIONS

General Analog Signal Processing  
 Differential Ratio and Percentage Computations  
 Precision AGC Loops  
 Square-Rooting

We have considered a number of computational circuits which make use of the logarithmic properties of silicon diodes where some pains are necessary to extend the computational function from one or two quadrants. There is one specific application where this is not necessary—the rms to dc converter.

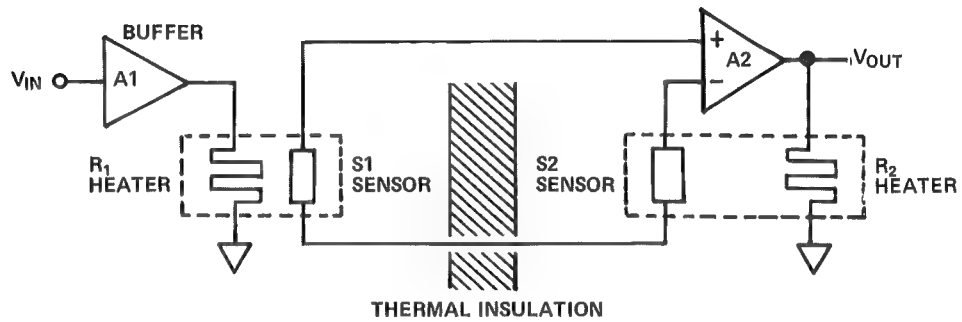
The rms value of an ac waveform is important to the engineer because it is a measure of the power in the signal. With sine and square waveforms the ratio of rms to peak (or to mean average—strictly mean average deviation (MAD)) value is well-known and measurements may be made by measuring one or the other and applying a correction factor, but where the waveform is unknown or variable the error between the mean and the rms value may be substantial.

## RMS, MAD, AND CREST FACTOR OF SOME COMMON WAVEFORMS

WAVEFORM		RMS	MAD	RMS MAD	CREST FACTOR																								
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 $V_m$	$\frac{2}{\pi} V_m$ 0.637 $V_m$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$																								
	SYMMETRICAL SQUARE WAVE OR DC	$V_m$	$V_m$	1	1																								
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$																								
<div> </div>	GAUSSIAN NOISE  CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}} \text{ RMS}$ = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	<table><tr><th>C.F.</th><th>q</th></tr><tr><td>1</td><td>32%</td></tr><tr><td>2</td><td>4.6%</td></tr><tr><td>3</td><td>0.37%</td></tr><tr><td>3.3</td><td>0.1%</td></tr><tr><td>3.9</td><td>0.01%</td></tr><tr><td>4</td><td>63ppm</td></tr><tr><td>4.4</td><td>10ppm</td></tr><tr><td>4.9</td><td>1ppm</td></tr><tr><td>6</td><td><math>2 \times 10^{-9}</math></td></tr></table>	C.F.	q	1	32%	2	4.6%	3	0.37%	3.3	0.1%	3.9	0.01%	4	63ppm	4.4	10ppm	4.9	1ppm	6	$2 \times 10^{-9}$				
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	PULSE TRAIN  η: "DUTY CYCLE"	<table><tr><th>η</th><th>MARK/SPACE</th></tr><tr><td>1</td><td>∞</td></tr><tr><td>0.25</td><td>0.3333</td></tr><tr><td>0.0625</td><td>0.0667</td></tr><tr><td>0.0156</td><td>0.0159</td></tr><tr><td>0.01</td><td>0.0101</td></tr></table>	η	MARK/SPACE	1	∞	0.25	0.3333	0.0625	0.0667	0.0156	0.0159	0.01	0.0101	$V_m \sqrt{\eta}$  $V_m$ $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	$V_m \eta$  $V_m$ $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	<table><tr><th><math>\frac{1}{\sqrt{\eta}}</math></th><th><math>\frac{1}{\sqrt{\eta}}</math></th></tr><tr><td>1</td><td>1</td></tr><tr><td>2</td><td>2</td></tr><tr><td>4</td><td>4</td></tr><tr><td>8</td><td>8</td></tr><tr><td>10</td><td>10</td></tr></table>	$\frac{1}{\sqrt{\eta}}$	$\frac{1}{\sqrt{\eta}}$	1	1	2	2	4	4	8	8	10	10
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2	2																												
4	4																												
8	8																												
10	10																												

We therefore require circuitry to measure the rms value of ac (or, indeed, dc) waveforms. The earliest circuitry for this purpose used the heating effect of the waveform.

## THERMAL RMS-DC CONVERTER

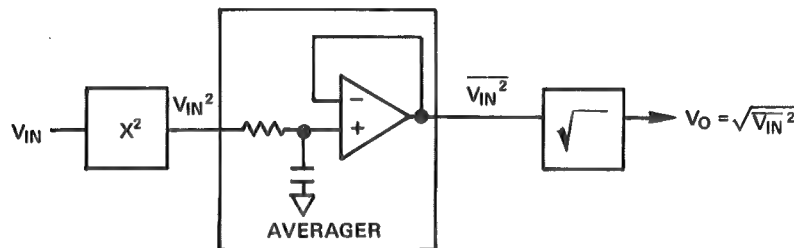


The waveform (probably amplified in a buffer amplifier) is applied to a resistor,  $R_1$ , which heats a temperature sensor. The output from the sensor is applied to the input to an amplifier whose other input comes from an identical sensor heated by an identical resistor,  $R_2$ , powered from the amplifier output. If the two sensor/resistor pairs have the same thermal inertia and the same thermal resistance to ambient (and some isolation from each other—although this need not be very good) it is evident that an equilibrium will be reached when the dissipation in  $R_1$  is equal to the dissipation in  $R_2$ . The dc voltage at  $R_2$  will then be equal to the rms value of the waveform at  $R_1$ .

Such an rms computation can be very accurate (errors  $< 0.1\%$ ) and can handle very high frequencies but the dynamic range available is small (auto-ranging can help but only at the expense of system complexity) and therefore the crest factor which can be handled is also relatively small. Also the design of the hardware, with its requirement for identical thermal performance of the two resistor/sensor pairs, is very demanding and the thermal inertia of the system causes long settling times. Quite recently the matched sensors have been fabricated in monolithic form. The accuracy of these monolithic parts is only about 1% and they are still slow to settle but they do have real advantages at RF.

At lower frequencies, however, higher accuracies and wider dynamic range can be achieved at lower cost by a computational circuit. It is quite obvious that the rms value of a signal may be computed with a squarer, an averager (leaky integrator), and a square rooter and that such a circuit could be built with two AD534s and an operational amplifier.

## DIRECT COMPUTATION OF THE ROOT-MEAN-SQUARE



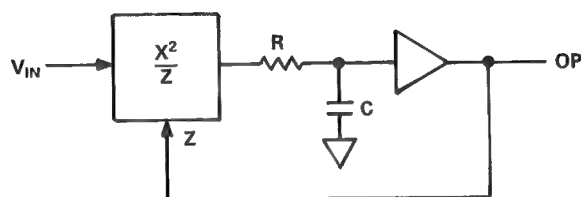
It is not a very good circuit. Because it contains a squarer it has limited crest factor and dynamic range (the output varies by 10,000:1 as the input varies by 100:1) and it also uses three precision components (two multipliers and an op amp). The same function can be realized by a single simple circuit which does what is known as an 'implicit' calculation which is arrived at by manipulating the original expression for rms.

$$V_{\text{rms}} = \sqrt{\overline{(V_{\text{IN}}^2)}}$$

$$\therefore V_{\text{rms}}^2 = \overline{(V_{\text{IN}}^2)}$$

$$\therefore V_{\text{rms}} = \frac{\overline{(V_{\text{IN}}^2)}}{V_{\text{rms}}}$$

We have arrived at our 'inverse function' again—by placing a function generator in a feedback loop we obtain an inverse function. In the present case we require a circuit to perform the  $X^2/Z$  function—we apply our input to the X terminal and take the output through an averager and then use it as a feedback signal at the Z terminal as well as the output.

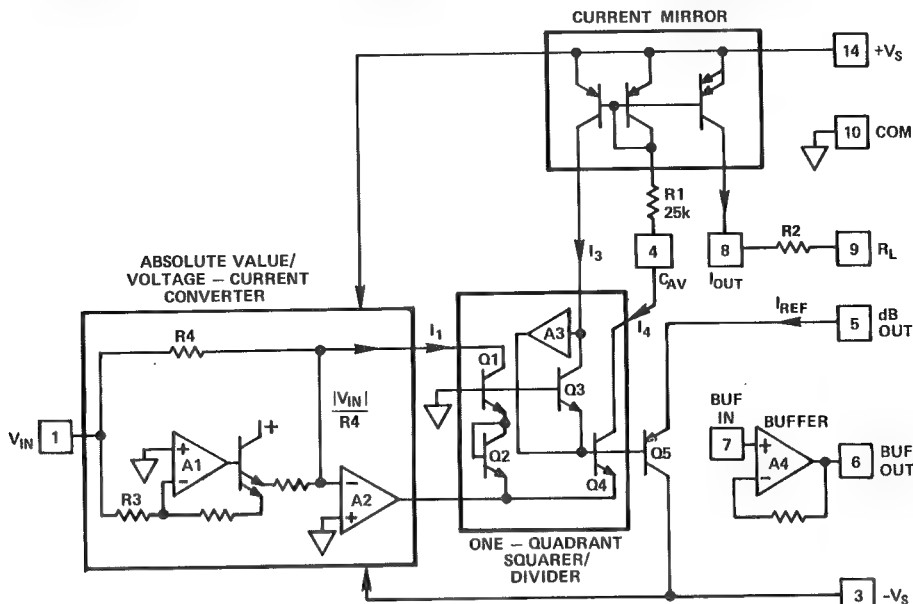


$$V_O = \sqrt{(V_{IN}^2)}$$

IF  $RC \gg$  THE PERIOD OF THE INPUT SIGNAL

While it is possible to construct such an rms circuit from AD534 circuits it is far simpler to design a dedicated rms circuit. The  $X^2/Z$  circuit may be current driven and need only be one quadrant if the input first passes through a modulus circuit (a modulus circuit may have either polarity input but although its output has the same amplitude as its input it always has the same polarity, whatever the polarity of the input.) The whole function may be constructed with four transistors, an amplifier, and a current mirror.

## RMS TO DC CONVERTER SIMPLIFIED SCHEMATIC



The whole rms/dc circuit is not much more complex. It comprises the circuit mentioned above, a modulus circuit with current output, a buffer amplifier to drive low impedances with a voltage output (the output from the current mirror is a current in a fixed resistor which loses accuracy if loaded), and a single extra PNP transistor to provide a linear dB output (which needs external temperature compensation). Analog Devices\* make several such circuits—they all contain laser trimmed resistors and hence provide high accuracy, even at high frequencies, high crest factors and high dynamic ranges, with minimal external trimming—they do, however, require a single external capacitor in the averaging circuit.

\*RMS to DC Conversion Application Guide – 2nd Edition”, Analog Devices, 1986.

## RMS TO DC CONVERTER FEATURES

FEATURES	AD536AJH	AD636JH	AD637JQ	AD736JN	UNITS
Input Range	7	0.200	7	0.200	$V_{rms}$
Accuracy	$\pm 5 \pm 0.5$	$\pm 0.5 \pm 1.0$	$\pm 1 \pm 0.5$	$\pm 0.5 \pm 0.6$	$mV \pm \% \text{rdg.}$
Bandwidth					
1% Accuracy FS Input	100	130	200	50	kHz
Crest Factor = $\frac{V_{peak}}{V_{rms}}$	7	6	10	5	—
( $\pm 1\%$ Additional Error)					

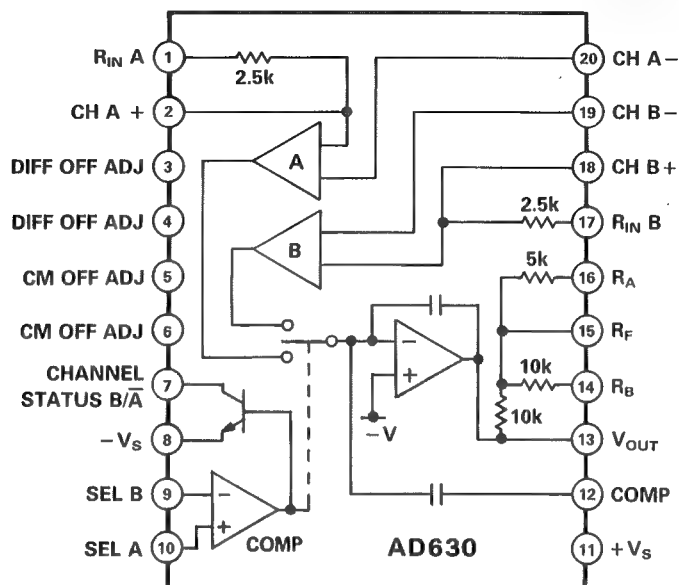
Their operation is quite simple—the two amplifiers in the input stage form an active rectifier which acts as a modulus circuit and drives a unipolar current to the squarer/divider which uses the logarithmic properties of its transistors to perform the function:

$$I_{OUT} = \frac{I_{IN}^2}{I_{FB}}$$

where  $I_{FB}$  is the feedback current from the current mirror which is driven by  $I_{OUT}$ . If we place a capacitor,  $C_{AV}$ , to ground from the  $I_{FB}$  port it will form a low-pass filter with  $R1$  and act as an averager. The output of the whole circuit is taken from a second output from the current mirror—this output flows in a resistor to give a voltage output which may be buffered, if required, by the buffer amplifier. It is obvious that this circuit will perform the implicit rms function described above—some applications are described in the next part of this seminar.

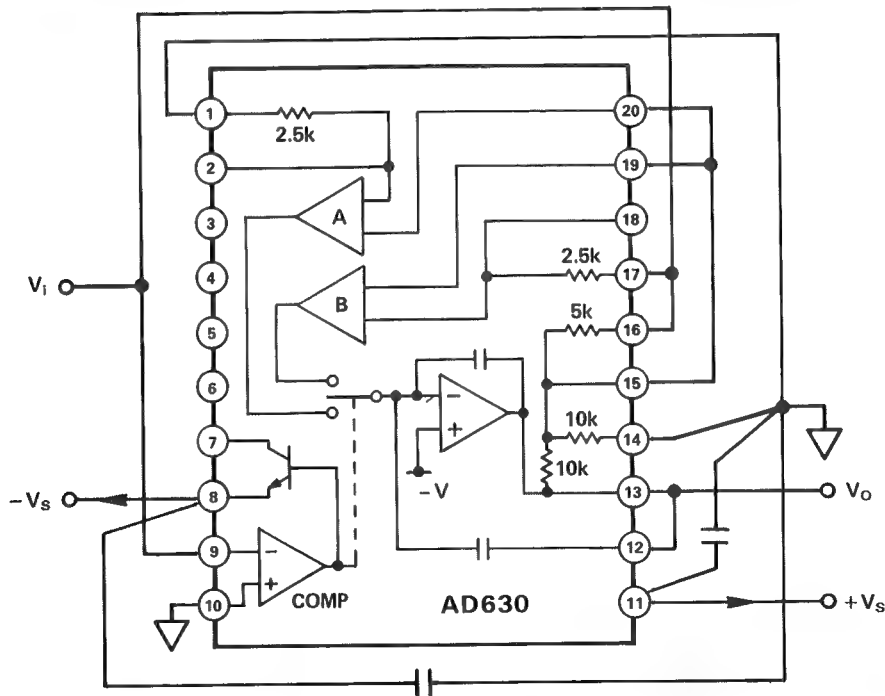
The final member of our collection of analog computational circuits does not use any new or unexpected properties of silicon junctions—it merely reconfigures two operational amplifiers and a comparator to yield a circuit which can be used in many different places. The AD630 contains the input stages of two operational amplifiers, one output stage, a number of laser-trimmed application resistors, and a comparator. The input to the comparator determines which of the two input stages is connected to the output stage.

### AD630 FUNCTIONAL BLOCK DIAGRAM

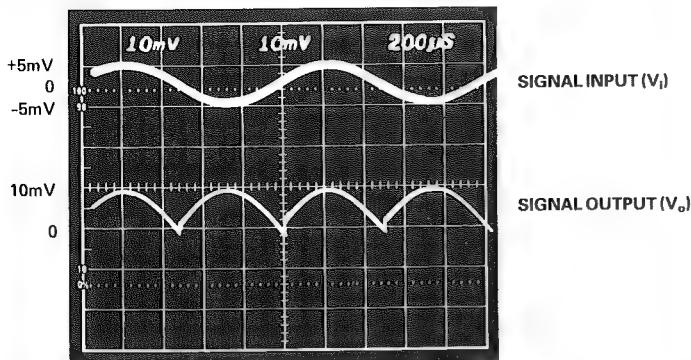


It may, of course, be used as a two-channel multiplexer. If the input stages are configured as inverting and noninverting inputs with the same gain and the same input signal it will act as a modulator if a carrier signal is applied to the comparator (its carrier leak can be as low as  $-66\text{dBV}$  at  $100\text{kHz}$  and improves at lower frequencies) and as a modulus circuit and a precision low-level rectifier if its input signal is also applied to its comparator.

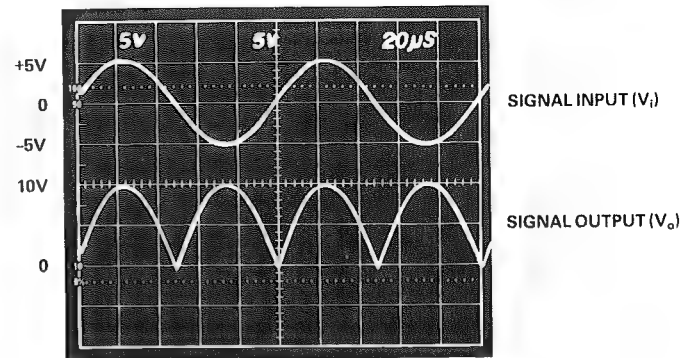
## PRECISION RECTIFIER SCHEMATIC DIAGRAM



### PRECISION RECTIFIER – LOW LEVEL INPUT



### PRECISION RECTIFIER – HIGH LEVEL INPUT



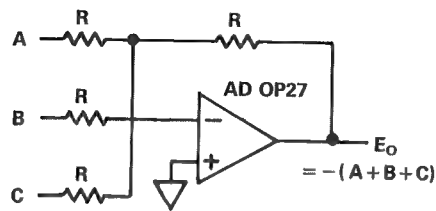
## APPLICATIONS OF ANALOG COMPUTATION CIRCUITS

There are innumerable applications of analog computation circuitry. As emphasized in the introduction to this part of our seminar there is no absolute superiority of analog or digital techniques for computation but there are many more places where analog computation is superior than are presently being used.

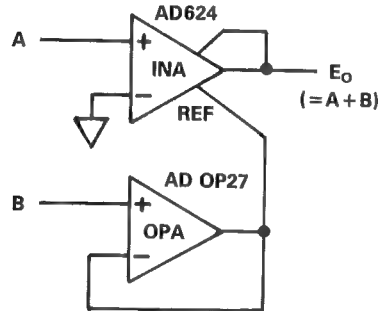
When precision analog computation elements are used (i.e., laser trimmed computation circuitry, op amps with low offset and minimal bias currents, etc.) it will often be found that the theoretical circuit will work almost without modification or trimming—although error budget analysis should always be carried out to ensure that the system performance will remain within specification. We can thus perform the basic algebraic operations of addition, subtraction, multiplication and division on voltages (or currents) with very simple circuitry.

Adders are usually made from an op amp and some resistors but this arrangement is inverting and requires a second inverting amplifier to restore the original polarity. It has, moreover, a relatively low input impedance. Both problems, and the necessity of finding accurate resistors, can be solved by the use of an instrumentation amplifier and an operational amplifier (if the source impedance of the B signal is very low ( $<1\Omega$ ) it may be applied directly to the reference input of the instrumentation amplifier).

## ADDERS



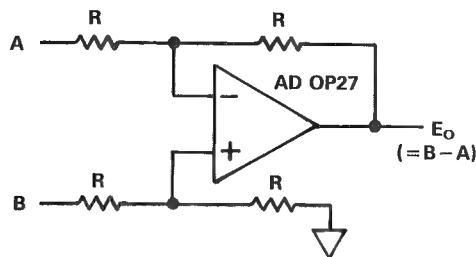
### BASIC INVERTING ADDER



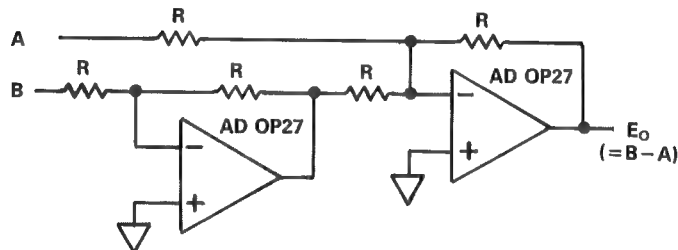
### NONINVERTING ADDER USING AN INSTRUMENTATION AMPLIFIER AND AN OPERATIONAL AMPLIFIER

A subtractor is merely an adder with the sign of one of its inputs reversed. It can be made with an operational amplifier and four equal resistors (but this type must be driven from a very low source impedance), from two operational amplifiers and five resistors (with the same disadvantages as an adder of the same general type), or from an instrumentation amplifier.

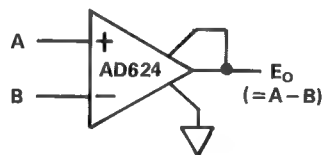
## SUBTRACTORS



### SIMPLE SUBTRACTOR



### MORE COMPLEX (BUT MORE FLEXIBLE) SUBTRACTOR



### HIGH IMPEDANCE SUBTRACTOR WITH INSTRUMENTATION AMPLIFIER

$$E_0 = \frac{(X1 - X2)(Y1 - Y2)}{SF} + Z2$$

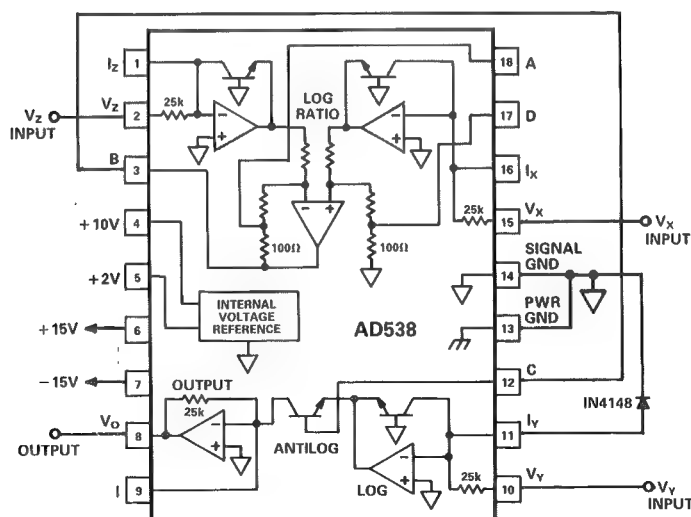
Because the inputs are differential the multiplier will compute the products of differences and will add to the output any voltage applied to the Z2 terminal. It is thus quite a powerful analog computer without any external components whatsoever, and will return its full specified performance of better than 0.25% FS accuracy without external trimming. If the same input is applied to both X and Y ports the basic multiplier functions as a squarer with about half the errors of the XY/10 multiplier.

Figure 1 is a schematic diagram of the AD534 integrated circuit configured as a four-quadrant multiplier. The chip is represented by a central vertical rectangle labeled "AD534".

- Inputs:**
  - X-INPUT:** Two inputs, X<sub>1</sub> and X<sub>2</sub>, are shown at the top left. They are labeled "X-INPUT ±10V FS ±12V PK".
  - SQUARER INPUT:** A single input, SF, is shown in the middle left. It is labeled "SQUARER INPUT ±10V FS ±12V PK".
  - Y-INPUT:** Two inputs, Y<sub>1</sub> and Y<sub>2</sub>, are shown at the bottom left. They are labeled "Y-INPUT ±10V FS ±12V PK".
- Outputs and Connections:**
  - OUT:** The primary output is labeled "OUT" and is connected to a horizontal line. It is also labeled "OUTPUT, ±12V PK".
  - Z<sub>1</sub>:** An input labeled "Z<sub>1</sub>" is connected to the "OUT" line.
  - Z<sub>2</sub>:** An input labeled "Z<sub>2</sub>" is connected to a horizontal line. It is also labeled "OPTIONAL SUMMING INPUT, Z, ±10V PK".
  - Supply Voltages:** The top supply is labeled "+V<sub>S</sub> +15V" and the bottom supply is labeled "-V<sub>S</sub> -15V".
- Equation:** The output equation is given as:
 
$$\text{OUTPUT, } \pm 12\text{V PK} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\text{V}} + Z_2$$

## ONE-QUADRANT COMBINATION MULTIPLIER/DIVIDER

$$V_{OUT} = V_Y \left( \frac{V_Z}{V_Y} \right)$$

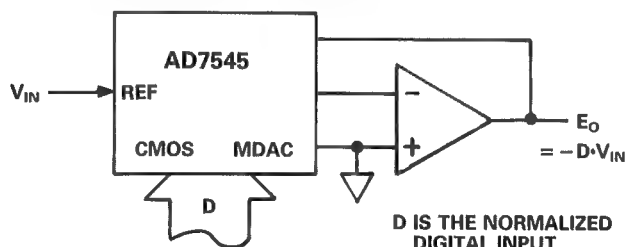




bipolar applications. It also has a lower bandwidth than the fastest transconductance circuits. Its application circuit is almost embarrassingly simple: there are two inputs, an output, and three power pins to connect and two pairs of pins must be short-circuited and one pin must be grounded via a diode.

While not strictly a pure analog technique we should not overlook the multiplying digital/analog converter (MDAC). These circuits multiply an analog input by a digital input and have an analog output, and are very convenient for many computations involving mixed analog and digital variables. A full description of their uses in computation, attenuators, programmable oscillators and filters, and many other applications is given in the data conversion section of this seminar—here we shall merely point out that it is possible to multiply bipolar analog voltages of up to  $\pm 30V$  by unipolar or bipolar digital numbers with resolutions between 8 and 14 bits by using CMOS MDACs in the AD752X, AD753X and AD754X ranges.

## MDAC PERFORMS MIXED ANALOG/DIGITAL MULTIPLICATION



If we connect the output of a transconductance multiplier, such as the AD534, to its Y2 input (with Y1 grounded) and apply external inputs to X and Z (both, being fully differential, may be used with differential or single-ended signals) we find that, because of the negative feedback in the system,

$$\frac{X \cdot (Y1 - Y2)}{10V} = Z$$

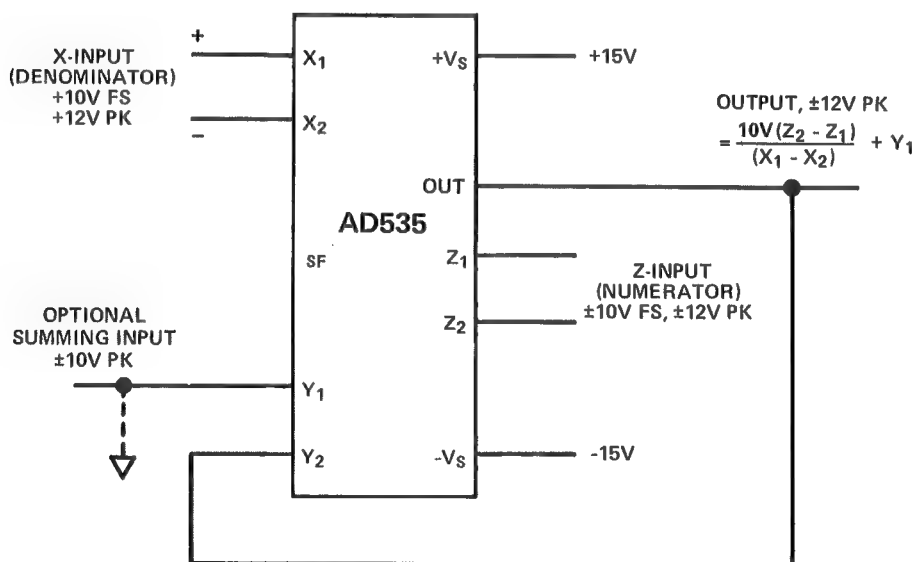
but  $Y2 = E_O$  and  $Y1 = 0$

$$\frac{X \cdot E_O}{10V} = Z$$

and  $E_O = -10V \cdot \frac{Z}{X}$  so that the circuit is a divider.

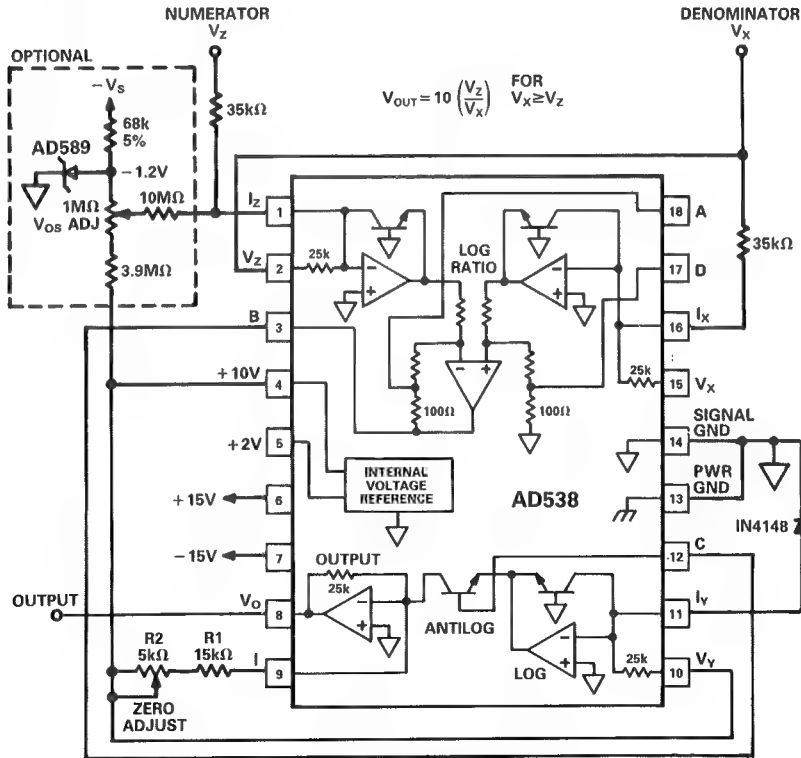
If Y1 is not grounded but has a voltage applied to it that voltage will be added to the output voltage.

## BASIC DIVIDER CONNECTION



The AD538 can, moreover, be used as a two-quadrant divider, even though its inputs accept only unipolar signals. This is done by using the current X and Z input ports and external 35K resistors to enter the numerator and denominator and adding the denominator to the numerator via the numerator voltage input port.

## TWO-QUADRANT DIVISION WITH 10V SCALING



This changes the transfer function from:

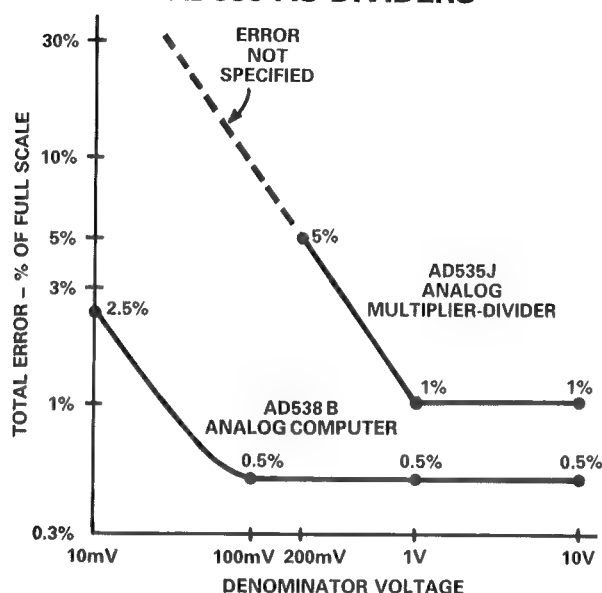
$$V_O = 10V \left( \frac{Z}{X} \right)$$

$$\text{to } V_O = 10V \frac{(Z + BX)}{X} = 10V \left( B + \frac{Z}{X} \right) = 10V \cdot B + 10V \left( \frac{Z}{X} \right)$$

Where  $B = \frac{35K}{25K}$  (the ratio of the input resistors).

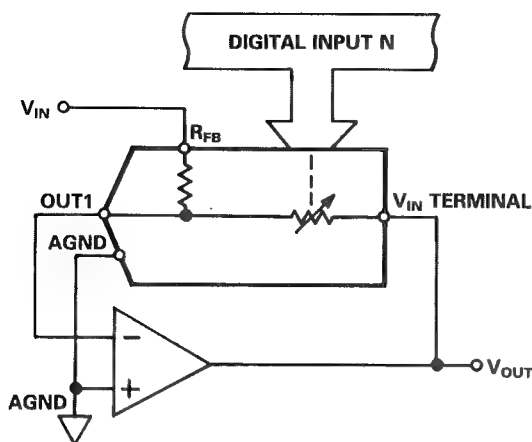
The additional  $10V \cdot B$  is subtracted in the output amplifier using the AD538 reference and an external resistor, R1 (trimmed by a potentiometer, R2, since the absolute values of the internal resistors of the AD538 are not very accurate, even though their matching is very accurate indeed—a penalty of the laser trim technique). The consequence of this operation is that, provided the magnitude of the denominator is greater than the magnitude of the numerator, the numerator may have either polarity and therefore the circuit is a two-quadrant divider.

## COMPARISON OF AD538 AND AD535 AS DIVIDERS



A final technique for division uses a CMOS MDAC as the multiplier in a feedback loop—again it is not a true analog divider but should not be overlooked in systems where both analog and digital signals are present.

## MDAC IN FEEDBACK LOOP MAKES A DIVIDER



### EQUATIONS

$$V_{OUT} = - \frac{V_{IN}}{N}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = - \frac{1}{N} \quad \text{where: } A_V = \text{Voltage Gain}$$

and where:

$$N = \frac{\text{BIT 1}}{2^1} + \frac{\text{BIT 2}}{2^2} + \frac{\text{BIT 8}}{2^8}$$

### EXAMPLES

$$N = 00000000, A_V = -A_{OL} \text{ (OP AMP)}$$

$$N = 00000001, A_V = -256$$

$$N = 10000000, A_V = -\frac{256}{128} = -2$$

$$N = 11111111, A_V = -\frac{256}{255}$$

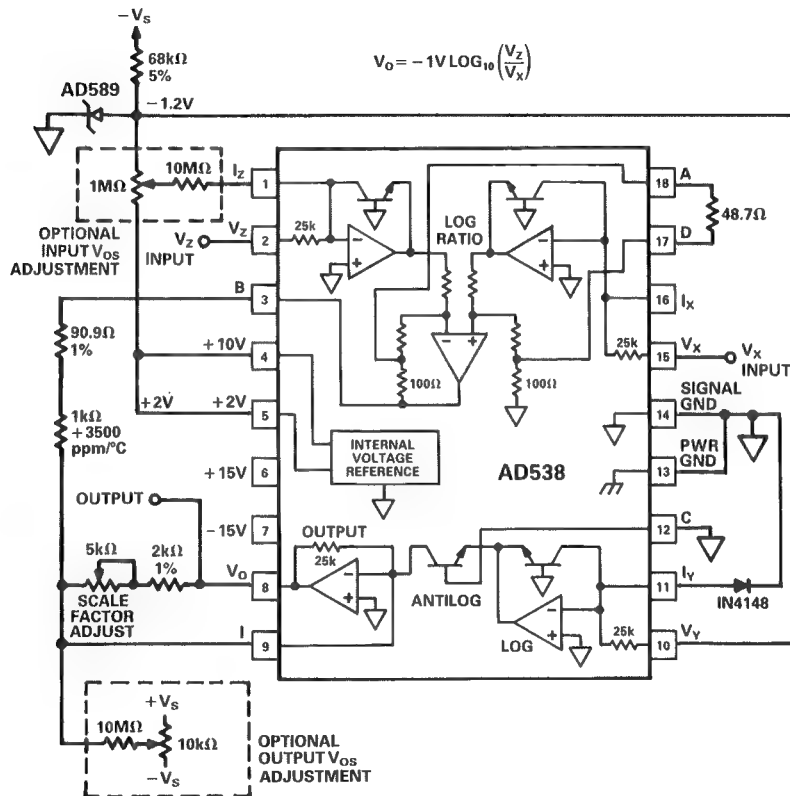
Everyone knows that division by zero yields infinity. When mathematics is performed with a pencil and paper this is acceptable—when it is performed with electronics and the output is a voltage we might expect division by zero to yield sparks and a smell of ozone. In fact division by too small a denominator will result in the divider output limiting near to one or other of the supplies, and the use of larger, but still small, denominators will tend to reduce accuracy and system bandwidth. It is important to calculate the expected accuracy at the extremes of the input ranges from the device data and to choose a device which will give the performance required. It is also important to choose a realistic performance, consistent with the total system, rather than demand the highest possible performance because it is within the state-of-the-art.

Many more complex mathematical operations are barely more difficult to perform than the basic  $+$ ,  $-$ ,  $\times$ , and  $\div$ . Logarithmic circuits will easily compute logarithms and powers and the AD538 will also compute arc tangents more quickly than most digital techniques and more accurately than any other analog ones.

The most serious drawback of the diode logarithm circuit, as we discussed earlier, is that the output contains a  $kT/q$  term and is temperature dependent. This temperature variation may be compensated by the use of a  $+3500\text{ppm}/^\circ\text{C}$  temperature variable resistor\*. The log ratio circuit shown has better than 0.5% accuracy for over 60dB dynamic range of inputs (10mV to 10V).

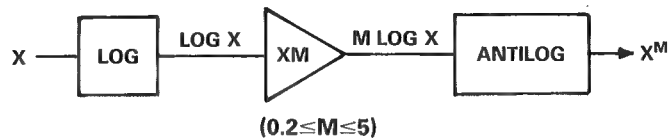
\*Available from Tel Labs Inc., 154G, Harvey Road, Londonderry, NH 03053. Tel: (603) 625-8994 Twx: (710) 220-1844.

## LOG RATIO CIRCUIT

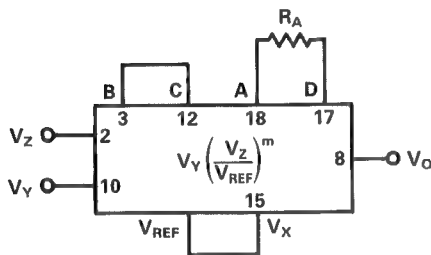


In a logarithmic circuit like the AD538, which contains log and antilog circuits and an amplifier, all that needs to be done to raise an input  $X$  to the  $M$ th power ( $0.2 < M < 5$ ) is to set the amplifier gain to  $M$ , which can be done with one or two resistors, depending on whether  $M > 1$  or  $M < 1$  (if  $M = 1$  no external resistors are necessary but who wants a unity power circuit?)

## HOW AN AD538 COMPUTES POWERS

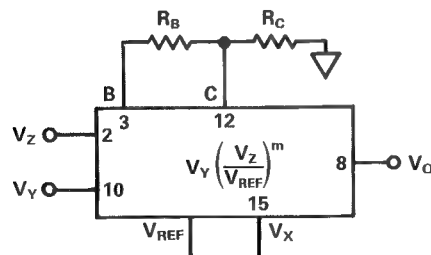


## HOW TO SET VALUES OF M



### POWERS

m	$R_A$
2	196 $\Omega$
3	97.6 $\Omega$
4	64.9 $\Omega$
5	48.7 $\Omega$



### ROOTS

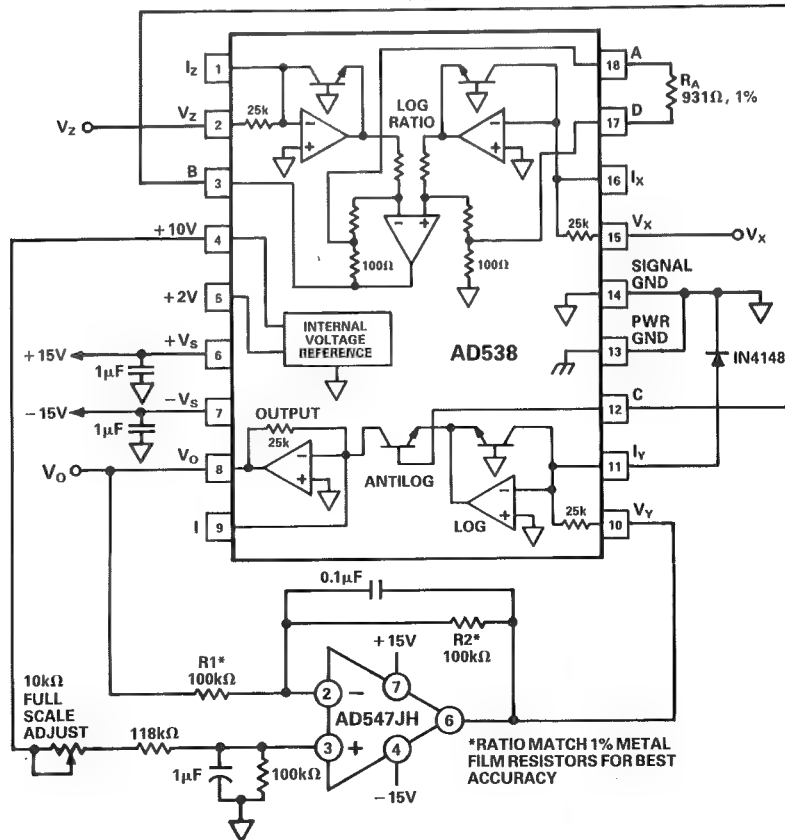
m	$R_B$	$R_C$
1/2	100 $\Omega$	100 $\Omega$
1/3	100 $\Omega$	49.9 $\Omega$
1/4	150 $\Omega$	49.9 $\Omega$
1/5	162 $\Omega$	40.2 $\Omega$

The arc-tangent circuit shown is typical of AD538 applications where Y is 1 so that  $V_O = \left(\frac{Z}{X}\right)^M$  for  $M < 1$ .

In an approximation to the arc-tangent function the AD538 may be made to compute the angle represented by two rectangular coordinates which, since they are applied to the X and Z inputs, we shall call X and Z rather than the more usual X and Y. If X and Z are within the range  $100\mu\text{V}$  and  $10\text{V}$  the error in the computed angle is under  $1^\circ$  (the AD639 can do a similar computation with fewer components but cannot work over as wide a dynamic range).

## THE ARC-TANGENT FUNCTION

$$V_\theta = [V_{\theta\text{REF}} - V_\theta] \times \left(\frac{V_z}{V_x}\right)^{1.21} \quad \theta = \text{TAN}^{-1}\left(\frac{Z}{X}\right)$$



The circuit exploits the fact that

$$T = \frac{(\tan T)^{1.21}}{1 + (\tan T)^{1.21}}$$

Where T is the angle normalized to  $90^\circ$ .

The AD538 and the external amplifier calculates  $\log(\tan T)$  from X and Z, amplifies it by a factor of 1.21 to raise to the 1.21 power and performs an implicit calculation to calculate the angle (which is expressed in terms of the reference voltage). Under these conditions the output voltage tends to  $V_{\text{REF}}$  as the angle tends to  $90^\circ$  although, in fact, the circuit cannot be used much above  $89.5^\circ$  because at  $90^\circ$  tangents become infinite and before then the circuit becomes unstable. R1 and R2 must be matched for highest accuracy, and the circuit is stabilized by the  $0.1\mu\text{F}$  integrating capacitor in the amplifier feedback path. The circuit works in a single quadrant since both X and Z must be positive.

Trigonometrical functions are more normally calculated by the AD639. No external components (other than supply decoupling capacitors) are required to compute sines, cosines, tangents and cotangents, and secants and cosecants with the AD639. Little more than an extra reference voltage (which may be generated from the internal reference with an operational amplifier and a couple of resistors) are required for versines and coversines. For details of the less common functions the reader should consult the AD639 datasheet and various application notes—the sine, cosine, and tangent will be described here.

## THE AD639 WILL COMPUTE

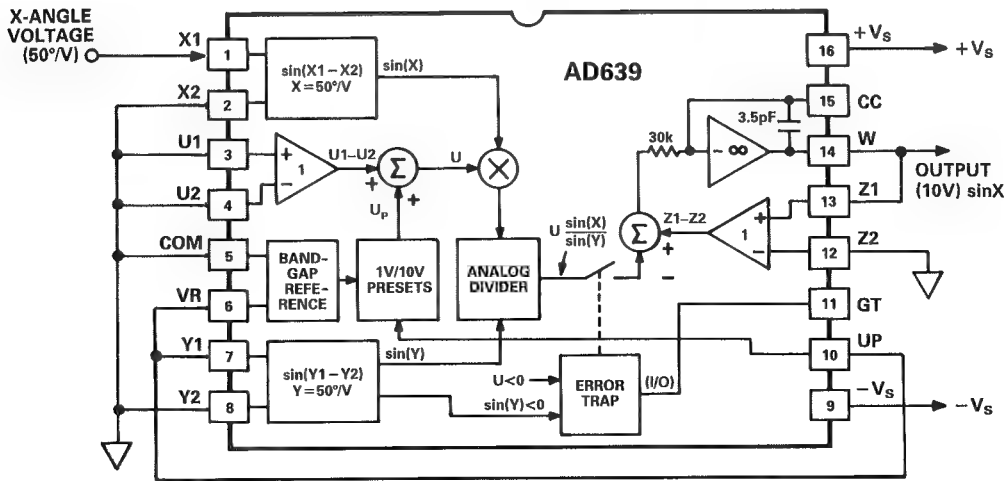
- Sine
- Cosine
- Tangent
- Cotangent
- Secant
- Cosecant
- Versine
- Coversine
- Exsecant
- Etc . . .

AND  
THEIR  
INVERSE  
FUNCTIONS

MOSTLY WITHOUT EXTERNAL  
COMPONENTS

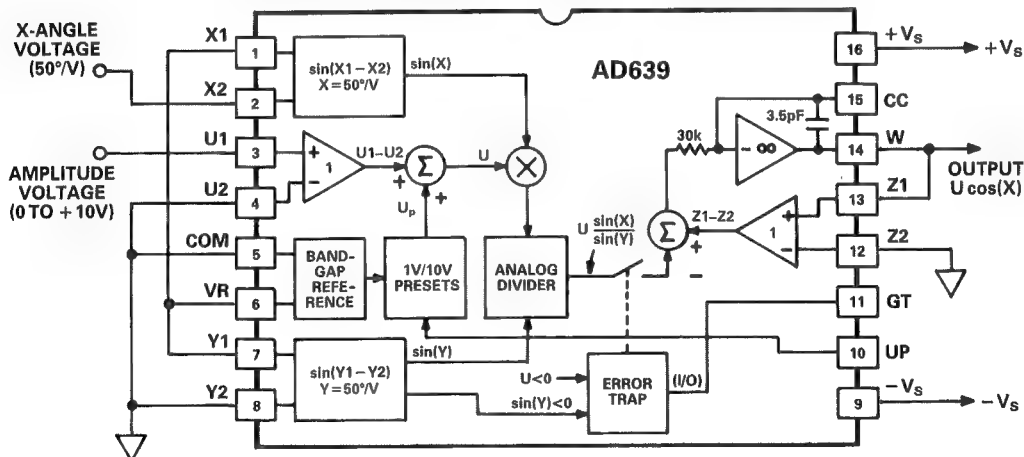
The sine circuit functions from  $-500^\circ$  to  $+500^\circ$  with best accuracy between  $-90^\circ$  and  $+90^\circ$ . Different scale factors may be selected by different connections of U1, U2 and UP.

### CONNECTIONS FOR THE SINE MODE WITH AMPLITUDE PRESET TO 10V



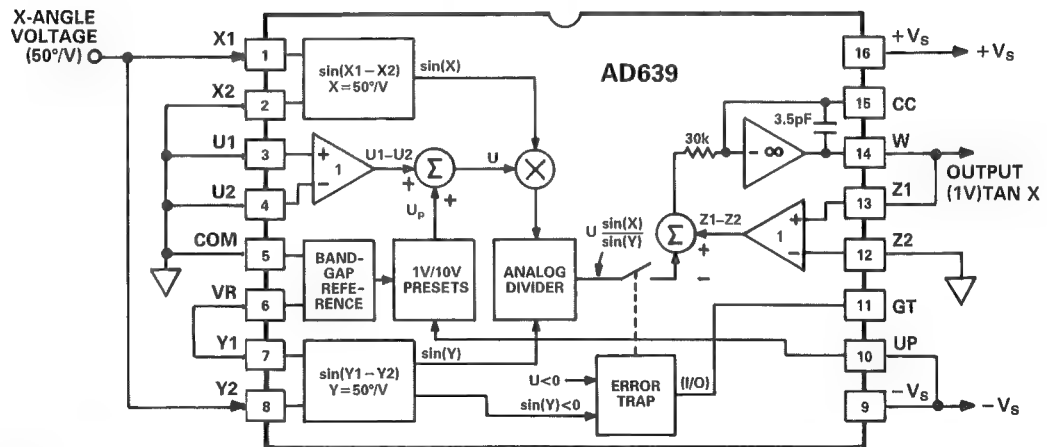
The cosine circuit differs from the sine only in that the X1 input is offset by the internal reference (preset to  $1.8V (=90^\circ)$ ) and the input is applied to the inverting X input  $-X2$ . Its angular range reflects the offset, being  $-400^\circ$  to  $+600^\circ$ , and its best accuracy is between  $0$  and  $180^\circ$ .

### CONNECTIONS FOR THE COSINE MODE WITH EXTERNAL AMPLITUDE CONTROL



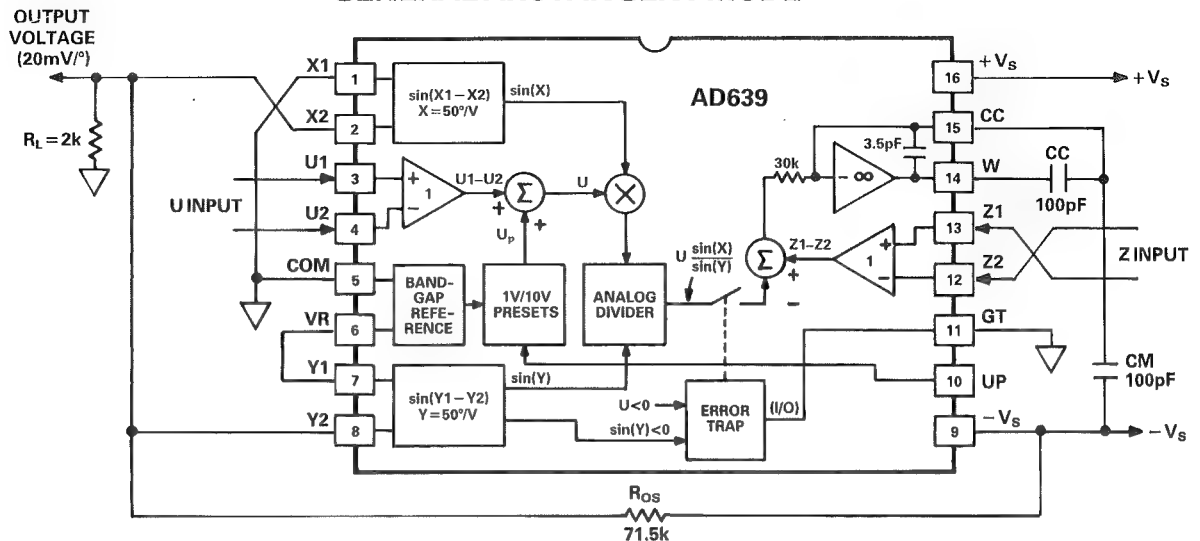
The computation of the tangent requires sine input to the X input and cosine (i.e., negative sine offset  $90^\circ$ ) to the Y inputs. For inputs above  $\pm 85^\circ$  the outputs, even if scaled to 1V, will go out of the operating range of the amplifier with a  $\pm 15V$  supply—instead the internal error trap operates and the output returns to zero while a warning flag is set on pin 11.

### CONNECTIONS FOR TANGENT MODE WITH AMPLITUDE PRESET TO 1V



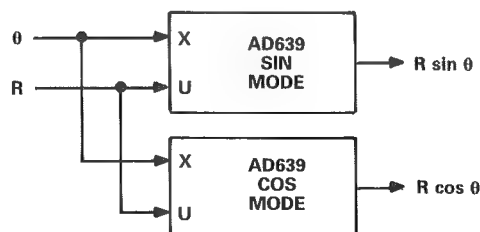
With the AD639 inverse trigonometrical functions are almost as easily computed as direct ones, although normally only the principal angular range is available ( $-90^\circ$  to  $+90^\circ$  for arc sine,  $0^\circ$  to  $+180^\circ$  for arc cosine, etc.). Although the AD639 contains an operational amplifier so that the inverse mechanism we keep explaining—a function generator in a negative feedback loop generates an inverse function—may be used yet again, some extra circuitry, mostly resistors, is necessary because the AD639 has low resistance inputs (only 3.6K to common) and therefore loads any circuitry driving it. The basic arc-tangent circuit is shown in the diagram and its operation, and that of the arc-sine and arc-cosine circuits, is described in the data sheet.

### CONNECTIONS FOR THE GENERAL ARCTANGENT MODE



The AD639 tangent and act-tangent circuits may be used, with other circuitry such as the AD630 and the AD534, to perform coordinate conversion from Cartesian (X, Y) to polar (R,  $\tau$ ) or vice versa.

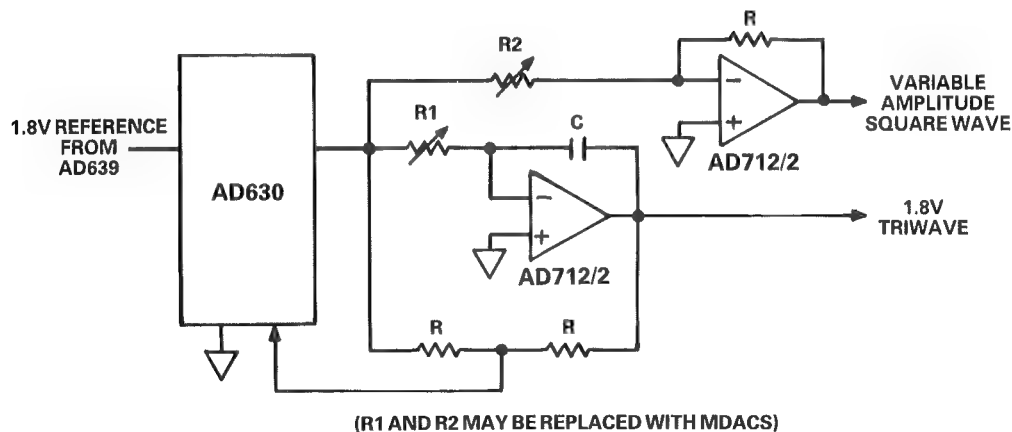
### POLAR-CARTESIAN COORDINATE CONVERTER



When the AD639 is described on its data sheet as a function generator the description is accurate, but it can be misleading since the term 'function generator' is frequently applied to a piece of testgear—an oscillator having sine, triangular, and squarewave outputs. The AD639 is not an oscillator.

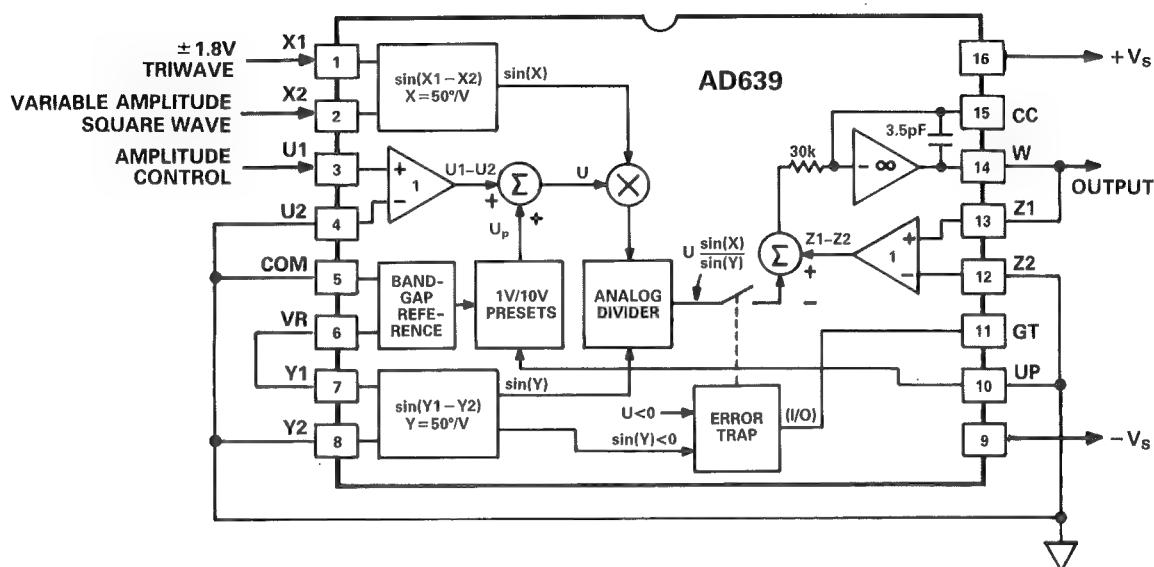
Nevertheless the AD639 may be used to convert a triangular waveform into a sinewave and, if a squarewave is available in quadrature to the tri-wave, the phase of the output sinewave may be varied continuously merely by varying the squarewave amplitude. The tri-wave required for this application has an amplitude of  $\pm 1.8\text{V}$  and may be generated very easily with an AD630 and an op amp, using the  $1.8\text{V}$  reference from the AD639 itself. The frequency of oscillation is set by  $R1$  and  $C$ —if digital control of frequency is required  $R1$  might be replaced with a CMOS MDAC—and the amplitude of the squarewave (which controls the phase of the AD639 output) is set by  $R2$ —which again could be replaced by a CMOS MDAC for digital control of phase.

### AD630 TRIWAVE GENERATOR



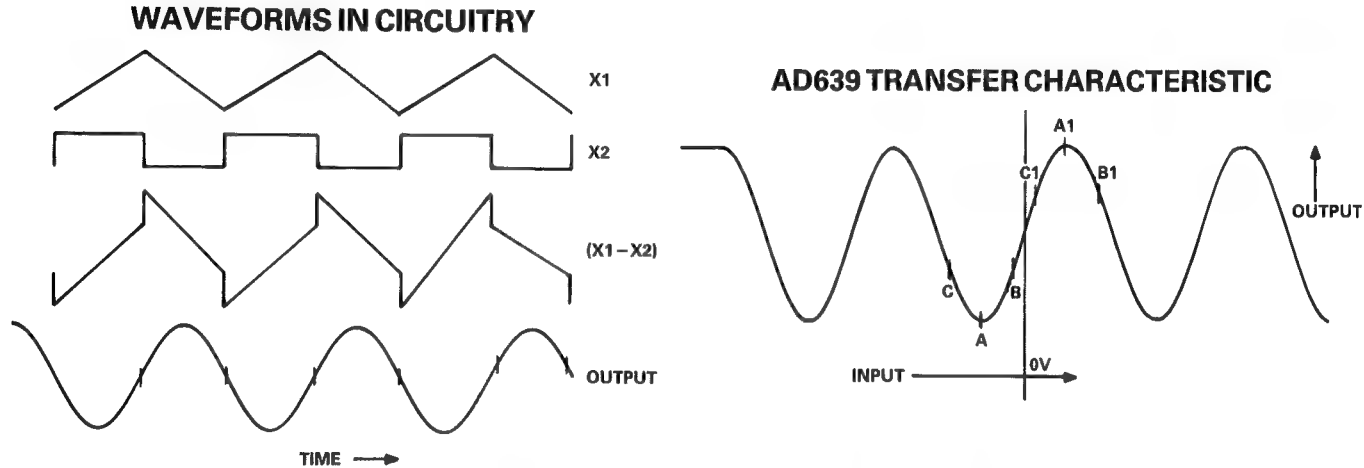
The triwave is applied to the X1 terminal of the AD639 and the squarewave to the X2 terminal. The Y port is connected to the reference (Y1) and ground (Y2) to bias the internal divider, but is otherwise unused. The output amplitude may be preset with the UP terminal or may be varied by applying a control voltage to U1 (again if digital control of amplitude is required this terminal might be driven by a DAC).

### VARIABLE-PHASE SINEWAVE GENERATOR





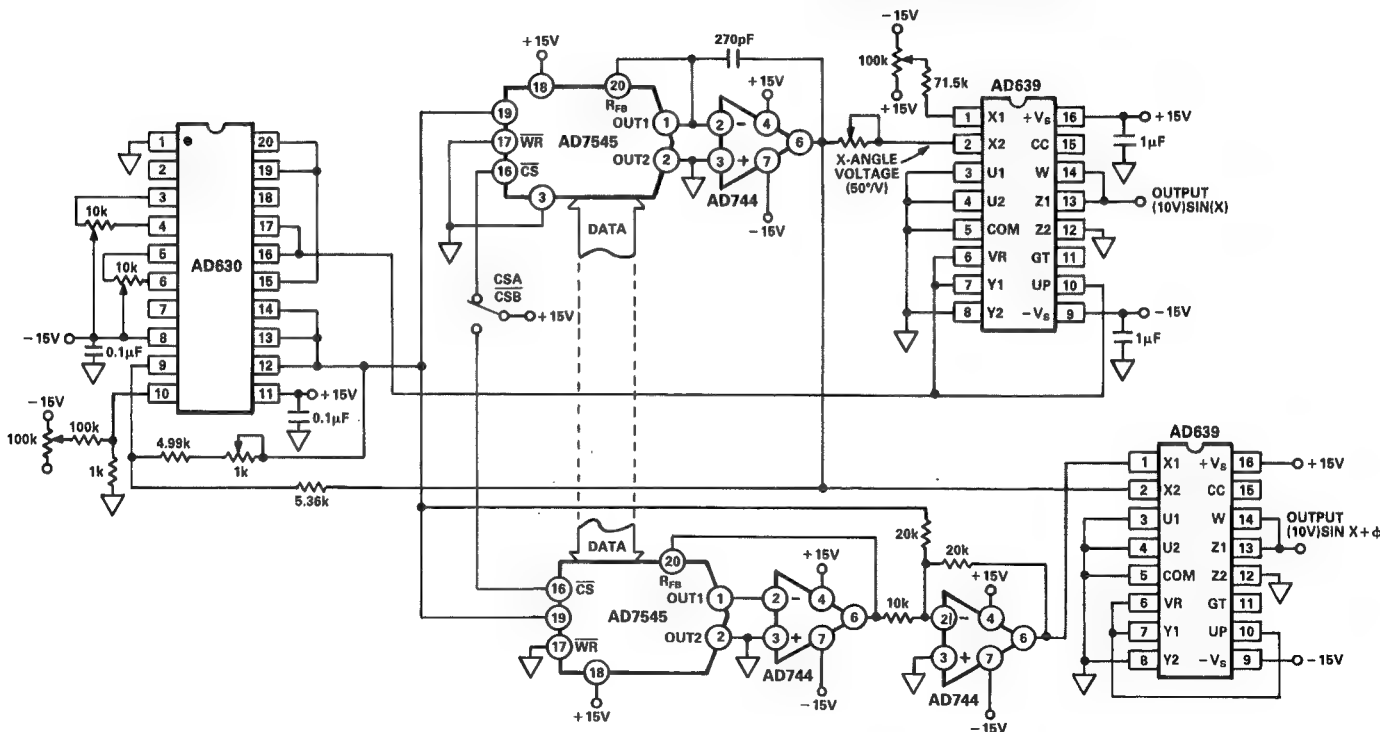
The operation of the circuit may be appreciated by first considering the case where the squarewave input has zero amplitude (i.e., X2 is grounded). As the triwave goes from  $-1.8\text{V}$  to  $+1.8\text{V}$  the output goes from A to A1 on the transfer characteristic (on the bottom line of the diagram) and then, as it goes from  $+1.8\text{V}$  to  $-1.8\text{V}$ , the output goes back from A1 and A. Thanks to the sinusoidal transfer function of the AD639 this linear cycling of the input produces a sinewave at the output.



If we now restore the squarewave to the X2 input, the output cycles from B to B1 and then, as the squarewave switches, jumps to C1 and cycles to C on the negative-going half of the triwave. At C the squarewave switches again and the output cycles back from B to B1 again. The effect at the output is a sinewave formed by sections B1 to B and then C to C1 of the AD639 transfer characteristic. Since there are jumps from B to C and from C1 to B1 when the squarewave switches there are small glitches on the output waveform where the jump occurs but they are generally insignificant because if the squarewave is symmetrical (equal positive and negative amplitudes) the values of B and C and or C1 and B1 are identical so the glitch is only the spike which gets past the output amplifier filter, not an overall change of level.

With the waveforms shown in the diagram increasing the squarewave amplitude increases the phase delay (lag) in the output waveform—if the phase of the squarewave is reversed the sinewave will, of course, lead the triwave, the squarewave in either case is  $90^\circ$  out of phase with the triwave—in the diagram it leads it.

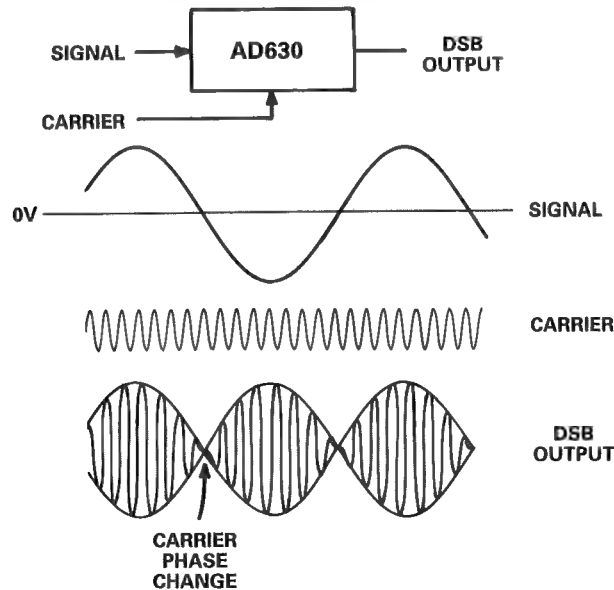
## PROGRAMMABLE FREQUENCY AND PHASE SINEWAVE GENERATOR



The AD630 will do a lot more than merely generate triwaves to drive the AD639. As mentioned above it will function as a modulus circuit giving a unipolar output with the same magnitude as its input (and a logic output indicating the polarity of the input), it will act as a two-channel multiplexer/buffer, and it will act as a high-performance modulator/demodulator.

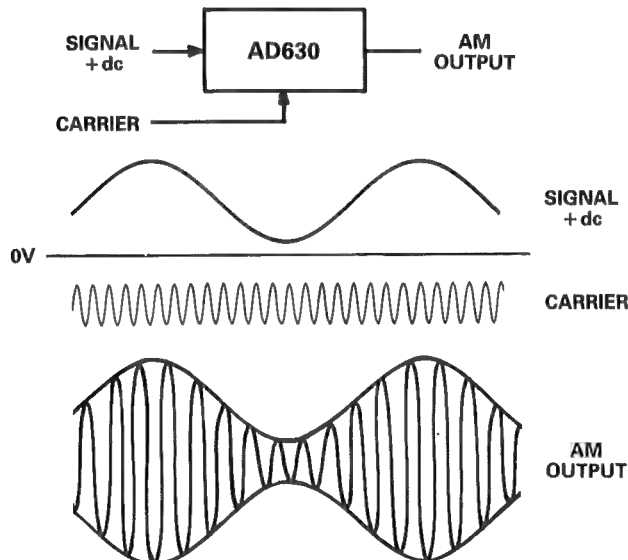
Modulator/demodulator circuits are quite common, and are available working at much higher frequencies than the AD630. Its contribution to the technology is its laser-trimmed precision—it has very low offset (and hence low carrier leak) and accurate gain. It is unsuitable for higher speed applications, or ones where cost is important and precision is not (the industry standard 1496 and 1596 were intended for such applications) but wherever precision is needed the AD630 has real advantages. As a modulator it has low carrier leak and high accuracy. If a signal is applied to the AD630 signal port and about 50mV rms of carrier to the comparator the output will be a double sideband signal (DSB or 'suppressed-carrier' AM).

### BALANCED MODULATOR PRODUCES DSB SIGNAL



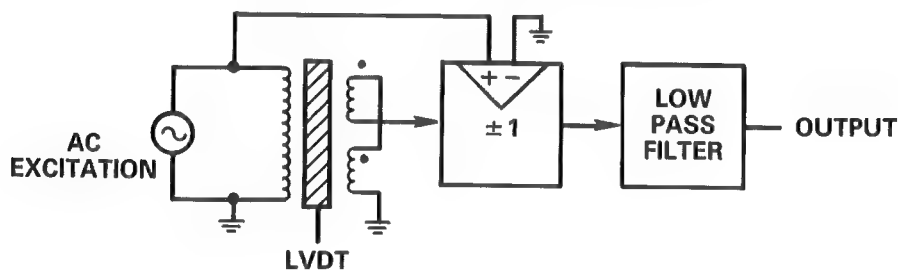
Many people expect amplitude modulation from such a circuit but in fact to obtain AM either the signal input must have a dc offset or carrier leak must occur (possibly by adding carrier to the signal input).

### CARRIER LEAK CAUSES DSB TO BECOME AM



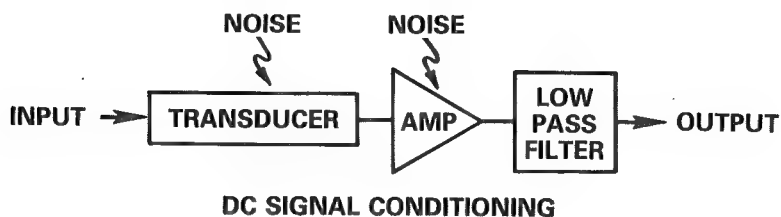
A modulator/demodulator will also function as a phase-sensitive rectifier. An application where a very accurate phase-sensitive rectifier is required is the demodulation of LVDT signals. A linear variable displacement transducer (LVDT) is a device for sensing position which consists of three coils, a primary and two secondaries connected in series antiphase. The secondaries are positioned on either side of the primary and the amount of flux in each depends on the position of a moving core—when the core is central there is equal flux in each secondary and the total output is zero. If the core is displaced one secondary will be linked by more flux than the other and the total output is not zero. The output amplitude and phase of the whole thing depends on the position of the core and an AD630 is ideal for converting this to a bipolar dc position signal.

### LVDT SIGNAL DEMODULATOR



Whole libraries have been written on applications of modulators and demodulators which we do not have space to review here, but there is one more application where the exceptional accuracy of the AD630 is particularly useful—synchronous demodulation. Many transducers have relatively small outputs and are often in locations where they are vulnerable to electrical noise, and dc amplifiers are liable to drift and to cause low frequency noise on their own account. In such circumstances noise may swamp a wanted signal.

### SMALL DC SIGNALS ARE EASILY LOST IN NOISE



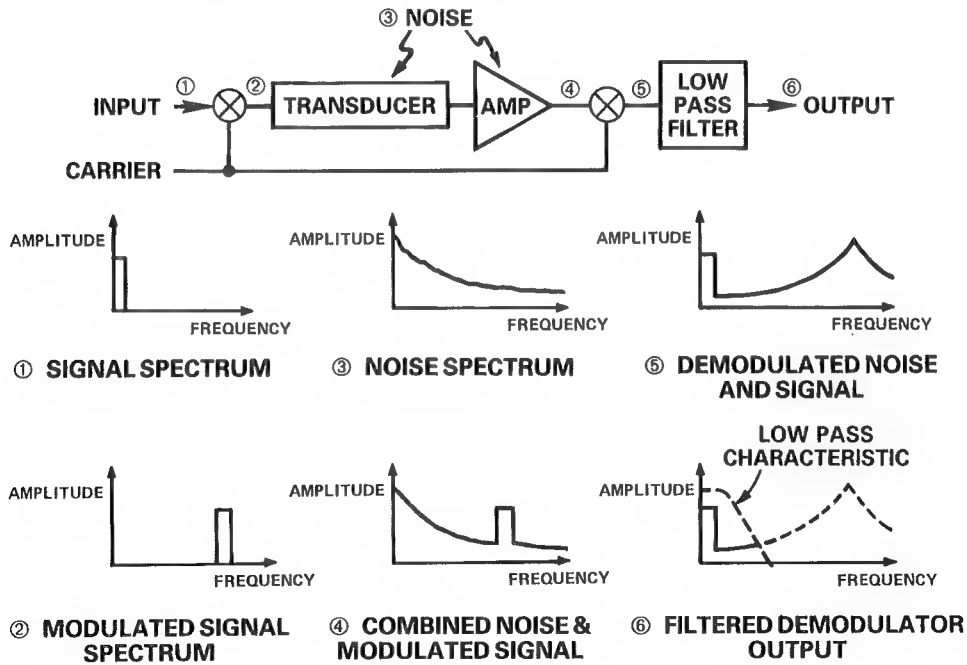
NOISE CHARACTERISTICS



SIGNAL CHARACTERISTICS

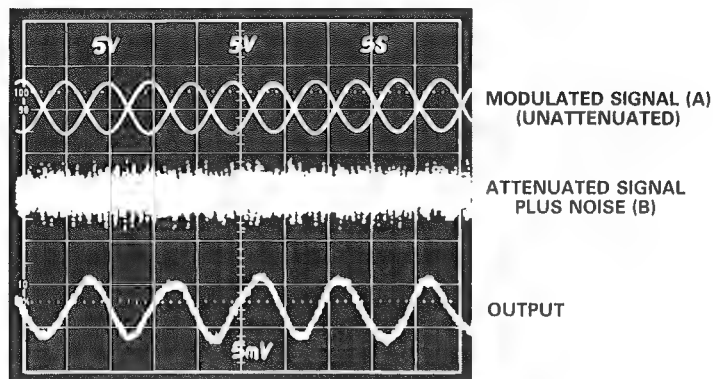
If we can use the signal to modulate a carrier—perhaps by energizing a transducer with ac rather than dc, perhaps by chopping the dc transducer output, or perhaps even by chopping the physical input to the transducer. We can then amplify the resultant ac signal, filter dc and LF noise, and, by synchronous demodulation, recover the original signal. It is more helpful to consider the operation in the frequency domain than the time domain.

## AC SIGNAL CONDITIONING FREQUENCY DOMAIN ANALYSIS



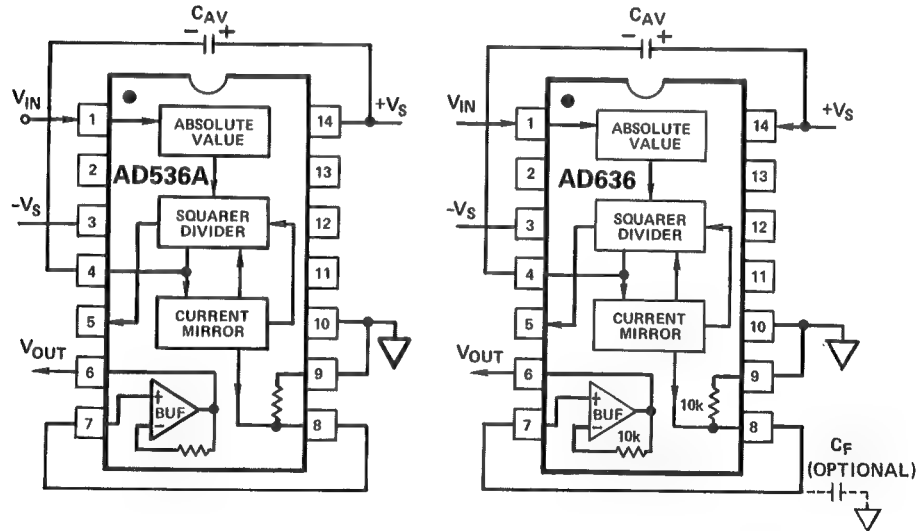
Finally the oscilloscope photograph shows how this technique may be used to recover information modulated on a carrier and buried in white noise 100dB stronger than itself.

## LOCK-IN AMPLIFIER WAVE FORMS

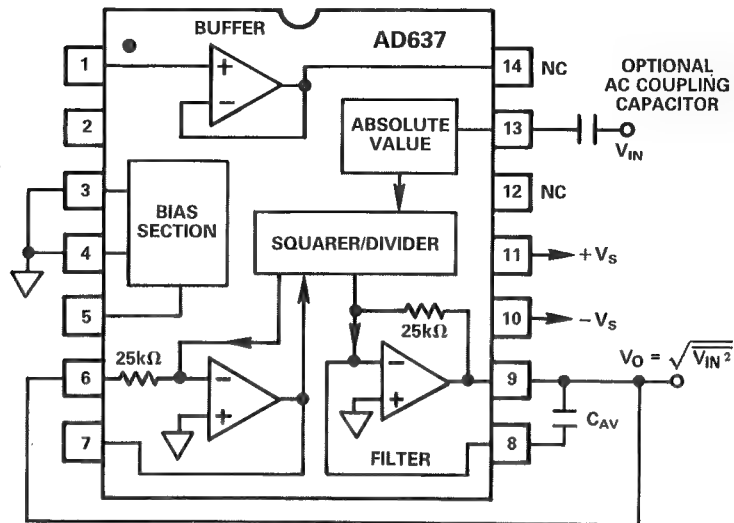


The final computational circuit whose applications we shall consider is the rms/dc converter\*. Obviously its main use is the computation of the rms value of an input signal which is generally ac but may be modulated dc of some sort. Although offset trims will improve performance slightly the only external component required is the integrating capacitor.

### AD536A/AD636 STANDARD RMS CONNECTION

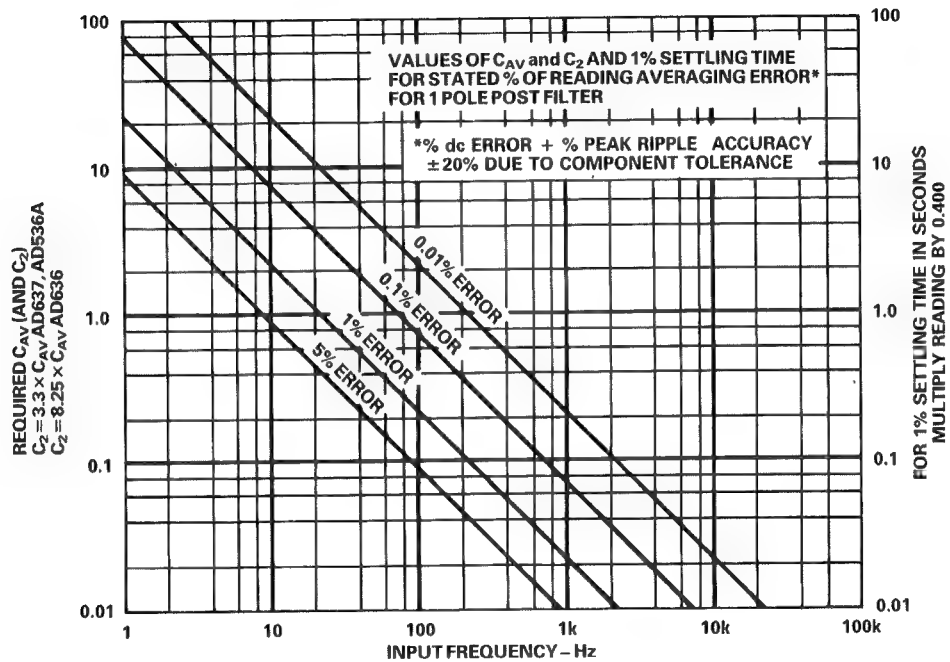


### AD637 STANDARD RMS CONNECTION



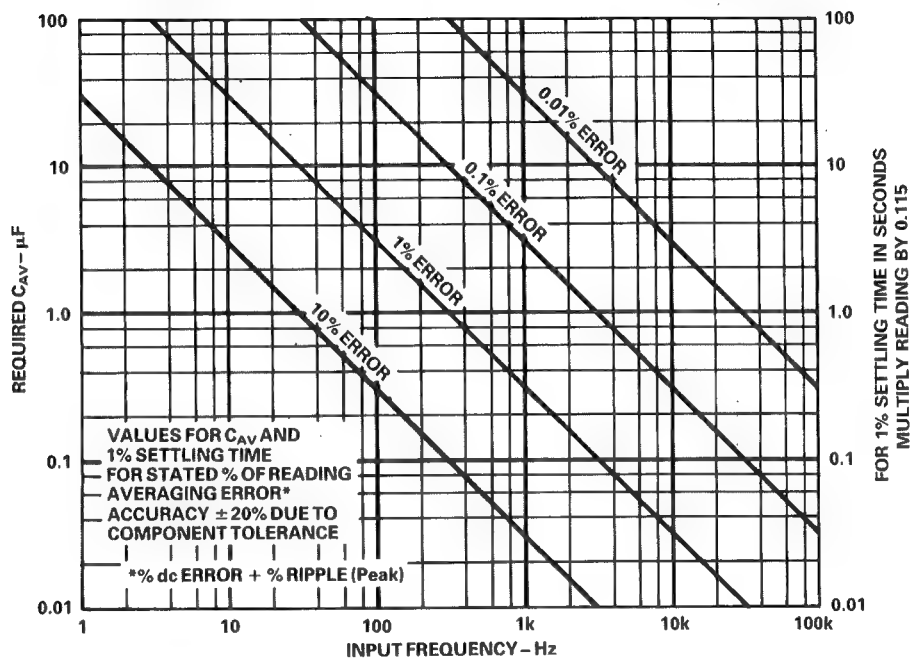
\*For detailed discussion see "RMS to DC Conversion Application Guide – 2nd Edition" – Analog Devices, 1986.

## ERROR/SETTLING TIME GRAPH FOR USE WITH 1-POLE OUTPUT FILTER CONNECTION

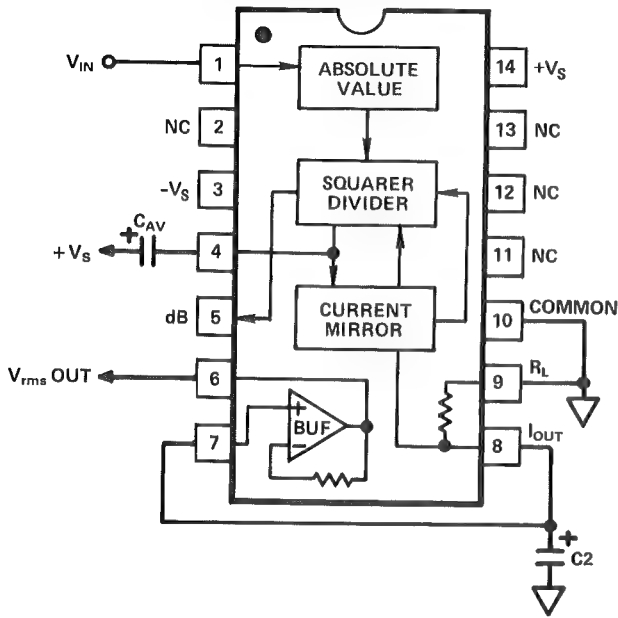


An extra stage of output filter will improve the ripple and the settling time (note that the settling time is twice as long after step reductions of input than after step increases—this is due to the averaging capacitor charging from a current source but discharging through a resistor).

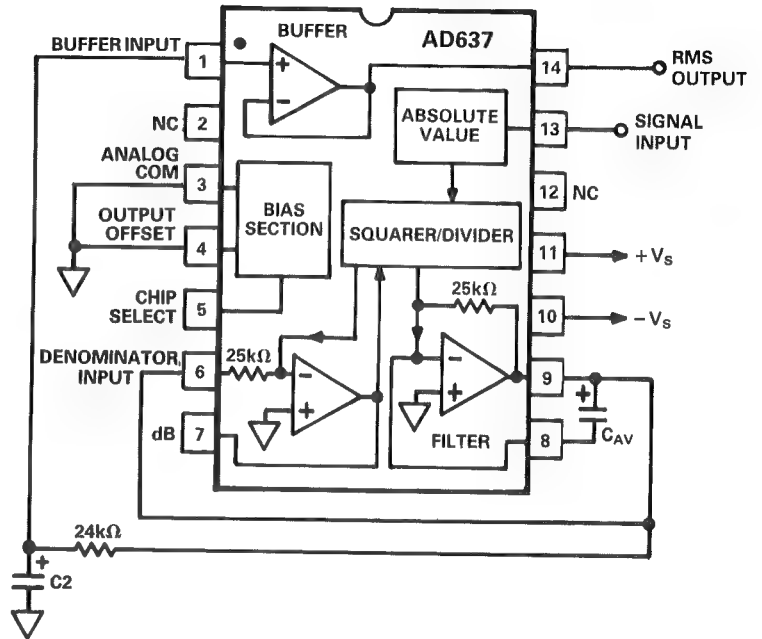
## ERROR/SETTLING TIME GRAPH FOR USE WITH THE STANDARD RMS CONNECTION



### AD536A/AD636 WITH A 1-POLE OUTPUT FILTER

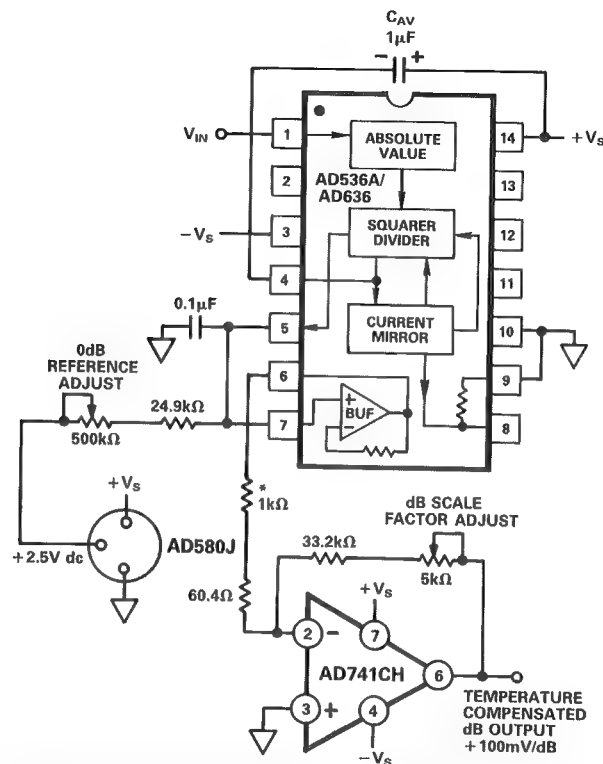


### AD637 WITH A 1-POLE OUTPUT FILTER



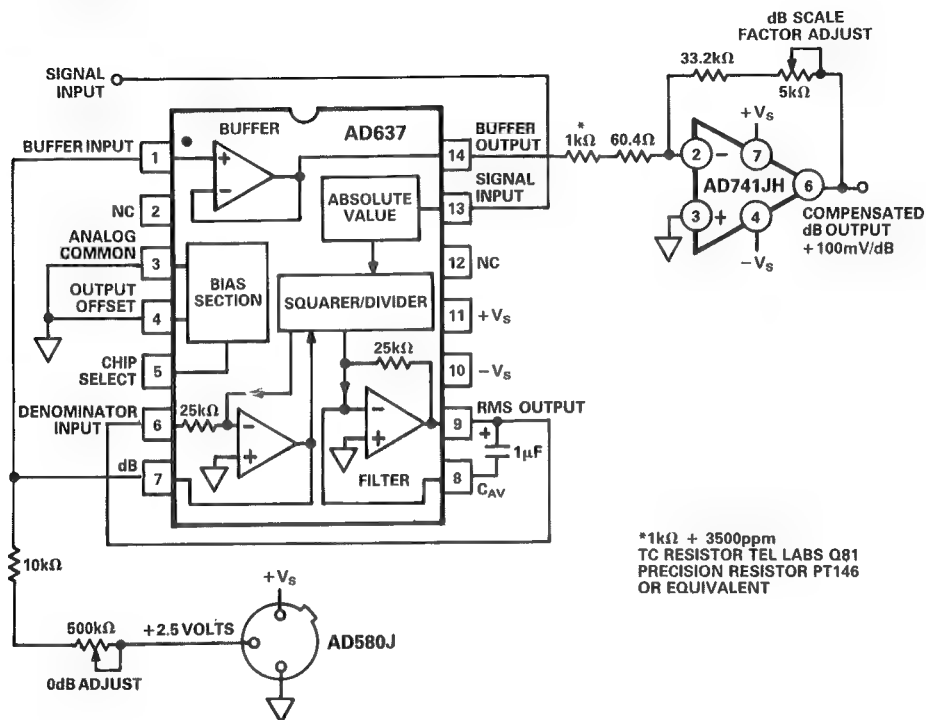
The dB output of the rms/dc converters is another useful circuit function. The output voltage changes by 3mV/dB if the dB terminal is driven by a constant current (which provides an  $I_{ES}$  reference for the dB stage). This voltage has a very high output impedance and it is also proportional to  $kT/q$  so it must be buffered with a buffer whose gain has a  $q/kT$  characteristic to compensate. This is quite easily done with the +3500ppm/°C resistor type mentioned earlier.

### AD536A/AD636 TEMPERATURE COMPENSATED dB OUTPUT CIRCUIT



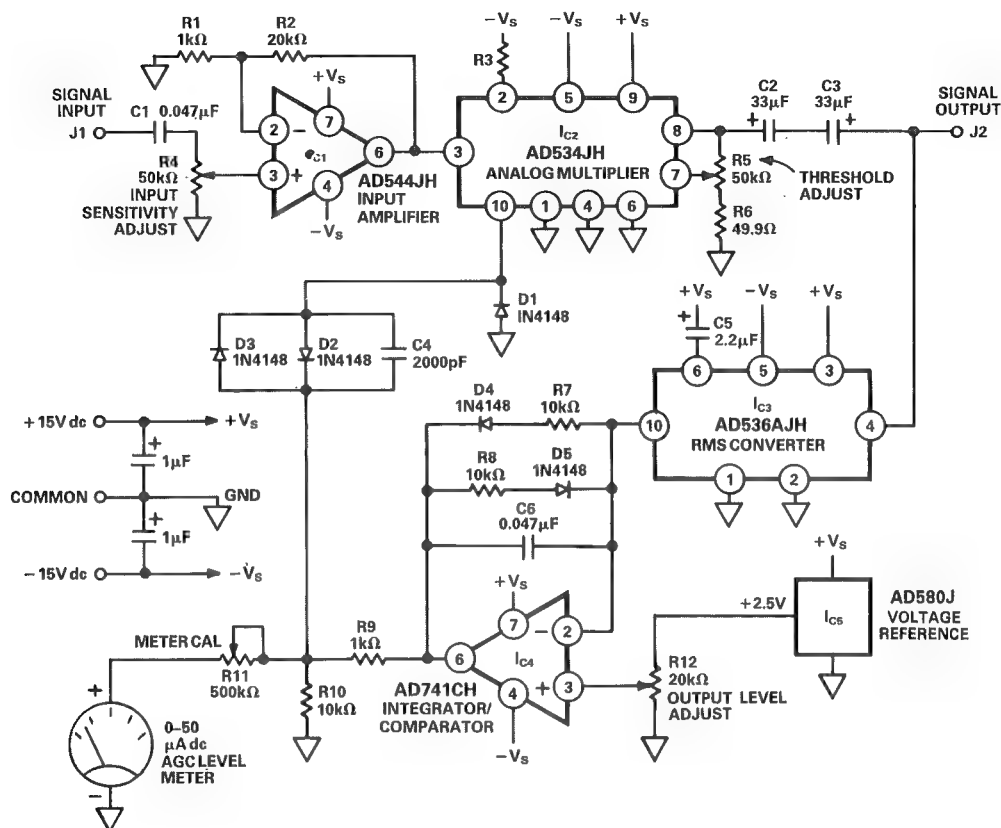
\*SPECIAL TC COMPENSATION RESISTOR +3500ppm 1% TEL LABS Q-81  
PRECISION RESISTOR CO #PT146 OR EQUIVALENT

## AD637 TEMPERATURE COMPENSATED dB CIRCUIT



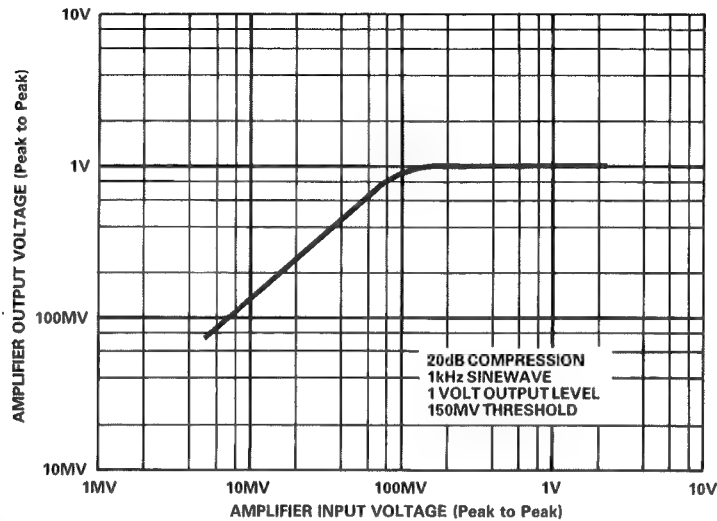
The output of an rms/dc converter may be used to set the gain of an amplifier in an automatic gain control (agc) system so that the output amplifier runs at constant output power.

## AN AUDIO RMS AGC AMPLIFIER



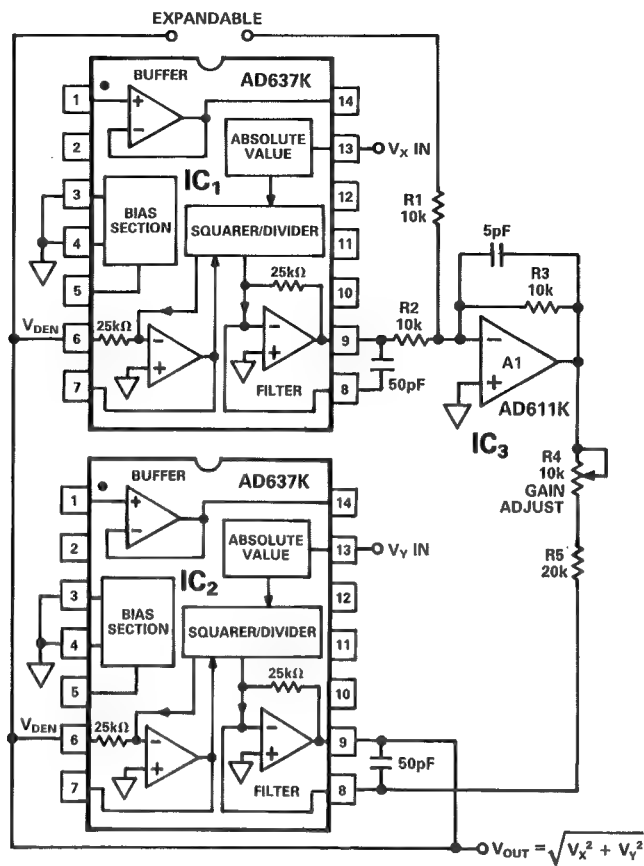


## INPUT VS OUTPUT—AUDIO RMS AGC AMPLIFIER



The last application of rms/dc converters is in vector summation. If we connect two or more AD637s in the circuit shown and their inputs are  $X_1$ ,  $X_2$  etc. the output of the system is  $\sqrt{X_1^2 + X_2^2 + X_3^2 + \dots}$ . This is another implicit calculation (the output is fed back to all the denominator inputs) and gives better accuracy and a wider dynamic range (60dB) than the explicit calculation.

## A VECTOR SUMMATION CIRCUIT



## CONCLUSION

This presentation on the uses of analog computation cannot be exhaustive. It has merely touched the surface of what computation and other circuit techniques are possible with precision laser-trimmed analog computation circuits. It if has given a slight insight into what can be done, however, it will have achieved its purpose—to encourage engineers to consider analog as well as digital solutions to computational problems. Once this is done there will be no need to urge more use of analog circuitry—it will be the obvious and cost-effective solution to many circuit and system problems.

The author would like to close, however, by offering a small gift to cut out and stick in your auto window:

# THINK ANALOG



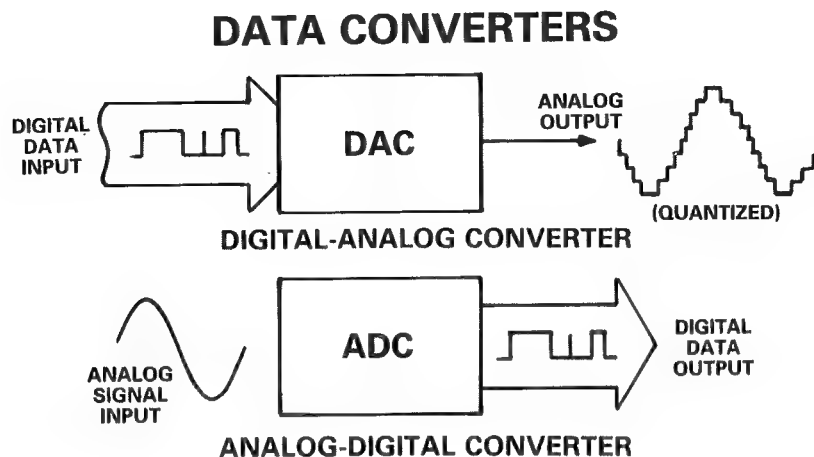
# **BASIC PRINCIPLES OF DATA CONVERTERS**



## BASIC PRINCIPLES OF DATA CONVERTERS

A Digital-to-Analog Converter, or DAC as it is generally abbreviated, is a device which multiplies a digital input and reference and outputs an analog quantity. Its converse is the Analog-to-Digital Converter, or ADC, which has an analog signal as its input and a digital representation of that input as its output.

Such definitions are rather imprecise—so let us consider each part of each definition in detail, starting with a DAC. A DAC has a digital input, which is to say that data is presented to it in the form of a numerical quantity, expressed in one of the standard ways in which numbers may be represented electronically. Different DACs will have different logic interfaces (for example TTL, ECL, CMOS, or some more specialized one), different data formats (simple binary, complementary binary, BCD, or some more complex and specialized format), and different input arrangements (data may be applied as a parallel word, a serial word, a number of nibbles to make a complete word, or whatever) but the essential feature from the point of view of definition is that the control input to a DAC is digital.



This section covers the basics of Data Converters, that is to say Analog-to-Digital and Digital-to-Analog Converters (ADCs and DACs). It will cover the basic functions, architectures by which these functions are accomplished, the specifications which apply to data converters, and the means by which they are measured.

### DEFINITIONS

It is helpful to define what ADCs and DACs are in general terms and then to make the definitions more rigorous.

## DAC CONTROL INPUT

May Be Any Logic Type: TTL, ECL, CMOS,  $\pm 4\text{mA}$  etc.  
May Be Any Format: Binary, Complementary Binary, Twos Complement, Ones Complement, BCD, Gray Code, or What Have You?  
May Be Any Structure: Parallel, Serial or Word-Serial.

**BUT IT MUST BE DIGITAL!**  
(There may be an analog reference input as well).

Many DACs have another input, the reference input, which is analog and not digital, but this need not be considered in the basic definition of a DAC although it will be dealt with in some detail later on.

The output of a DAC is analog. Engineers unfamiliar with data converters usually assume that the output of a DAC is a voltage but in fact it may be any analog quantity—the usual outputs are a voltage or a current, or an attenuation.

But although the output is analog it has one special characteristic which is unusual in analog signals—it is quantized. Since the input to a DAC is digital there can be only a finite number of input states—there can therefore be only a finite number of output states.

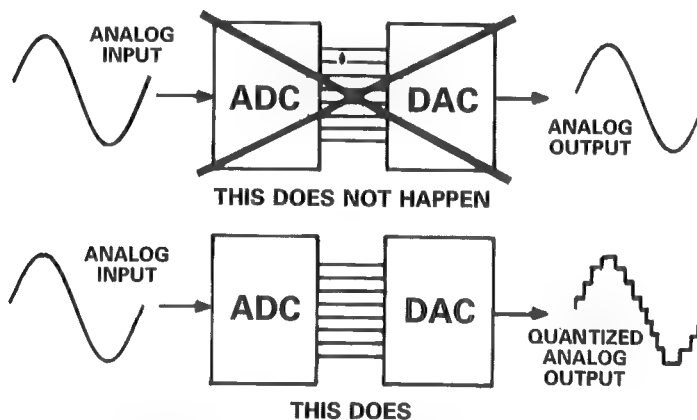
## DAC OUTPUT

May Be Any Analog Variable: Usually Voltage, Current or Resistance (Attenuation)  
But May Be Anything (Light, Water Flow, Phase Shift, Etc.)  
May NOT Have Any Value: Since a DAC Has Digital Input It Has Only a Finite Number of Input States—It has, Therefore, Only a Finite Number of Output States.

**DAC Inputs and Outputs are Quantized**

Many people assume, without thinking, that if an ideal ADC and DAC are connected together and a smooth analog signal is applied to the ADC input it will reappear at the DAC output. This is not the case—the signal that appears at the DAC output is an approximation made up of discrete steps. The size of these steps depends on the resolution and conversion rate of the system. The difference between the original input and this quantized output is sometimes expressed in the form of noise on the input signal, known as “Quantization Noise”. In an N-bit system the quantization noise has a value of  $-6N$  dB with respect to full scale.

## QUANTIZATION NOISE



**FOR AN N-BIT CONVERTER QUANTIZATION NOISE IS  $-6N$  dB ON FULL SCALE**

This mistake lies behind many problems in the design of systems involving data conversion and it is very important that engineers who use DACs and ADCs are constantly aware which signals are quantized and which are not.

We can thus define a Digital-to-Analog Converter as a device which converts a digital input to an output which is an analog parameter and we must note that the output, like the input, is quantized.

## DIGITAL-TO-ANALOG CONVERTER FUNCTION

**A Digital-to-Analog Converter (DAC) Converts Digital Code to an Analog Parameter.**

**Any Parameter may be a DAC Output but Common Ones Are:**

- **Voltage**
- **Current**
- **Resistance (Attenuation)**

**The Analog Output is Quantized**

It is not necessary to spend so much time in considering the definition of an Analog-to-Digital Converter (ADC) since most of the considerations are similar. Most ADCs take an appreciable time to perform a conversion and so the digital interfacing is usually more complex. This is because, in addition to the data output, there may be a number of other digital ports such as “start conversion” and address inputs and “busy” (i.e., conversion in progress) outputs. Such complexity does not affect the definition of function.

The function of an ADC is to output, in digital form, an approximation to the value of its analog input. The output is only an approximation since the analog input may have any value within the defined input range and yet the digital output may only take one of a discrete number of values. There is therefore a difference between the actual output and the input of up to half an LSB which is known as the quantization uncertainty

## ANALOG-TO-DIGITAL CONVERTER FUNCTION

**An Analog-to-Digital Converter (ADC) produces a digital output corresponding to the value of signal applied to its analog input.**

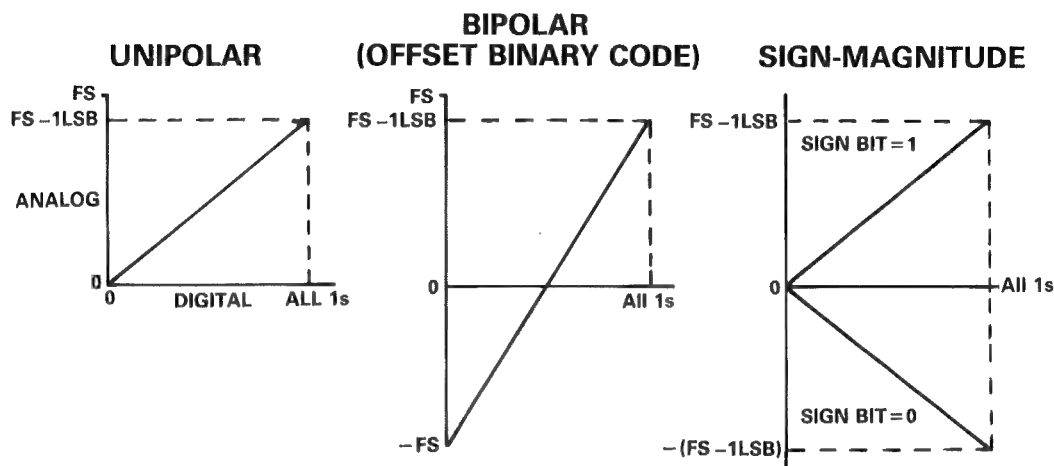
**Since the output is digital it can only take one of a finite number of discrete values and therefore may not exactly correspond to the value of the analog input. The difference is known as the QUANTIZATION UNCERTAINTY.**

In addition to the basic ADC or DAC which we have defined real ADCs and DACs frequently contain many extra analog and digital functions. Since these are not essential to the ADC or DAC function there is no real point in discussing them at this stage in the seminar.

ADCs and DACs may be unipolar or bipolar. A unipolar device has an output with constant polarity while a bipolar device has an output which may be of either polarity. There are two types of bipolar device, the standard “bipolar” ADC or DAC and the “signed”. In the standard “bipolar” a digital zero signal (all 0’s) corresponds to analog full-scale negative, an all 1’s to full scale (minus 1 LSB) positive, and (MSB = 1 and all 0’s) to zero. In the “signed” ADC or DAC the analog signal goes from zero to full scale (minus 1 LSB) as the digital goes from all 0’s to all 1’s and an extra bit corresponds to polarity. It is obvious that all three have the same basic structure—the unipolar is the simplest case, the standard bipolar is a unipolar with a negative offset of 1 MSB, and a signed one is a unipolar one plus a sign bit.



# DATA CONVERTER TYPES



We are assuming here that the code involved is binary—converters are sometimes built using Binary-Coded Decimal (BCD) Code or Gray Code but the majority are binary. (BCD converters are useful where digital displays are involved and Gray Code converters are invaluable where their property of changing only one bit at a time prevents errors during transitions from one code to the next). But there are several different binary codes which may be used with bipolar converters.

## COMMONLY USED BIPOLAR CODES

Number	Decimal Fraction		Sign + Magnitude	Twos Complement	Offset Binary	Ones Complement
	Positive Reference	Negative Reference				
+7	+7/8	-7/8	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	+6/8	-6/8	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	+5/8	-5/8	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	+4/8	-4/8	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	+3/8	-3/8	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	+2/8	-2/8	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	+1/8	-1/8	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
0	0+	0-	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
0	0-	0+	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
-1	-1/8	+1/8	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
-2	-2/8	+2/8	1 0 1 0	1 1 1 0	0 1 1 0	1 1 1 0
-3	-3/8	+3/8	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
-4	-4/8	+4/8	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
-5	-5/8	+5/8	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
-6	-6/8	+6/8	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
-7	-7/8	+7/8	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
-8	-8/8	+8/8		1 0 0 0	0 0 0 0	

The simplest code, offset binary, simply increases from all 0's to all 1's as the analog quantity goes from full scale negative to 1 LSB below full scale positive. Complementary binary is exactly the same code but with negative logic (0's become 1's and 1's become 0's).

Two's complement is the same as offset binary, except that the MSB is inverted (i.e., it is 1 below zero and 0 from zero on up), and one's complement is a bipolar code formed by inverting all the bits of unipolar binary code for the corresponding negative values—it has the same problem as the signed (sign + magnitude) converter in that there are two codes for zero.

## STATIC SPECIFICATIONS

Data converter specifications are frequently confusing but are essentially simple—the confusion most often arises from inconsistent use of units. The error in a converter may be specified in least significant bits (LSB), millivolts (or microamps in a current operated device), percentage of full scale, or parts per million (ppm) of full scale. Quantization noise is expressed in decibels (dB) below full scale. Different manufacturers, or even one manufacturer on different occasions, will express the same parameter in any of these units and it is essential that any user of data converters be familiar with the conversion. The table summarizes it very simply and should, if possible, be memorized—if the whole table is too long the 10-bit row is easily remembered (10V/10 bits/1 LSB  $\approx$  10mV  $\approx$  1/10 percent) and the others may easily be calculated from it by multiplying or dividing by powers of 2.

### DATA CONVERTER ERROR TERMINOLOGY (10 VOLT FULL SCALE)

RESOLUTION (BITS)	mV	% FS	ppm FS	dB FS
8	39.1	0.391	3906	- 48
10	9.77	0.098	977	- 60
12	2.44	0.024	244	- 72
14	0.61	0.006	61	- 84
16	0.153	0.0015	15	- 96
18	0.038	0.00038	3.8	- 108
20	0.0095	0.00010	1.0	- 120

A SIMPLE MNEMONIC IS TO REMEMBER THAT AT 10V FS AND 10-BITS

1 LSB  $\approx$  10mV  $\approx$  1/10 % FS ( $\approx$  1000ppm  $\approx$  -60dB).

ONE CAN THEN WORK IN POWERS OF 2 TO CALCULATE THE OTHERS.

### D/A CONVERTER ERRORS FOUR BASIC CONVERTER ERRORS (STATIC, 25°C)

1. Offset  
The error which adds to all codes equally. (User trimmable)
- 1a. Zero  
The error when the digital input code calls for zero output.
2. Gain (Scale Factor)  
An error in the slope of the transfer characteristic. It affects all codes by the same percentage. (User trimmable)
3. Nonlinearity (Integral Nonlinearity [INL] or Relative Accuracy)  
Integral nonlinearity is a measure of the deviation of a converter's transfer characteristic from a straight line. (Not user trimmable)
4. Differential Nonlinearity [DNL]  
The measure of the difference between the ideal (1LSB) and the actual change in analog output for 1LSB increase in digital code. (Not user trimmable)

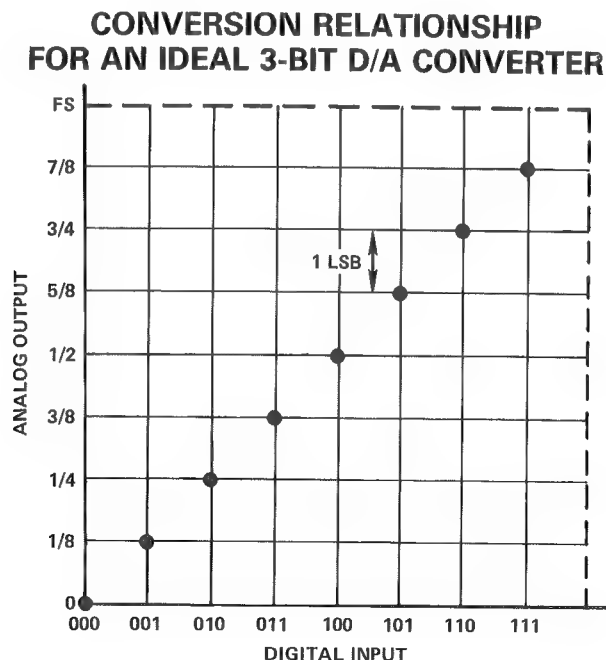
There are four basic dc specifications for data converters: gain, offset, linearity and differential linearity. Of these, gain, offset and differential linearity may vary sufficiently with variation of temperature that their temperature coefficients must also be specified. The linearity of a converter does, or course, vary with temperature but rarely enough for it to be necessary to specify its temperature coefficient.

## TEMPERATURE COEFFICIENTS

1. Offset TC  
A shift due to temperature which affects all readings equally and is expressed as  $\mu\text{V}/^\circ\text{C}$  or ppm FS/ $^\circ\text{C}$ .
- 1a. Zero TC  
Zero shift due to temperature. In a bipolar DAC the zero TC has contributions from both the offset and gain TCs.
2. Gain TC  
Change of the slope of the transfer characteristic with change of temperature. It is expressed as ppm of reading/ $^\circ\text{C}$ . (Reference may or may not be included in this specification)
3. Differential Nonlinearity TC  
Shows the relative change in bit-weights with temperature and is a measure of when a converter can be expected to go nonmonotonic. It is expressed a ppm FS/ $^\circ\text{C}$ .

All the static specifications (and their temperature coefficients) may be defined by considering the graph of the transfer characteristics of the converter. Because the definitions that follow have been written to be equally true for both ADCs and DACs they are slightly more complex and pedantic than the definitions for one or the other but this generality emphasises that essential similarity of converter specifications. We should, however, consider the transfer characteristics of DACs and ADCs separately before considering their static specifications so that the differences as well as the similarities are quite clear.

The transfer characteristic of an ideal unipolar 3-bit DAC is shown in the diagram. It consists of eight points which lie on a straight line. All 0's code gives zero output and all 1's gives 1 LSB below full scale.

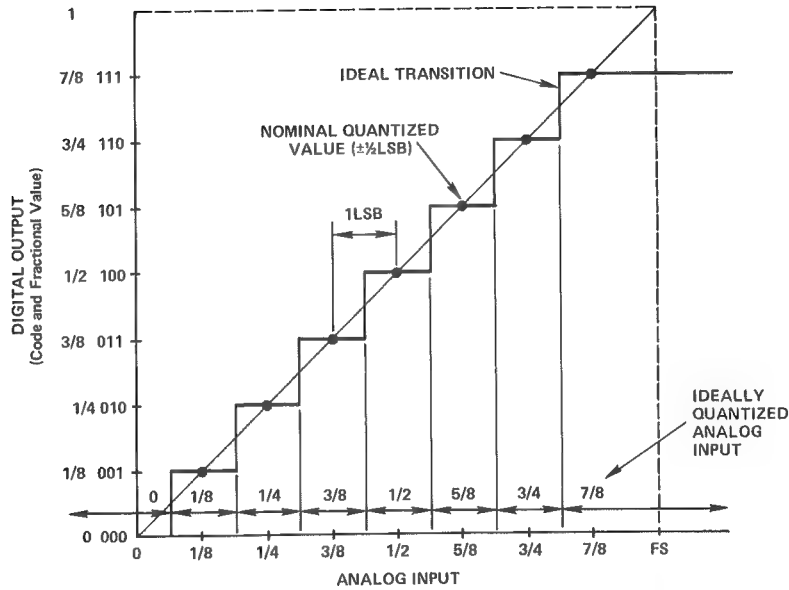


The output for all 1's is 1 LSB below full scale and not full scale because a DAC can be considered as a digitally-controlled potentiometer which produces an analog output which is a normalized fraction of its reference input—this reference is “full scale” and to produce full-scale output from an N-bit DAC would require a digital input of 1 in the (N + 1)th bit and then all 0's. Since a N-bit DAC does not have an (N + 1)th bit the largest possible output is when the input is all 1's and the output is then 1 LSB below the reference or “full scale”.

As we keep emphasizing, a DAC has both its inputs and its outputs quantized and it is misleading to think of its characteristic as a line—it is a series of points. Nevertheless it can be quite useful to consider the line through these points when discussing the definitions of DAC specifications.

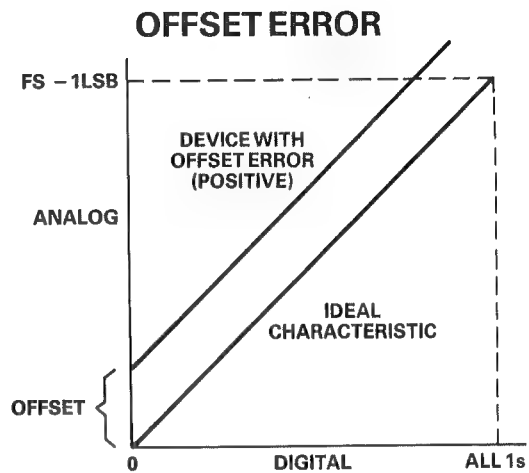
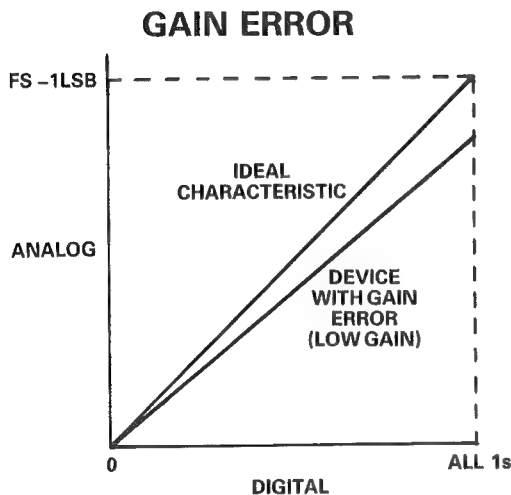
The transfer characteristic of an ideal 3-bit ADC is also shown. In this case the analog input may have any value within its range but the digital output is still quantized. Out of range inputs normally produce all 0's or all 1's outputs, depending on whether they are underrange or overrange respectively, but some types of ADC do not behave in such a convenient way and these types may have output(s) indicating out of range inputs. If the analog input is increased the first change in an ideal ADC's output occurs for an input of 0.5 LSB and subsequent changes occur 1 LSB apart until the last takes place 1.5 LSB below full scale. The resulting diagram is a series of steps, 1 LSB wide, and the line which we consider when discussing specifications is the line through the midpoints of these steps.

## CONVERSION RELATIONSHIP FOR AN IDEAL A/D CONVERTER



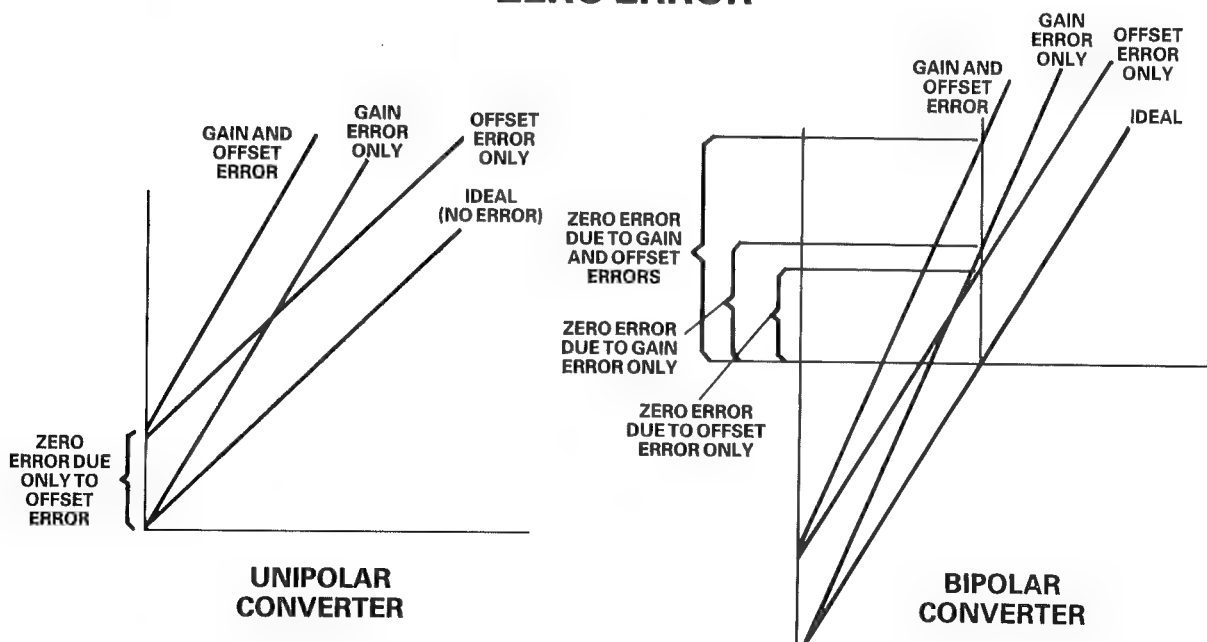
The first specification to consider is the gain. This is defined as the analog scale factor governing the relationship between signal amplitude at the analog and digital ports (when we define digital amplitude we refer, of course, to the amplitude represented by the digital code, not to logic levels). More simply the gain is the gradient of the transfer characteristic. Ideally a change of  $K$  LSB in analog signal should correspond to a change of  $K$  LSB of digital code—if the gradient is steeper or shallower than this there is said to be a gain error. Normally the gain error is measured by noting the analog change for a digital change of all 0's to all 1's—it should be  $(2^n - 1)$  LSB. Gain error applies (multiplicatively) to all codes equally and may therefore be adjusted by the converter user who can usually increase or decrease the gain by altering resistance somewhere in the converter.

The next specification that we shall consider, offset, also applies to all codes equally. The offset error adds to all codes and, again, may generally be user trimmed by adding an equal and opposite error so that the two cancel—the way that this is done depends on the converter architecture.



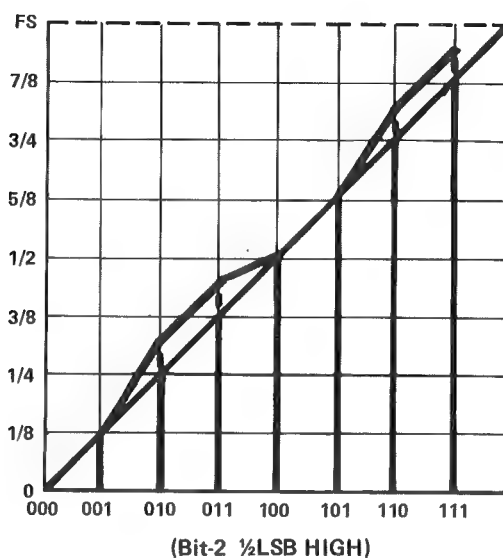
There is frequently confusion (even among data sheet writers) about the difference between offset and zero errors. The zero error is defined as the error in analog value when the digital code calls for analog zero. In unipolar devices the offset error and the zero error are identical but in bipolar devices the zero error contains contributions from both offset and gain error. For this reason the two terms should not be considered interchangeable.

## ZERO ERROR



Both gain errors and offset errors, applying equally to all codes, may be trimmed by the converter user. The other two dc errors do not and may not. The specifications are linearity and differential linearity and the corresponding errors are known as (integral) nonlinearity and differential nonlinearity (abbreviated to INL and DNL) respectively.

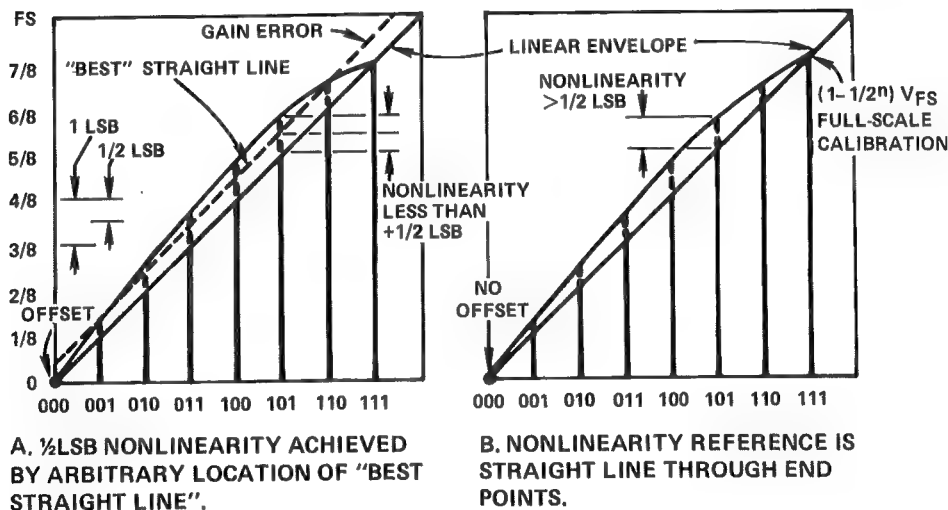
## LINEARITY ERROR



The INL is the deviation of the transfer characteristic of the converter from a straight line. At Analog Devices INL is defined by the "end-point" method—that is to say the INL is defined as the maximum difference between the actual plot of the device response and the straight line drawn from the all 0's point to the all 1's point. It is not unknown for some manufacturers to define INL by the "best straight line" method—here the INL is defined as the maximum difference between the actual plot of the device and the best straight line through its points. Such a definition has the advantage of giving a better "paper" specification but the disadvantage

of being virtually unuseable as a specification for system error analysis (a system is not expected to work to a best straight line—it is expected to work to the ideal straight line, the one through the end points). For most practical purposes the end-point figure is twice as large as the best straight line one (although it is possible to invent circumstances where it is not).

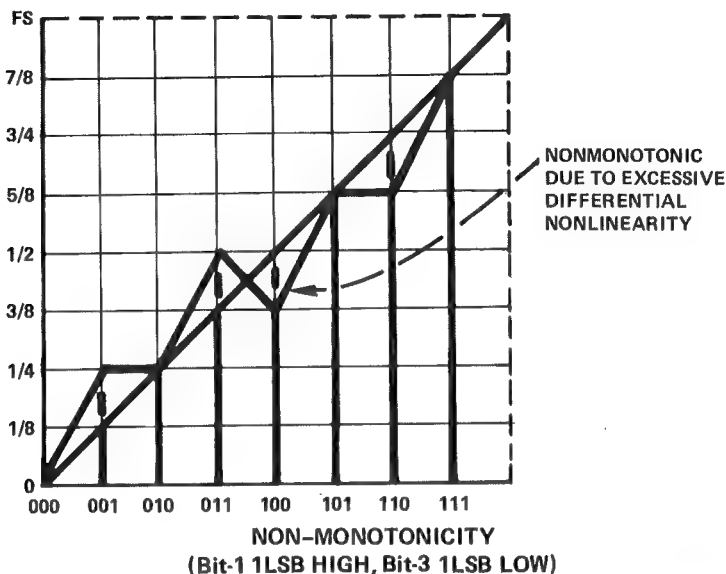
## COMPARISON OF LINEARITY CRITERIA



The differential nonlinearity (DNL) of a converter describes the variation in analog value between pairs of adjacent digital codes. In an ideal converter there is no variation, a digital code change of 1 LSB always corresponds to an analog change of 1 LSB, and the DNL is zero—in practice this rarely occurs. Although the basic principle is the same for both ADCs and DACs the visible effects on the plots of their characteristics differ sufficiently that it is worthwhile looking at the two cases separately.

In an ideal DAC an increase of digital code by 1 LSB causes the output to increase by 1 LSB. If, at any particular code transition, the analog change is not 1 LSB then the device is suffering from DNL at that transition.

## DIFFERENTIAL NONLINEARITY



DNL always refers to the change of analog output with  $\pm 1$  LSB change of code—even if the analog output is correct at a particular code there may be still be DNL in the transition to that code. If the DNL is negative and has a magnitude of over 1 LSB then an increase of digital code will cause a decrease in analog output. A DAC which behaves in this way is said to be nonmonotonic. A mathematical function is said to be monotonic between certain limits if it has no maxima or minima between those limits. A DAC is said to be monotonic if it has no local maxima or minima in its transfer characteristic—that is to say that the slope of its transfer characteristic has the same sign over its whole range.

Monotonicity is critical for many DAC applications—if a DAC in a servo system of any sort is nonmonotonic the feedback becomes positive rather than negative in the nonmonotonic region and the system may oscillate or latch. For this reason most DAC specifications contain guarantees of monotonicity to certain levels or resolution. However, if the DNL is guaranteed to be less than 1 LSB then the DAC will be monotonic, even if this is not explicitly guaranteed.

## MONOTONICITY

**Monotonicity requires that a converter NEVER give decreasing analog output for increasing digital code. Nonmonotonicity is the result of excess differential nonlinearity ( $>1\text{LSB}$ ).**

**Monotonicity is essential for many control applications.**

**A converter which has DNL specified  $\leq 0.5\text{LSB}$  is better characterized than one which is merely “monotonic” – but most manufacturers would specify the monotonicity as well, even though the specification is redundant.**

Sometimes a data sheet will guarantee monotonicity at a particular temperature only. It is often possible to predict whether the device will be monotonic at other temperatures. In the example given two DACs are compared, both with initial accuracy of 60ppm but one having a DNL TC of 1ppm/°C and the other having 2ppm/°C. At +125°C the first has a total error of  $60 + 100 \times 1 = 160\text{ppm}$  which is less than 240ppm so the device is monotonic to 12 bits, the second has a possible total error of  $60 + 100 \times 2 = 260\text{ppm}$  which is more than 240ppm so this device MAY not be 12-bit monotonic (if it were to be guaranteed monotonic at 125 degrees the manufacturer would be guaranteeing that at least some of the errors would cancel—this might be a reasonable guarantee). The same computation and considerations may be applied to an ADC to predict missing codes (see below).

## MONOTONICITY

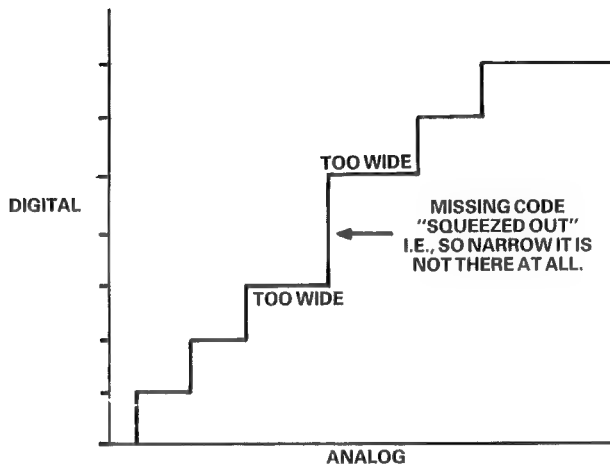
- Factors Contributing:**
1. Initial Accuracy
  2. TC of DNL
  3. Temperature Change

**Examples (12-bit DAC – 1LSB = 244ppm FS):**

<b>Initial Accuracy:</b>	<b>0.25LSB (60ppm)</b>	<b>0.25LSB (60ppm)</b>
<b>DNL TC:</b>	<b>1ppm/°C</b>	<b>2ppm/°C</b>
<b>Temperature Range</b>	<b>–55°C to +125°C</b>	<b>–55°C to +125°C</b>
<b>Max Possible Temperature Change:</b>	<b>+100°C</b>	<b>+100°C</b>
<b>Max Possible DNL Change:</b>	<b>100ppm</b>	<b>200ppm</b>
<b>New Max Possible Error:</b>	<b><math>60 + 100 = 160</math></b>	<b><math>60 + 200 = 260</math></b>
<b>Monotonic (Error &lt; 1LSB)?</b>	<b>YES</b>	<b>NO</b>

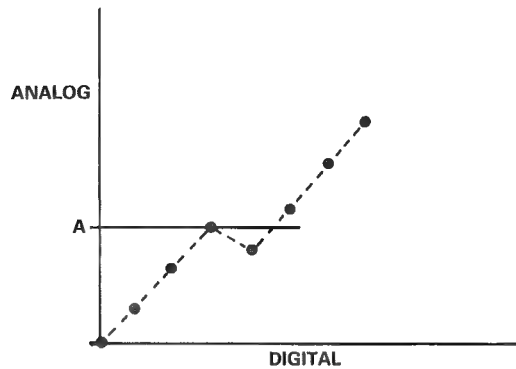
In an ideal ADC each code is exactly 1 LSB wide. The effect of DNL on an ADC is to make particular codes wider or narrower than this—as in the case of a DAC DNL is generally specified in terms of LSBs. If the DNL of an ADC is less than  $-1\text{LSB}$  for any reason the code width will become negative, that particular code will not occur, and the converter will suffer from a missing code. Missing code(s) is the ADC equivalent of nonmonotonicity and is as serious in many applications.

### ADC WITH DNL



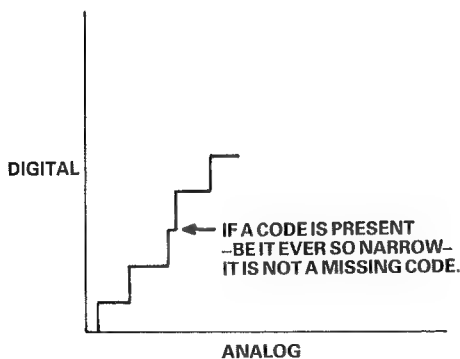
The normal cause of missing codes in an ADC containing a DAC is that the DAC is nonmonotonic. ADCs using DACs search through various DAC codes until they find one with an analog output which matches the analog input to the ADC (the exact search algorithm used depends on the type of ADC). If the DAC is nonmonotonic the algorithm may fail and certain codes will not occur. Consider the 3-bit DAC in the diagram—if it is used as a component in an ADC any input large enough to give an output of 3 LSB is also large enough to give an output of 4 LSB (since the DAC output for 3 is greater than the DAC output for 4 and the search algorithm will look at 4 before it looks at 3). Thus the ADC will never give an output of 3—so 3 is a missing code.

### NONMONOTONIC DAC MAKES AN ADC WITH MISSING CODES



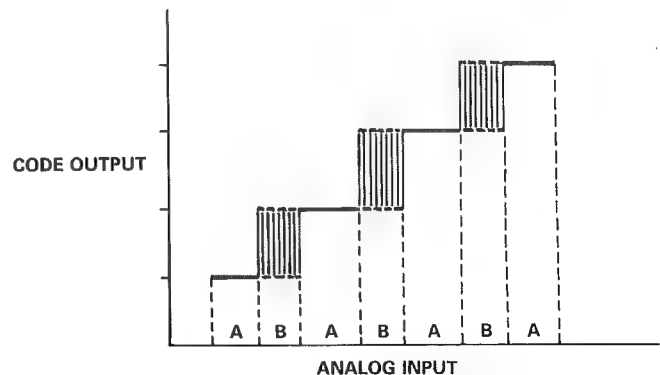
There is some dispute over the exact definition of “missing code” in real ADC specifications. In an ideal, noise-free, ADC if the DNL is never less than  $-1$  LSB then every code, be it ever so narrow, will be present. But real ADCs have noise which results in a transfer characteristic which is blurred at code transitions.

### MISSING CODES



SIMPLISTIC DEFINITION OF MISSING CODE

### MISSING CODES

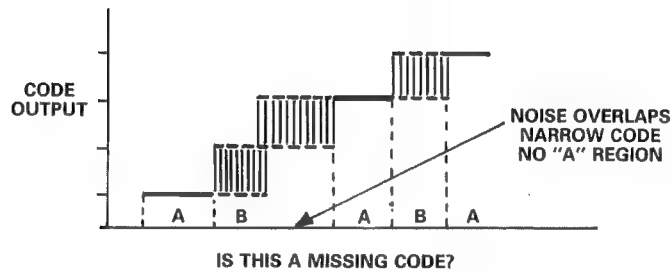


EFFECT OF A NOISY CONVERTER



If the analog input lies in one of the regions A in such a noisy ADC the output will always be the same code, but if it lies in one of the regions B it is evident that converter noise may cause the output to be one of the two adjacent codes. If such a noisy converter also has poor DNL it may be that some of the A regions may be squeezed out.

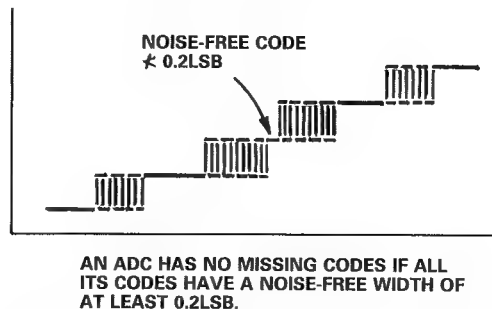
## MISSING CODES



### EFFECT OF NOISE AND DNL COMBINED

In this case the code which is always noisy will sometimes be missing—but not always. Should it be considered a missing code or not? This point has caused considerable discussion among converter manufacturers and users and opinions range from the low-cost manufacturer's "If a code is present sometimes then it can't be missing."—which certainly keeps his yields up to the purist's "If a converter is noisy then I'm not interested anyway."—There is consensus that a code should be noise-free for at least 0.2 LSB of its range in order not to be considered missing—this is a demanding specification at high resolution since it calls for DNL to be  $<0.8\text{LSB}$  in a noise-free converter and for the noise to be less than  $(0.4\text{LSB} - \text{DNL}/2)$  in a noisy one.

## MISSING CODES



### CONSERVATIVE MISSING CODE DEFINITION

In addition to the four major static specifications (and the temperature coefficients of three of them) there are a number of other static specifications which are normally defined on converter data sheets. The majority, such as input impedances, logic levels, power consumption, etc., are self explanatory and need not be considered here, but two, power supply sensitivity and absolute accuracy, should be mentioned further.

In an ideal converter, the performance is unaffected by variations in the power supply (in fact the diagram of the ideal converter does not even show a power supply—the ideal converter, like the perfect black body, the reversible heat engine, and the "little old lady who only used it to go to church on Sundays", is a useful theoretical concept which does not exist in reality). In fact many (but by no means all) converters will only work within quite narrow ranges of power supply and even within these limits variations in supply may affect gain, offset and linearity. The greatest effect is generally upon gain—the result of imperfections in the reference and buffer—and such converters normally have power supply sensitivity (variation of gain vs. variation of supply voltage) as one of their specifications.

The absolute accuracy of a converter is the difference between the actual and expected output for any given input. It is the sum of the gain, offset and linearity errors at that input, and the figure may be calculated for a particular input (remembering that gain errors are proportional to input and, if end-point linearity is considered, linearity errors are greatest away from the end-points) or for a worst case over the whole transfer characteristic. As we mentioned earlier, ADCs, but not DACs, have another error, the quantization uncertainty, which is

intrinsic to all ADCs and adds 0.5 LSB uncertainty even to a perfect one. Absolute accuracy and its variation with temperature are not often specified on a data sheet but may be calculated by the user, from the static specifications which are given, for the particular circumstances under which the converter is to be used.

Such "error budget" calculations can be frightening—each error, in itself, is small but the total, over temperature, frequently causes system specifications to be rethought or much more accurate converters to be specified.

## **DYNAMIC SPECIFICATIONS**

In addition to static specifications, converters have noise specifications and speed related dynamic specifications. Noise is defined in the usual way and relates to the analog input of ADCs and the analog output of DACs.

## **CONVERTER NOISE**

**In addition to noise feedthrough from the digital to the analog parts of converters the analog sections themselves are affected by noise.**

**This occurs as voltage and current noise—with similar spectral characteristics to noise in other analog circuitry—at the input of ADCs and the output of DACs.**

The speed related dynamic specifications differ greatly between ADCs and DACs. A detailed study of the dynamic performance of high speed converters is contained in a seminar prepared by the Computer Labs division of Analog Devices and will not be given here. This seminar will merely consider the speed related specifications of normal low-speed converters.

The speed specifications of ADCs are of two type—analog and digital. The digital specifications relate to the switching speeds and propagation delays in the output logic circuitry and will be discussed in the "Microprocessor Interface" section of this seminar. The analog specifications are the conversion time and the maximum input signal bandwidth.

## **ANALOG-DIGITAL CONVERTERS MAJOR DYNAMIC SPECIFICATION IS CONVERSION TIME**

**IT MAY BE BETWEEN NANoseconds AND SECONDS  
DEPENDING ON THE TYPE OF ADC.**

Considered as a black box an ADC has an analog input and a digital output. It is rarely possible, however, to assume that the digital output reflects the state of the analog input a fixed period before—most conversion techniques are more complex than that. We shall discuss different conversion techniques and their timings in detail in the section on "ADC Architecture"—at this point it is sufficient to say that most ADCs require a digital "start conversion" command and the digital output data becomes available some time later. This delay is called the "conversion time". Different ADCs may have conversion times which range from nanoseconds to seconds.

Some ADCs latch their analog input during conversion. Such an analog latch is called a "Sample-and-Hold Amplifier" or "Track-and-Hold Amplifier" variously abbreviated to SHA, SAH, or THC—it is intrinsic to some ADC architectures and is sometimes added to other types of ADC to improve their performance. The most important SHA specification is usually its acquisition time. SHAs are discussed in detail in the "Data Acquisition Subsystems" section of this seminar.

If the analog input is not latched it must not change by more than 0.5 LSB during a conversion unless the converter is of a type (such as a VFC or an integrating ADC) which integrates and averages the input signal during the conversion period. This severely limits the input bandwidth of an ADC (the bandwidth of an integrating ADC is limited by its own integration). Consider an  $n$ -bit ADC which is digitizing a sine wave whose peak-peak amplitude is the full-scale range of the ADC. During the conversion period the input may not change by more than 0.5 LSB. At its maximum rate of change a signal of  $F$  Hz changes 0.5 LSB in  $1/(2^{n+1} \times \pi \times F)$  seconds. This gives us an equation relating  $n$ ,  $F(\max)$  (the maximum input frequency which may be digitized without a SHA), and  $T_c$  (the conversion time).

## ADC WITHOUT A SHA

$$F(\text{max}) = \frac{1}{2^{(n+1)} \cdot \pi \cdot T_C} \text{ Hz}$$

Solving for  $n=16$  and  $T_C = \mu\text{s}$  gives a maximum input frequency to a  $10\mu\text{s}$  16-bit ADC ( $10\mu\text{s}$  is very fast for a 16-bit ADC) of 0.24Hz!

For an AD670 (8-bit  $10\mu\text{s}$ ) the figure is 124Hz and for an AD7572 (12-bit  $5\mu\text{s}$ ) it is 8Hz.

This equation leads us to the startling conclusion that even such a fast ADC as the AD7572  $T_C = 5\mu\text{s}$ ) has an input bandwidth, when used without a SHA, of less than 8Hz.

The two important DAC specifications are settling time and glitch—maximum update rate is also important but unless the DAC logic is unusually slow it is normally limited by the settling time and need not be considered separately. Multiplying DACs should also specify reference bandwidth, both  $-3\text{dB}$  and 1 LSB feedthrough.

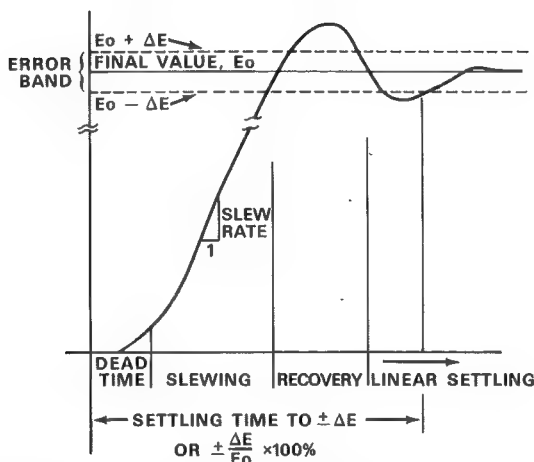
Settling time specifications are very confusing. Manufacturers seem to delight in using different standards for different devices so that comparison is difficult, if not impossible. The reason is simple—specifications are chosen to show the device in the best possible light. If we are to make sense of a settling time specification we should understand what is meant by settling time.

The settling time of a DAC is the time taken for the output to move to, and remain within, a specified error band after the digital input has changed. It is important to note the “and remain” part of this definition—in many DACs the output will ring in and out of the error band for a few cycles before finally settling within it—the specification relates to the final entry to the error band, not the first one. The settling time may be subdivided into dead time, slewing, recovery, and linear settling time. The dead time, known as “propagation delay”, is the time between the digital change and the analog output starting to move, the slewing time is the time during which the analog output is changing as fast as it can (i.e., at its maximum slew rate), the recovery time is the time during which the converter recovers from its fast slewing phase, and the linear settling time is the time during which it settles to its final state.

In general we may consider only the total settling time and not bother with subdividing it, but if the slewing time occupies the majority of the total settling time then the settling time will be proportional to the step size and different analyses may be necessary for different step sizes.

If the device is critically damped there is no recovery time and the output passes directly from slewing to linear settling. Some DACs are hard to damp in this way since the impedance of their internal current output DAC varies with code and the current-voltage converter cannot be optimized for a fixed source impedance.

## SETTLING TIME MEASUREMENT

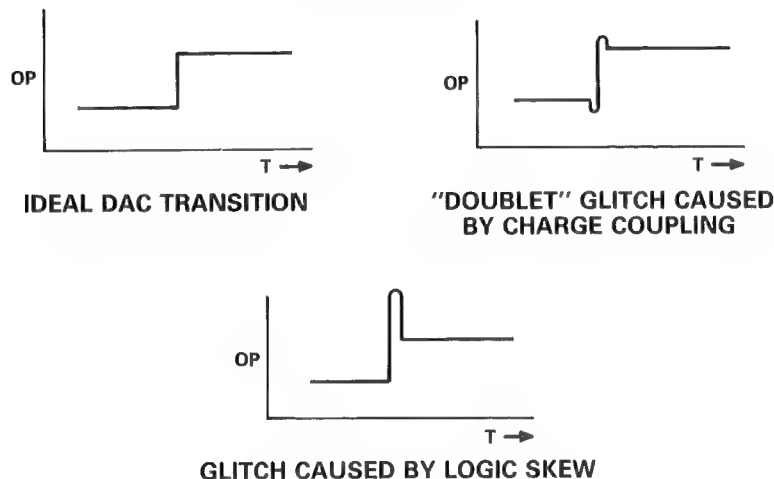


THE SETTLING TIME OF A DAC IS THE TIME BETWEEN THE LOGIC EDGE WHICH INITIATES A CODE CHANGE AND THE ANALOG OUTPUT MOVING, AND REMAINING, WITHIN THE SPECIFIED OUTPUT ERROR BAND.

When considering settling time specifications it is also important to realize that in some types of DAC different transitions have different rates (for example positive going will be faster than negative going if pull-up is with a transistor and pull-down with a resistor), and the settling in a voltage output DAC will be slower than in a current output DAC of the same general type since capacitance charging takes time.

If we change the digital input to a DAC we expect the analog output to change from one value to another. In practice the output during switching may go well outside the region between the start and finish values—this effect is called a “glitch” and has two separate causes.

## GLITCHES



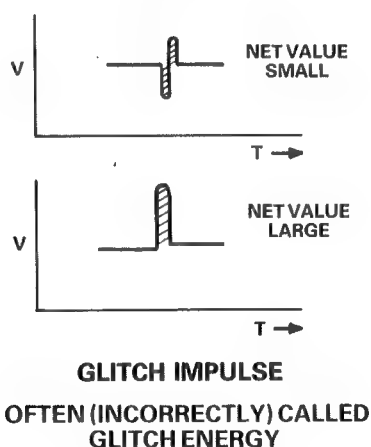
If stray capacity couples the digital circuitry to the analog circuitry (as is inevitable to some extent) then when the digital circuitry switches a transient will appear in the analog circuitry. Such capacity will be due both to stray capacity on the DAC chip and to package and circuit-board capacity. In many types of DAC (but not all!) this type of glitch is fairly small (and can be minimized by minimizing stray capacities external to the DAC itself), does not vary much with code, and frequently consists of a “doublet” pulse having equal positive and negative excursions. This type of glitch is thus generally fairly easy to filter from the DAC output.

If positive-going and negative-going transitions in the DAC logic have different speeds then during a code change the faster operation will be complete first. This means that there will be a short period when some of the switches in the DAC have changed and some have not—this causes the DAC output to go to an intermediate state which may be well outside the region between its start and finish. Glitches of this type are frequently much larger than the previous type, are not “doublets”, and vary greatly with code. They are much harder to filter.

Glitches may be removed by filtering the DAC output (at the cost of increased settling time), by placing a SHA in the DAC output which is set to hold during DAC transitions (this is a good method but is limited by glitches in the SHA itself), or by designing the DAC for minimum glitch impulse.

Although the specifications of glitches often speaks of “glitch energy” or “glitch charge” these terms are often misnomers—while it is quite reasonable to evaluate the energy (in picojoules) or the charge (in picocoulombs) associated with a glitch, the figure generally specified by DAC manufacturers is the impulse—the net product of volts and time in the glitch pulse.

## GLITCHES



Glitch is normally specified for the worst case (i.e., the transition having most glitch) and the variation with code may also be specified. Fixed reference DACs have their glitch specified for normal operation but multiplying DACs are often specified with a zero reference input, a "doublet" type of glitch but will give unfairly good results for glitches caused by logic skew. (Multiplying DACs are discussed in more detail later but for the benefit of those unfamiliar with the term it should be understood that all DACs have references—in the general case the reference has a fixed nominal value but a multiplying DAC is designed to use a reference which may be varied widely, so that in essence the output of a multiplying DAC is the product of the digital code and the analog reference input. For this reason the dynamic specifications of a multiplying DAC should include the bandwidth of the reference input for operation within specification.)

## GLITCH

**Glitch is measured under normal operating conditions.**

**In the case of a multiplying DAC the reference may be set to zero to measure "doublet" glitch, and to its maximum value to measure combined "doublet" and skew-related glitch.**

## CONVERTER TESTING

The methods and apparatus used to test converters are influenced by a number of factors relating to converter applications, the nature and speed of tests to be performed, and the skill of the test personnel involved. The relative importance of various converter performance specifications is dependent on each particular application, and the converter user is naturally interested in testing those parameters which significantly influence his system performance. Two typical applications illustrate how the application of the converter influences the importance of various performance parameters.

Differential linearity, fast settling time and a small switching transient (glitch) are generally of concern when DACs are used as CRT vector generators, since display quality depends critically on these parameters. Small errors in absolute calibration or zero are rarely of consequence, since they cause only small shifts of display size and position, which can be easily corrected by the operator.

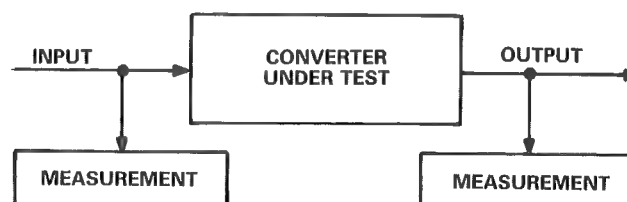
In contrast, a DAC used as a programmable stimulus generator in an automatic test system requires good absolute calibration and zero-stability but does not need fast dynamic response, transient-free switching, or exceptional differential linearity.

The configuration and degree of automation of converter test circuitry is influenced by the purpose of the test (e.g., engineering performance evaluation, incoming inspection, functional checks, etc.), the versatility, measurement speed, data-reduction, and display capability of the test equipment, and the skill required for its operation. Simple test fixtures designed to test a few converter parameters can be made easily and inexpensively but must usually be operated by relatively skilled people, and test data obtained from them must usually be processed before it is of use.

Versatile automatic testers are necessarily complex and costly. An automatic tester generally performs tests quickly, however, and can be operated by less-skilled people. High-resolution converters have large numbers of data points which must be examined to extract performance information. A 12-bit DAC, for example, has  $2^{12}$ , or 4096, possible states. Fortunately, by knowing the type of converter errors or deviations from ideal performance that are commonly encountered, it is possible to devise tests which permit useful data to be gained from the investigation of far fewer than the  $2^n$  states associated with an n-bit converter.

The general principle of testing a converter is to compare its input and output and see whether they agree and, if not, by how much.

## GENERALIZED CONVERTER TEST



**WHILE THE DIGITAL READING IS GENERALLY TRIVIAL  
THE ANALOG MEASUREMENT MAY BE VERY DEMANDING**

To measure the accuracy of a 12-bit converter to  $\pm 1/4$  LSB by such methods a voltmeter with relative accuracy (linearity) to  $\pm 0.001\%$  is required. Such an instrument costs several thousand dollars since increased accuracy costs much more than additional digits. To make such a measurement the user would either need to automate the test sequence or memorize the exact voltage for each of  $2^n$  codes. It is easier to use a precision DAC as a reference and work from there by comparing analog and digital signals.

## USING A REFERENCE DAC

An 8-bit measurement requires a 10-bit DAC.

An 10-bit measurement requires a 12-bit DAC.

An 12-bit measurement requires a 14-bit DAC.

An 14-bit measurement requires a 16-bit DAC.

An 16-bit measurement requires a 18-bit DAC.

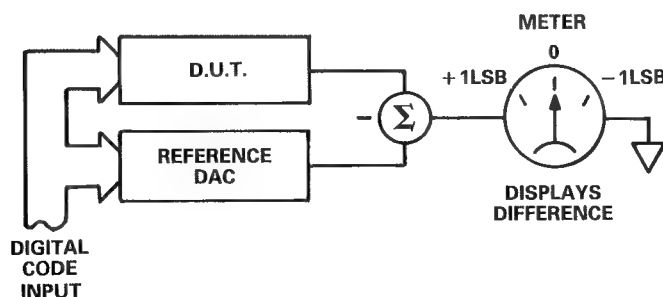
An 18-bit measurement requires a 20-bit DAC.

An 20-bit measurement requires the National Bureau of Standards.

## DAC TEST CIRCUITRY

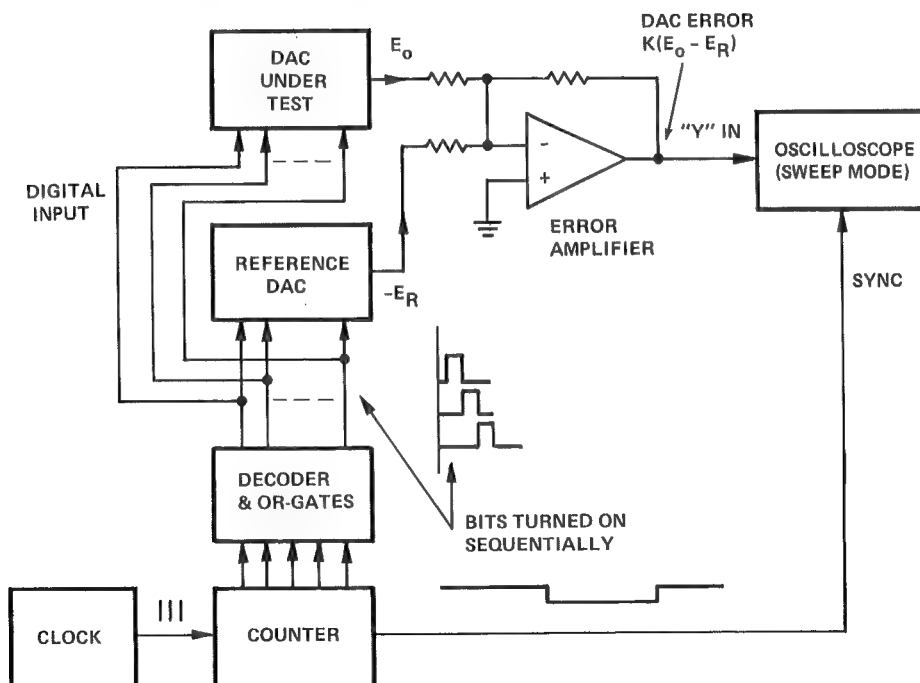
To test a DAC using a reference DAC uses the general principle shown in the diagram—the same code is applied to both DACs and the difference in their outputs, rather than their absolute values, is displayed.

### DAC ERROR TESTING



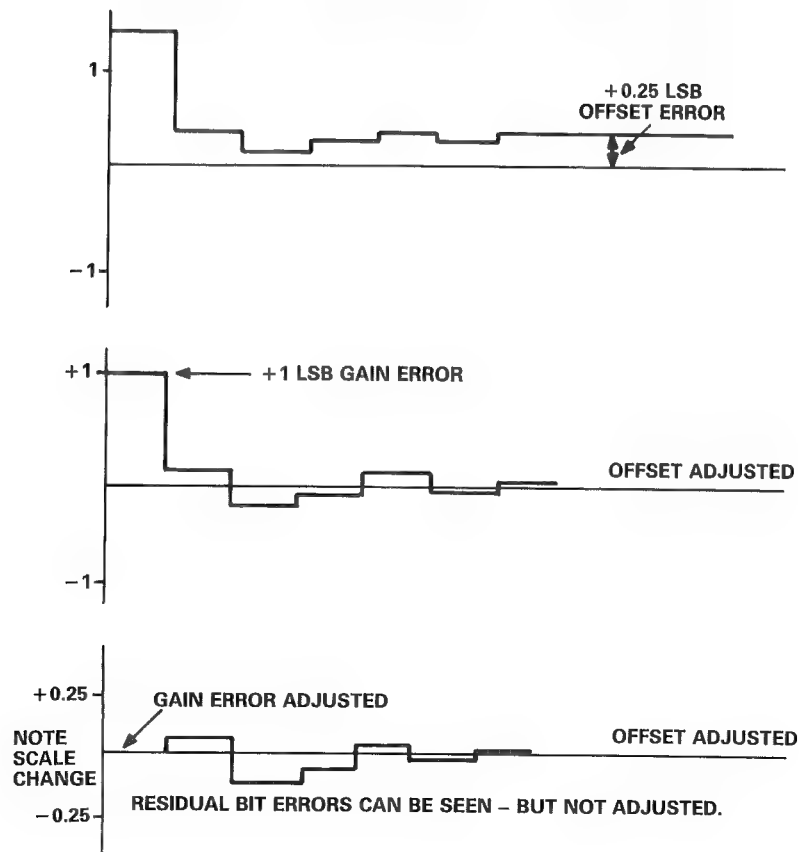
This is a very slow method and it may be sped up considerably if the code entry is automatic and only a few codes are used. In the "bit-scan" mode the same comparison is made between a DUT and a reference DAC but the difference output is applied to the vertical input of an oscilloscope. Only  $n+2$  codes are applied to an  $n$ -bit DAC—these are all 1's, each bit set 1 in turn, starting with the MSB, while the rest are 0, and all 0's. The oscilloscope is in normal sweep mode and is triggered by the leading edge of the all 1's code—its time-base is adjusted so that the sweep displays all  $n+2$  outputs.

### DAC DYNAMIC TEST – BIT SCAN MODE



The oscilloscope displays the error in the DUT at each code in turn. With a code of all 0's it displays the offset error. With a code of all 1's it displays the sum of the gain and offset errors.

### DAC BIT – SCAN TEST – DISPLAYS



As mentioned earlier the gain and offset errors of a DAC may be trimmed by the user and we may use this bit-scan display to do it. Order is important—the offset should be adjusted first (at the all 0's code) until it is zero. The error at the all 1's is now just a gain error and it should also be adjusted to zero—exactly as shown in the diagram.

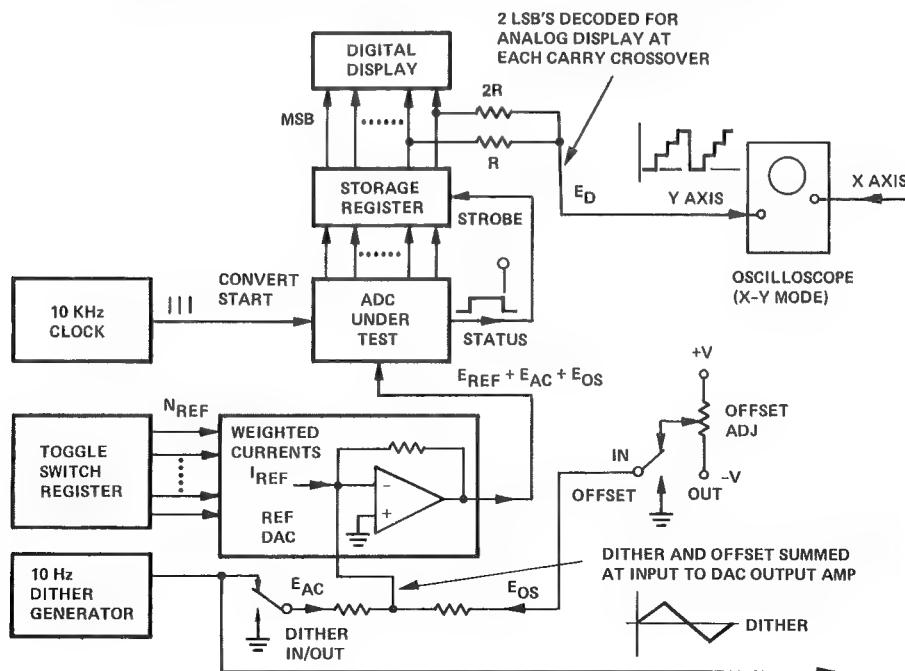
The remaining display shows the individual bit errors. Many DAC architectures define individual bits independently—this test is an excellent way of demonstrating bit errors in such DACs (DAC manufacturers use the same test to perform individual bit trims but these are a manufacturing step and cannot be performed by the user—all that he can do is to see how good or bad his DAC is).

The test may be used with DACs whose bits interact and is a convenient way of trimming offset and gain but it will not be so useful in assessing the linearity of such devices and more complex tests may be necessary to do so.

## ADC TEST CIRCUITRY

An obvious simple ADC test is slowly to increase the analog input and observe the bit transitions as they occur, deriving the offset, gain, and linearity errors from them. It is a very slow and boring test to perform and a faster and equally efficient test is the "dynamic cross-plot" which, like the DAC bit-scan test, allows trimming as well as measurement of gain and offset errors.

### ADC DYNAMIC CROSS-PLOT TEST

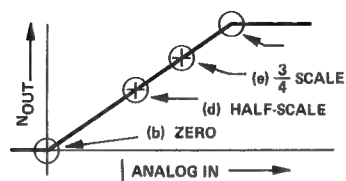


This test uses a reference DAC as well—the test set-up is shown in the diagram. It looks complex but may, in fact, be built in most laboratories in under an hour. A low frequency, low amplitude waveform is summed with the DAC output and applied to the ADC input—the waveform is also applied to the horizontal input of an oscilloscope working in the X-Y mode. This low frequency waveform is known as a "dither" waveform and may be sinusoidal or triangular but not discontinuous (sawtooth or square). Its period should be more than 1000 times the conversion time of the ADC so that input level changes during conversion are insignificant, and its amplitude should be 10-12 LSB. This low dither frequency limits the technique's usefulness in measurements on converters with conversion times much in excess of 1ms but is otherwise unimportant.

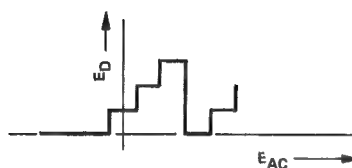
This dither waveform superimposed on the DAC output causes the ADC to perform a series of conversions 5 or 6 LSB above and below the DAC output. The two LSB of the ADC output are applied to a 2-bit DAC (a fancy name for 2 resistors!) via a latch (or directly if conversion is fast and the pauses between conversion are long enough) and thus to the oscilloscope screen. As the dither waveform rises and falls the ADC cycles through 10 to 12 adjacent codes and they appear on the oscilloscope as a series of 4-step staircases. By observing these staircases it is possible to measure, and adjust, the ADC's performance.



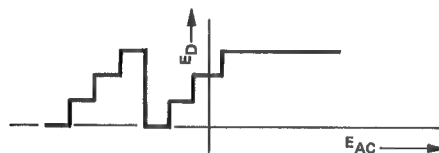
## ADC DYNAMIC CROSS-PLOT WAVEFORMS



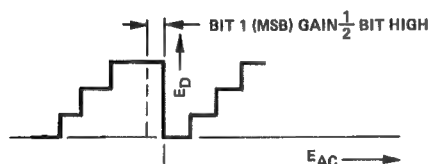
**A. WAVEFORM LOCATION ON TRANSFER CURVE**



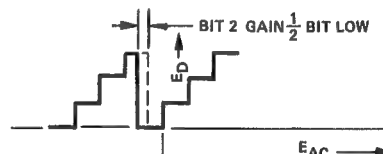
**B. ZERO CALIBRATION**



**C. FULL-SCALE CALIBRATION**



**D. HALF-SCALE CARRY, BIT-1 GAIN HIGH**



**E. 3/4 SCALE CARRY-BIT 2 GAIN LOW**

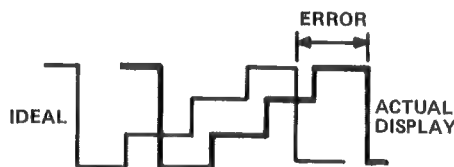
First of all the position of the undeflected oscilloscope beam is noted and the dither waveform turned on. The reference DAC is set up with 1 in the LSB and all 0's and the bottom step of the cross-plot waveform is adjusted to center on the Y-axis, as in B of the diagram, by adjusting the ADC offset. The reference DAC is then set to 0 in the LSB and all 1's, as in C of the diagram, and the ADC gain is adjusted so that the pen ultimate step is centered on the Y-axis.

Offset and gain are trimmed by this arrangement and other ADC measurements may now be made (in fact offset and gain should theoretically be trimmed with the reference DAC at all 0's and all 1's respectively and the codes used to introduce some interaction but they are used for two reasons—the interaction is insignificant, and if all 0's or all 1's were to be used the "step" involved would extend to minus infinity or plus infinity respectively and it would not be possible to "center" it).

Once the ADC under test is trimmed the cross-plot may be used to investigate DNL, INL, and noise. The DAC is set to the major bit transitions and the code widths in the staircase observed. If they are of very different widths the device has poor DNL; if one or more codes are not present the device has missing codes.

If the DAC is set to a particular code and the display shows clearly that, that code is not centered on the Y-axis then the device has an INL error of the amount that the code is displaced. If INL error is suspected of being so large that the "wrong" staircase is on screen then the codes should be increased in steps which are sufficiently small to see the correct staircase "walking away" across the screen.

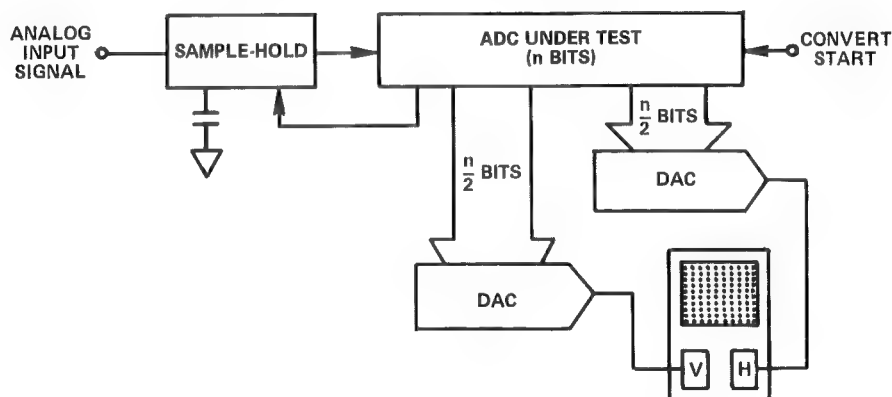
### INTEGRAL NONLINEARITY IN AN ADC CAUSES THE DYNAMIC CROSS-PLOT DISPLAY TO BE DISPLACED FROM ITS IDEAL POSITION



Noise in the ADC manifests itself as fuzzy edges to the cross-steps. It may be measured in LSB or mV.

A simple test for missing codes under the traditional definition uses two  $\frac{n}{2}$ -bit DACs to test an n-bit ADC. The ADC input is slowly increased at a rate of less than 0.1 LSB per conversion (so that at least 10 conversions occur for each LSB), the ADC outputs are fed half to each DAC (which output goes to which input, on which DAC, is unimportant), and the DAC outputs go to the X and Y inputs of a storage oscilloscope in the X-Y mode. Each code is a unique point in a matrix on the oscilloscope screen—it is easy to spot a missing point in a matrix, and if a point is missing a code is missing! (Uniform point brightness indicates good DNL, and wide variation of brightness indicates poor DNL).

### ADC MISSING CODE TEST



This test is very simple to perform and interpret and gives a very quick and efficient screen for ADCs with missing codes.

### DATA CONVERTER ARCHITECTURES

Data converters are relatively complex structures and may contain some or all of the following subsystems:

### SUBSYSTEMS USED TO BUILD DATA CONVERTERS

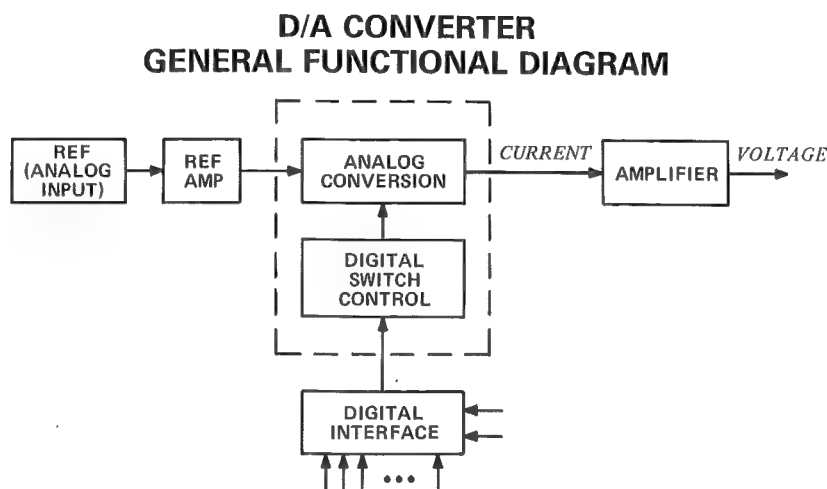
- Amplifiers and Comparators
- Voltage References
- Precision Resistors
- Current Sources
- Logic Circuitry
- Switches

THESE MAY BE MANUFACTURED WITH MANY DIFFERENT TECHNOLOGIES.

These may be made using many different structures and technologies. Many of the technologies used by Analog Devices to manufacture data converters are described in the section of the seminar devoted to process technology but it is not necessary to understand the technology to understand the architectures of different types of data converter—all that is necessary is to realize that few monolithic technologies are equally suitable for the manufacture of all these subsystems. Furthermore in real life, as opposed to theoretical designs, few subsystems are perfect and converter architectures will be chosen to minimize the effects of imperfections in the technologies used.

## DAC ARCHITECTURES

A generalized DAC architecture is shown in the diagram.

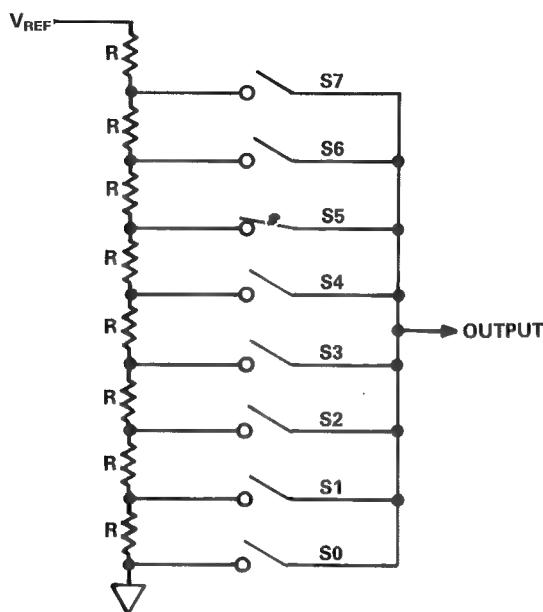


It consists of a core—which is essential to the DAC function—and a number of other subsystems which are convenient but not necessary. The core contains the basic data conversion and digital switch control which normally consists of resistors (or precision current sources) and switches which are generally transistors or MOS devices.

Other desirable subsystems include amplifiers, references, and digital subsystems of varying complexity. Which optional subsystems are included in a DAC depends on the function for which it is designed and the process which is used to manufacture it. This process is determined by the performance required of the core converter and we shall consider the various types of core before we consider their surrounding subsystems.

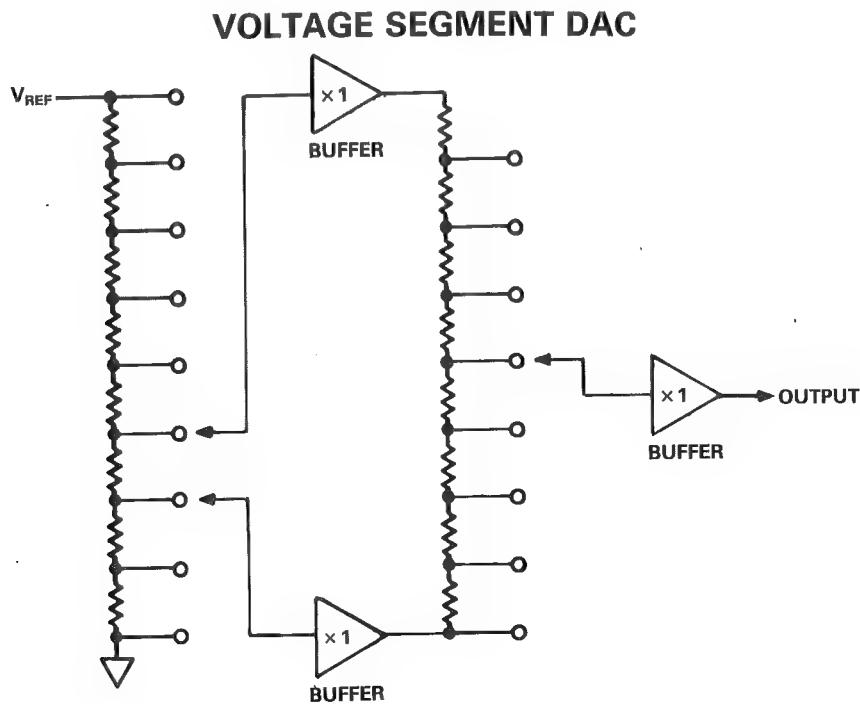
## DAC CORES

The simplest DAC uses a Kelvin Divider—a simple chain of resistors with a switched tap.



Only one switch is closed at any time and the output voltage is the voltage at the point on the divider chain to which the output is switched. Such a DAC is very simple in concept, is monotonic even if the resistors are not well-matched, and (since all the voltages are always present) has potentially quite high speed, but does have certain drawbacks. First of all it has a high, and code variable, output impedance (although this problem can be minimized by the use of a buffer amplifier). Secondly an  $n$ -bit converter requires  $2^n$  resistors which can result in a large structure, thirdly the switches used must operate with either side biased anywhere between ground and  $V_{REF}$ , and finally the logic requires extensive decoding.

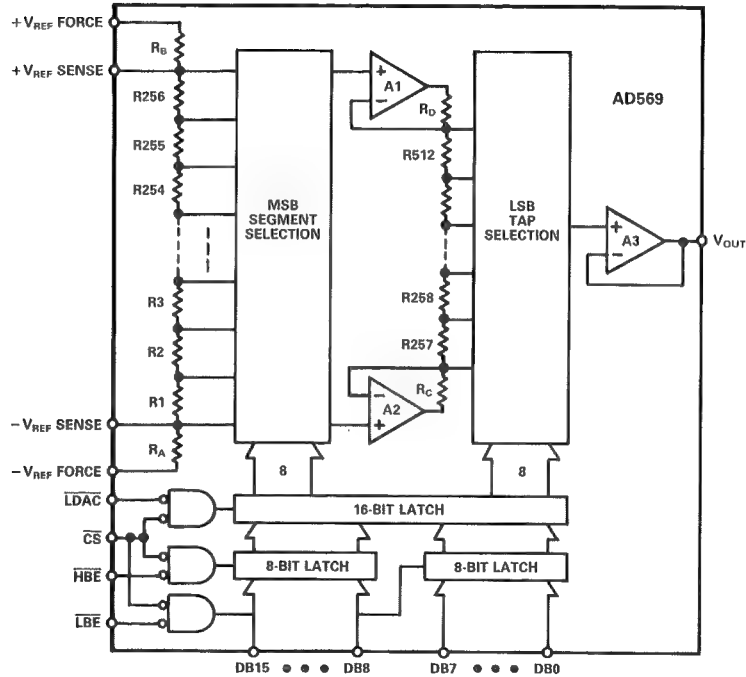
These disadvantages are such that the basic structure is very rarely used in real commercial DACs but extensions of the technique are quite useful since they retain the intrinsic monotonicity of the system while overcoming some of its limitations. The most common extension is the voltage segment DAC where there are two dividers.



The reference voltage is connected across the first divider and the second divider is connected between adjacent taps on the first divider—the particular pair being chosen by the more significant bits of input code. It is evident that if the second divider is connected directly to the first it will load it and reduce the voltage across the particular resistor it is connected to but this difficult can easily be overcome by putting unity gain buffers between the two if the whole DAC is to be monotonic either the buffer offsets must be well under an LSB or the switching scheme must be more complex and one buffer be connected only to odd taps and the other to even taps.

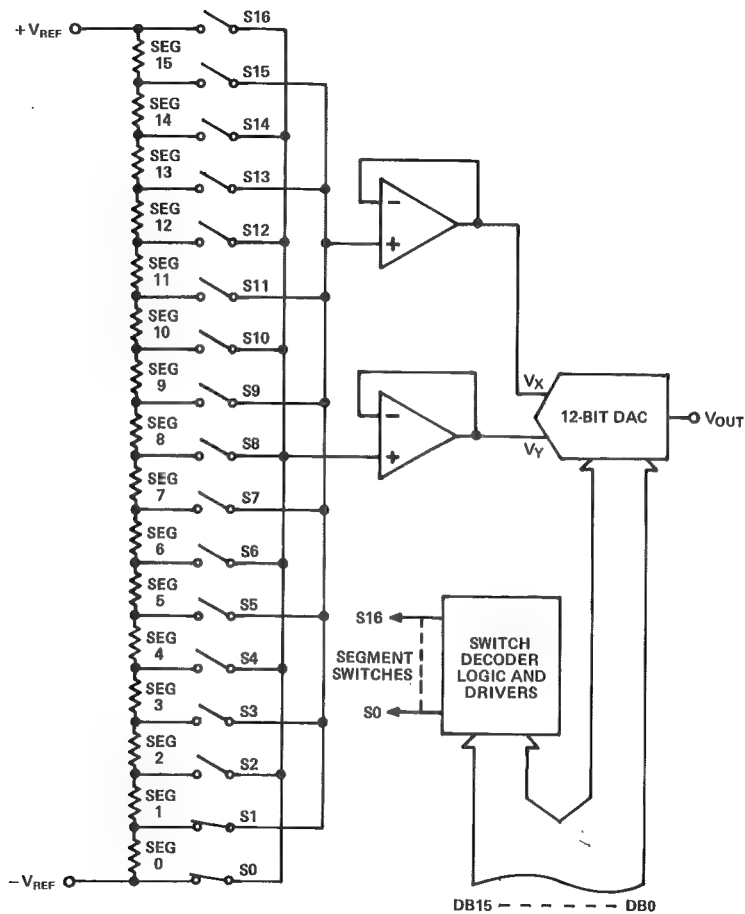
The result of this scheme is that the reference input is divided in turn by the first and second resistor chain and so an  $n$ -bit DAC may be made with two chains of  $2^{(n/2)}$  resistors. Furthermore the DAC is intrinsically monotonic even if the resistors are grossly mismatched (gross resistor mismatches cause gross integral linearity errors and can even cause fairly major differential linearity errors but never of such a sense as to cause non-monotonicity). An example of such a DAC is the AD569 which uses BIMOS technology to make a 16-bit voltage segmented DAC.

## AD569 FUNCTIONAL BLOCK DIAGRAM



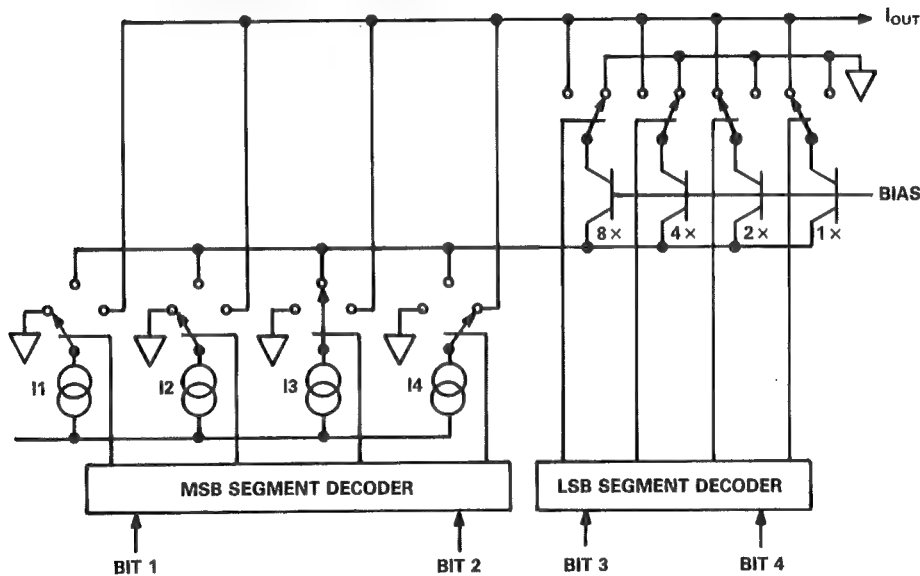
The AD569 uses untrimmed resistors (it is quite expensive to trim over 500 resistors per chip) and has INL of 13-bits while being monotonic to 16-bits—in the type of closed-loop application for which it is intended an INL of 13-bits is more than adequate.

The second half of a segmented DAC need not be another simple divider chain but may be some other type of DAC.



The principle of the segmented DAC may also be applied to current segmentation where instead of a resistor chain dividing a reference voltage a number of switches route currents.

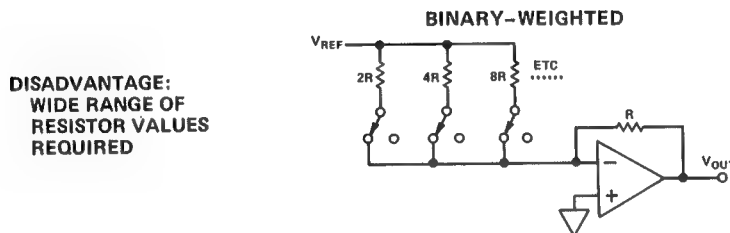
## CURRENT SEGMENT 4-BIT DAC



In the DAC illustrated four switches route equal currents to ground, to the output, or to the output via a second 2-bit DAC. This second DAC divides its input current into four equal parts and routes each to the output or to ground. It is evident that such a system is the current equivalent of the voltage segmented DAC described above and is inherently monotonic: as the input code increases from zero at first  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_4$  all flow to ground, then increasing amounts of  $I_1$  flow to the output while the rest flow to ground, then all  $I_1$  flows to the output and increasing amounts of  $I_2$  with it while the remainder flow to ground, and so on. Since any current connected to the output by increasing code is never disconnected while the code continues to increase the output is nonmonotonic.

Despite the simplicity of simple voltage- or current-divider structures the usual text-book illustration of a DAC does not use them. This is because the simple binary-weighted DAC has a major conceptual advantage—if driven by a simple binary number it does not require any decoding logic—each logic input drives a switch.

## CONTINUOUS BINARY-WEIGHTED NETWORK

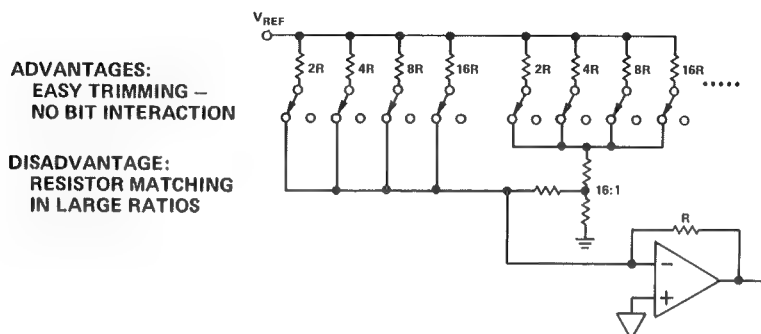


A series of resistors in the ratio  $2R$ ,  $4R$ ,  $8R$ ,  $16R$ , etc., are connected to a reference voltage and switched to a current summing point at ground potential. The switches are controlled respectively by the MSB, next MSB, etc., and it is clear that twice as much current flows in each resistor as in its successor. Thus the total current at the summing point is set by the reference and the binary control inputs to the switches and we have a current output DAC. If a voltage output is needed an I-V converter formed by an operational amplifier and a resistor (of value  $R$ ) is all that is necessary to provide it.

The binary weighted DAC is conceptually very simple and is therefore widely used for teaching purposes but it suffers from a serious drawback in real life: its range of resistors. An  $n$ -bit voltage output DAC of this type requires a resistor range of  $2^n:1$  and in practical integrated circuits it is very difficult to make accurately matched resistors with a range of more than 30:1—giving a maximum resolution of only 5 bits.

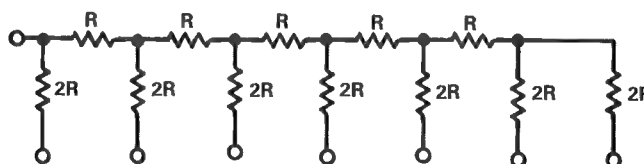
This limitation may be overcome by building two or more such binary weighted 4-bit DACs and attenuating their outputs accordingly. This technique is known as the successively weighted binary quad and has been used in a number of early DACs.

## SUCCESSIVELY-WEIGHTED BINARY QUADS



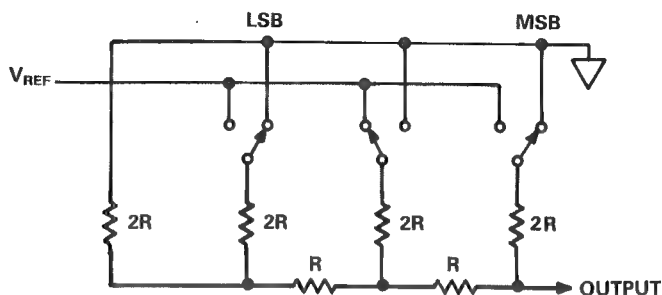
Its disadvantage is still the range of resistance necessary. Although it is quite possible to manufacture precision resistors having a ratio of 16:1 whose resistances match and track over temperature, it is not economical of chip (or thin-film substrate) area. For this reason most binary weighted DACs have been superseded by DACs built with ladder networks.

## A SIX BIT R-2R LADDER NETWORK



A ladder network is an array of resistors, organized as shown in the diagram and having only two different values of resistors— $R$  and  $2R$ . It is simple in concept and if the resistors match to 1 part in  $2^n$  will give  $n$ -bit monotonicity but unlike the voltage dividing DACs described above, where the switches involved had only to switch voltages to high-impedance buffers, the ladder network is a current operated device and the switches used with it must be of sufficiently high performance as not to degrade the DAC performance. It may be used in two different configurations, each having its own particular benefits and disadvantages.

## STANDARD 3-BIT DAC USING R-2R LADDER NETWORK

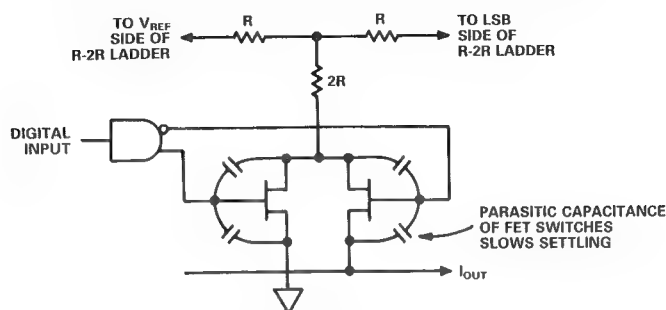


(OUTPUT IS A VOLTAGE BUT AS  $Z_{OUT}$  IS FIXED  
[ $= R$ ] THE DAC MAY ALSO BE USED AS A  
CURRENT OUTPUT DAC INTO A LOW IMPEDANCE).

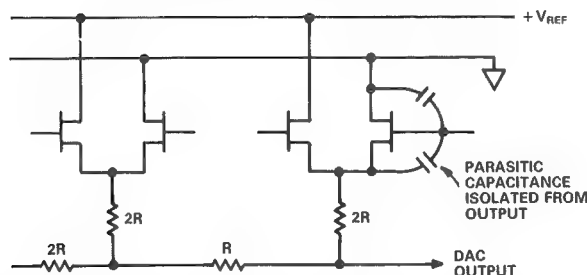
In the most common configuration, the "Standard R-2R DAC", the output is taken from the end of the network and each of the arms is switched between ground and a reference voltage. If the reference source impedance is assumed to be negligible it is evident that the impedance at the output terminal is  $R$  and does not change with code. It is slightly less evident but may quite simply be calculated from first principles that the output voltage is the product of the reference voltage and the normalized binary number applied to the switches—alternatively if the output is connected to a point at ground potential the output current will be equal to the reference voltage times the normalized binary code divided by  $R$ .

We thus see that the standard configuration offers voltage or current output and a constant output impedance. The manufacturing resistor trim algorithm is simple and also, since any stray capacity between the digital control lines and the switches goes to low impedance reference or ground lines, any charge injected into the DAC during digital transitions flows quickly to ground and so the glitch impulse is low and the settling time is fast. Nevertheless the configuration does have its drawbacks.

## DAC ARCHITECTURE AFFECTS GLITCH



"NORMAL" CMOS DAC STRUCTURE

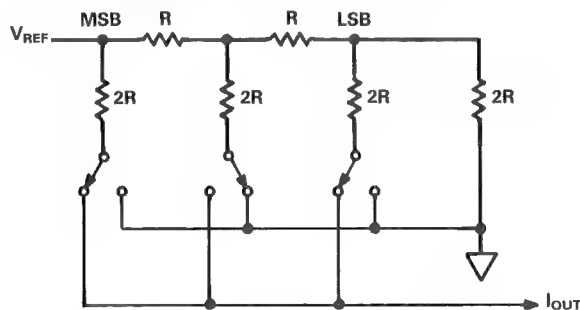


"BACKWARDS" DAC STRUCTURE OF AD7572 FACILITATES FAST SETTLING

The input impedance at the reference input depends on the digital code applied to the switches. This should not be a major problem but it does necessitate low impedance references and connections and prevents trimming of the DAC gain by means of a small trimmer in series with the reference input (gain must either be trimmed by trimming the value of the reference voltage or by altering gain elsewhere in the system). The other problem is a technological one but can be quite serious: as the switches change state the end of the resistance arms go from ground potential to  $V_{REF}$ . This can have two possible effects—modulation of switch resistance and modulation of the ladder resistance itself. If the ladder is made with diffused resistors the resistance value may depend on the bias between the resistor and the diffusion well in which it is sited and changes in bias will cause changes of resistance and so affect the DAC accuracy.

Modulation of switch resistance is more serious. There is no difficulty in replacing diffused resistors with thin film ones which do not have the resistance modulation problem but there is no substitute for semiconductor switches (DACs have been built with relays but this paper describes reality, not ivory towers). Again, this problem does not affect the performance of available DACs, it affects the type of DAC which is available. Many older MOS and CMOS processes suffered from switch channel modulation sufficiently to limit the specifications, or the range of available reference voltages, of DACs using this architecture. Modern processes can be made more tolerant of switch channel bias and standard DAC performance can be improved, but even so the possible reference voltage with this architecture is much lower than with an inverted R-2R DAC and the range of available products is smaller.

## INVERTED 3-BIT DAC USING R-2R LADDER NETWORK



(OUTPUT IS A CURRENT AND OUTPUT IMPEDANCE VARIES WITH CODE.)



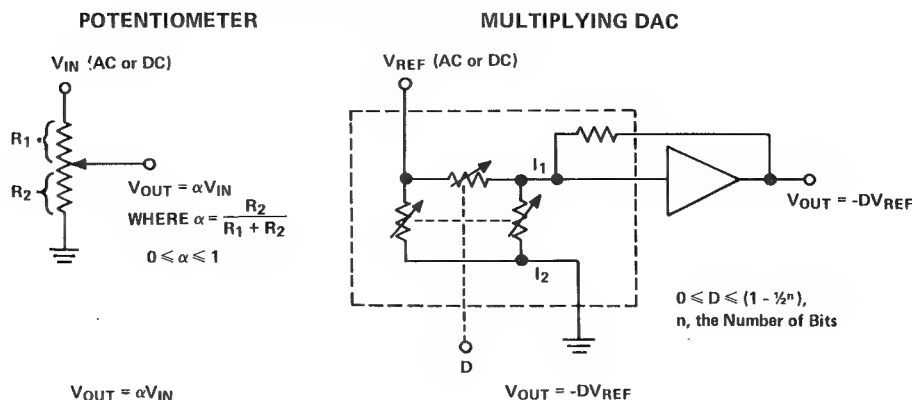
In the “Inverted R-2R DAC” the connections for the reference and output are reversed from the previous case. This means that the reference input impedance is code-invariant and so the gain of this DAC may be trimmed with a low value potentiometer in series with the reference input. The output impedance, though, now varies with code and the output can only be a current flowing to a virtual ground point. This code variable output impedance make frequency compensation of an output I-V converter more difficult since it is driven by a varying source impedance. Furthermore the capacity of the output line is much larger (and code-variable) because of the parasitic capacity of the FET switches, which degrades the high-frequency performance of such a DAC.

The greater charge injection in the output line during code changes, as a consequence of charge being coupled from the switches into the output line rather than into low impedance ground and reference lines, also reduces performance by increasing glitch energy. On the other hand the switches are always very near ground potential, whatever the value of reference, so switch resistance modulation is not a problem, and the reference may in many cases exceed the switch supply. Indeed if the switches are MOS devices, which can conduct in either direction, the reference may have either polarity and may even be ac.

All DACs have outputs which are the product of their reference and the normalized digital code applied to them but DACs which will function correctly when their reference is varied over a wide range (which must include zero but need not necessarily be bipolar) are known as “multiplying DACs” or MDACs. CMOS DACs with inverted R-2R ladder networks are particularly good MDACs since their reference may be bipolar and, if they are operated in the bipolar mode, they are capable of four quadrant multiplication. The basic MDAC may be thought of as a digitally-controlled potentiometer.

## MULTIPLYING D/A CONVERTERS

A multiplying DAC is nothing more than a digitally controlled potentiometer (attenuator).

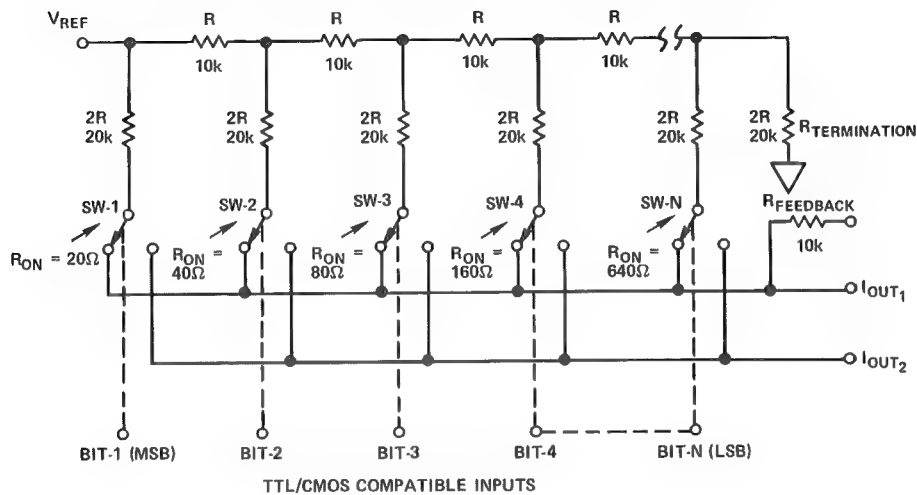


The output of such a multiplying DAC is the product of two variables, one digital (the input code) and one analog (the reference). They may therefore be used as computational devices, digitally-controlled attenuators, and digitally programmable resistors. There are even special MDACs, called “LOGDACs”, which contain very high resolution MDACs and decoding circuitry arranged so that each LSB change in the digital input produces a fixed percentage (decibel) change in the attenuation from reference input to output, unlike conventional MDACs where each LSB change produces an equal output increment. The difference may be considered equivalent to the difference between linear and logarithmic potentiometers.

It is important to realize that although MDACs are widely used as digitally controlled potentiometers and hybrid analog/digital computing devices they are widely used, with external fixed references, in normal DAC applications.

The final drawback of the inverted R-2R DAC is apparent only to the manufacturer—the trimming algorithm is considerably more complex than that of the standard part. With the use of computers during automated laser trim operations this is not a very serious problem. Both standard and inverted ladder networks may quite readily be trimmed for 14-bit INL and DNL over temperature. Above 14-bits trimming ladder networks becomes more demanding and although it is possible to manufacture 14-bit ladder networks which retain 16-bit performance over their full operating temperature range it is more usual to use mixed techniques—generally segmented plus ladder—at higher resolutions.

## AD754X FAMILY LADDER NETWORK SWITCHES ARE LARGER TOWARDS THE MSB



Each switch in a ladder network carries twice the current of its successor. Therefore it is customary to scale the switches, making the ones nearer the MSB end of the DAC larger, although scaling rarely continues for more than five or six bits.

### AUXILIARY DAC SYSTEMS

In addition to the cores which we have discussed in some detail DACs may contain a number of different subsystems. They include amplifiers, references, and more or less complex digital systems.

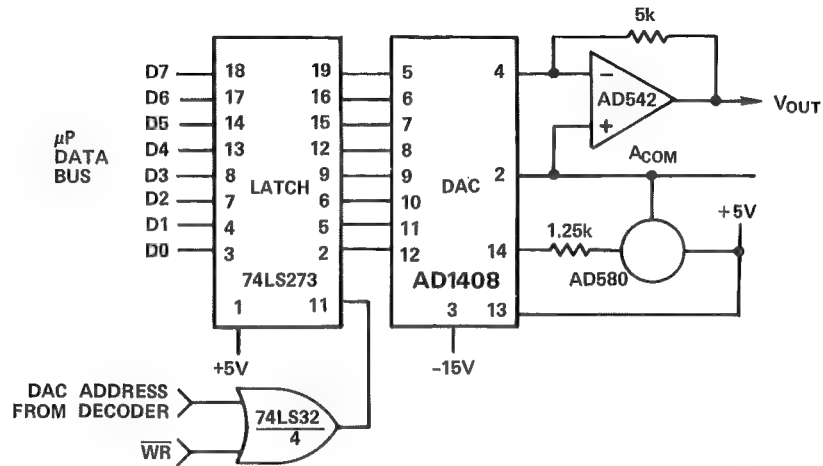
Amplifiers include buffer amplifiers for references, buffer amplifiers for segmented DACs (as described above), and operational amplifiers which function as I-V converters to convert current output DACs to voltage output DACs. In general the output amplifiers of DACs are not capable of driving large output currents—this is not because the design of such amplifiers is particularly difficult but because the increased dissipation due to a large output current will cause temperature gradients on the chip which will cause temperature related mismatch of the resistors in the DAC and thus degrade its accuracy. Where large output currents are required it is generally better to use a separate power output stage (which may often be a single power transistor within the DAC's output feedback loop).

All DACs require a reference—a source of voltage or current which defines the DAC output scaling. MDACs, as explained above, have an output which is the product of the reference input and the digital code but all other types of DAC require a fixed reference (possibly with provision for slight variation in order to provide gain trim). This fixed reference is frequently provided within the DAC itself.

Whether or not a DAC contains an internal reference depends on two things. If a DAC is required to function in a potentiometric manner together with other circuitry in a system it cannot use an internal reference. On the other hand many DACs would be improved by an internal reference but do not have one because the particular integrated circuit technology used to manufacture them is incapable of making a reference of adequate performance—this is discussed in more detail in the section of the seminar dealing with processes.

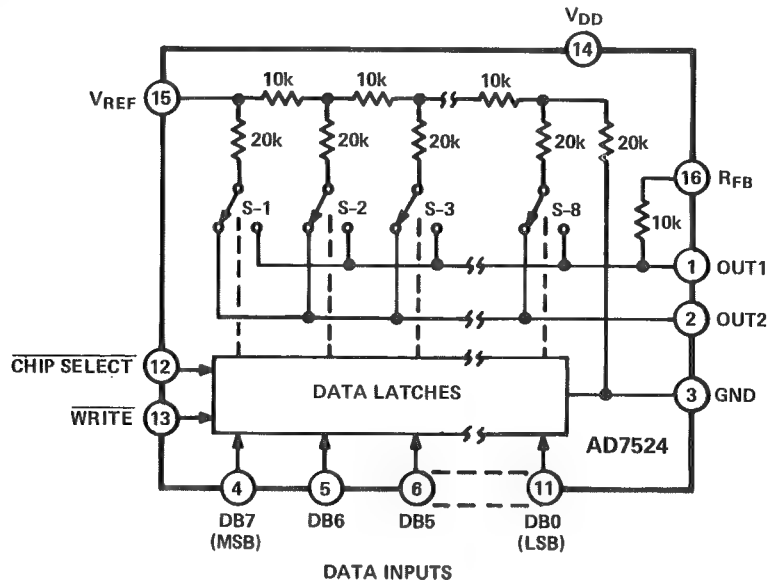
Finally all DACs contain digital circuitry. At its simplest this is merely a number of level-shifters to allow standard logic (TTL, CMOS, ECL, etc) to drive the DAC switches but today few DACs are so simple—most contain latches and many contain additional circuitry to enable them to interface to microprocessors with minimal additional componentry. Such circuitry has evolved slowly.

## μP INTERFACE TO EARLY 8-BIT DAC



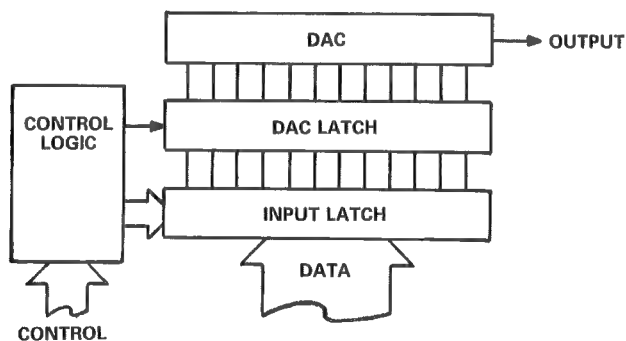
The earliest monolithic DACs contained a DAC core with TTL or CMOS interface levels and required that data be applied continuously to the inputs. Practical applications of such DACs, therefore, required the use of external latches to hold valid data and DAC manufacturers quite quickly included such latches in their products.

## EARLY CMOS DAC WITH INTEGRATED LATCH



While this worked well for  $n$ -bit DACs working from  $M$ -bit data buses where  $M \geq n$ , extra circuitry was still necessary where high definition DACs were to be loaded from narrow buses.

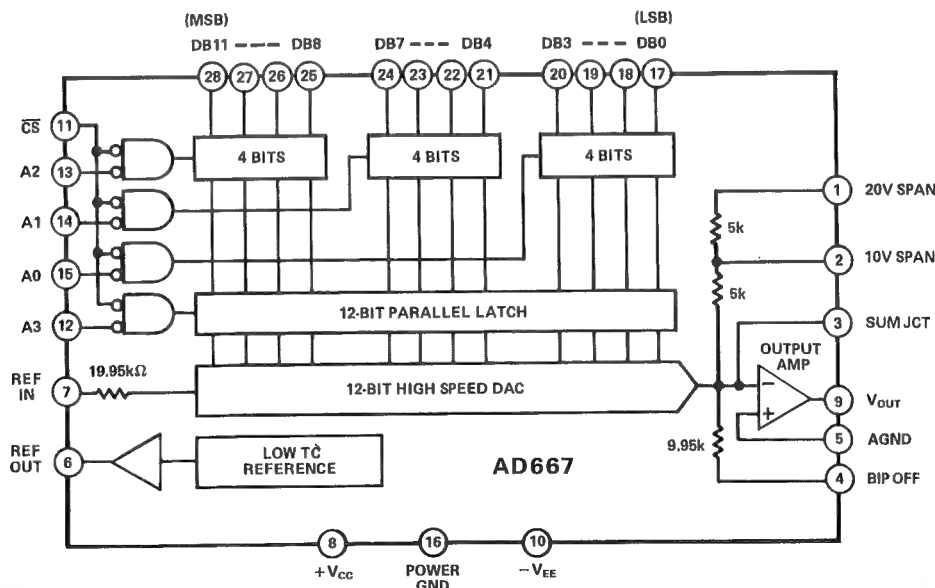
## A DOUBLE-BUFFERED DAC



This led to the introduction of the “double-buffered” DAC which contains two banks of latches—the first rank of “input” latches which acquire data from external sources and the second rank of “output” latches

which take their data from the input latches and present it to the DAC. The important feature of the double-buffered DAC is that the input latches may be loaded piecemeal without affecting the DAC output—only when the second rank latches are loaded (which need not occur until sometime after the data in the input latches is complete) does the DAC output change. The structure of the input latches of DACs have been made to load from 1-bit, 4-bit, or 8-bit data buses, and there are DACs containing shift registers, FIFOs, and RAM. The important principle is that there is an intermediate store where data is held prior to being presented to the DAC to update the output.

### AD667 FUNCTIONAL BLOCK DIAGRAM



The AD667 is an excellent example of a DAC containing most of the auxiliary subsystems mentioned in this section. It is a 12-bit voltage output DAC containing its own reference, buffer, and output amplifier and having a double-buffered data structure which allows it to be loaded from microprocessors having 4-bit, 8-bit, 12-bit or 16-bit data buses.

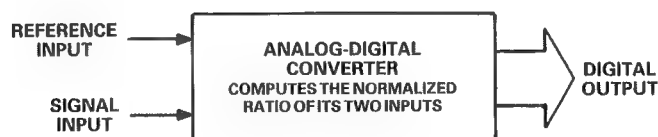
### AD667 FEATURES

- Complete 12-Bit D/A Function
- Double-Buffered Latch
- On Chip Output Amplifier
- High Stability Buried Zener Reference
- Single Chip Construction
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max
- Settling Time: 4μs max to 0.01%
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs

### ADC ARCHITECTURES

There are innumerable ways of obtaining a digital representation of an analog quantity, which is what an analog-digital converter does, but all of them involve comparing the input to the converter with a reference in some way that allows the computation of the ratio of the two quantities.

### BASIC ANALOG-DIGITAL CONVERTER FUNCTION



This section of the seminar considers a number of the more common systems for performing this function. They are the flash converter, and its slower, but more economical and higher resolution, variant the half-flash

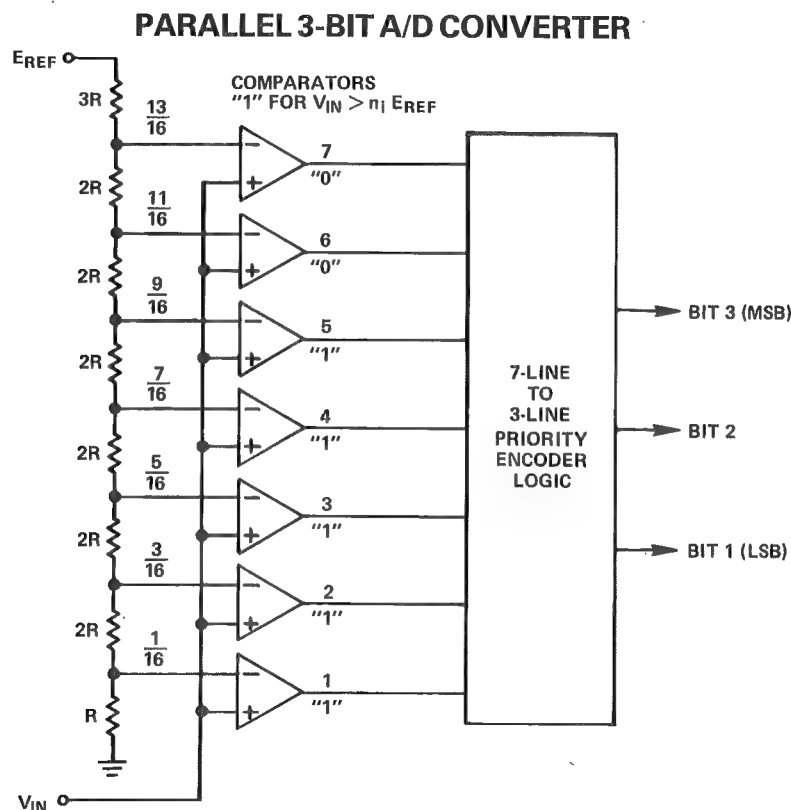
converter, the various types of integrating ADC and, closely related, the two types of voltage-to-frequency converter, and the two types of ADC incorporating DACs—the tracking and the successive approximation converters. Each type will be considered in turn and we shall also consider an ADC system, the floating-point ADC, which may be used to increase the dynamic range of an ADC.

## ANALOG-DIGITAL CONVERTER TYPES

Flash and Half-Flash	<ul style="list-style-type: none"> <li>• Fast</li> <li>• Power-Hungry</li> <li>• Lower Resolution</li> </ul>
Integrating	<ul style="list-style-type: none"> <li>• High Resolution</li> <li>• Inexpensive</li> <li>• Slow</li> <li>■ Noise Immune</li> </ul>
Voltage-Frequency Converters (VFCs)	<ul style="list-style-type: none"> <li>• Fast Response But Slow Conversion</li> <li>• Serial</li> <li>• High Resolution</li> <li>• Noise Immune</li> </ul>
Tracking (Counter/Comparator)	<ul style="list-style-type: none"> <li>• Fast in Track</li> <li>• Slow in Multi-Channel Applications</li> <li>• Susceptible to Noise</li> </ul>
Successive Approximation	<ul style="list-style-type: none"> <li>• Quite Fast</li> <li>• Flexible and Versatile</li> <li>• Accurate</li> </ul>
Floating-Point	<ul style="list-style-type: none"> <li>• Uses Any Type of ADC</li> <li>• Wide Dynamic Range</li> <li>• Complex</li> </ul>

## FLASH & HALF-FLASH CONVERTERS

The flash or parallel ADC is the fastest variety of solid-state ADC. An  $n$ -bit flash converter consists of  $2^n$  resistors connected in series with the reference voltage applied across the chain (all the resistors are equal except the top one, which is 1.5 times the value of the rest, and the bottom one, which is 0.5 times). In a unipolar flash converter the bottom of the chain is grounded but in a bipolar one the top and bottom of the chain are connected to positive and negative references respectively. A comparator is connected to each resistor junction, which requires  $2^{N-1}$  comparators, and the signal input is connected to the other input of all of them. The comparator outputs are connected to the inputs of a logic circuit called a priority encoder.



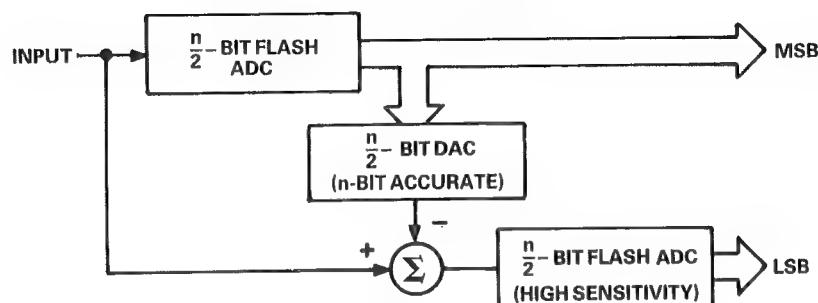
It is evident that the voltages on the comparator inputs, reading from the bottom of the chain, are 0.5 LSB, 1.5 LSB, 2.5 LSB, etc., above ground or the negative reference, until the highest is 1.5 LSB below the reference voltage, and that all the comparators whose reference inputs are lower than the signal input will have one output state while all the rest will have the other. The priority encoder has as its output the number of the highest comparator on the chain which has an input larger than its reference and this, of course, corresponds to the magnitude of the input voltage and therefore the system performs an analog-digital conversion. Since all the comparators are working simultaneously the time between a signal being present on the input and the corresponding digital code becoming available at the output is the sum of the comparator propagation delay and the priority encoder propagation delay—both may be very short and flash converters of 6-bit and 8-bit resolution are available with conversion times well under 5ns—corresponding to conversion rates of hundreds of megasamples/second. Some flash converters contain latches in either the comparators or the logic circuitry to lock the output state to prevent it from changing while a reading is taken.

The basic concept of a flash converter is simple and, providing the comparator offsets are all less than 0.5 LSB, it has no missing codes (although its INL will depend on the quality of its resistor matching—and a flash converter could be made deliberately nonlinear if such a feature was required for a particular application). But despite its speed and lack of missing codes the flash converter has three major disadvantages: its size, its input impedance, and its power consumption. An  $n$ -bit flash converter contains  $2^n - 1$  comparators (if it has an extra comparator to indicate overrange, as many flash converters do, it contains  $2^n$ ). Thus an 8-bit one contains 255 comparators and a 10-bit one 1023. Such large numbers of comparators, which are precision analog circuits and not simple memory cells, occupy quite large chip areas, even with modern chip component densities, and converters of these resolutions are correspondingly expensive. Since the input is applied to every comparator the input impedance in a converter containing a large number of comparators will be the parallel combination of all their input impedances—which makes high demands on the buffer circuit or SHA driving the converter and may make the analog bandwidth substantially less than the Nyquist frequency implied by the conversion rate. Furthermore, in order to achieve adequate speed the comparators must consume relatively high currents and therefore high resolution, high speed, flash converters consume considerable amounts of power.

In many demanding applications users are prepared to pay these cost and power penalties but at present 12-bit resolution is impracticable and 16-bit is impossible.

For higher resolutions the “half-flash” or “subrange” converter offers a development of the technique which gives higher resolution and lower power and system complexity at the cost of longer conversion times and greater conceptual complexity. A half-flash converter is illustrated in the diagram. It consists of two  $n/2$ -bit flash converters, a  $n/2$ -bit DAC, and a subtractor circuit.

### BASIC HALF-FLASH CONVERTER (FEED FORWARD ARCHITECTURE)

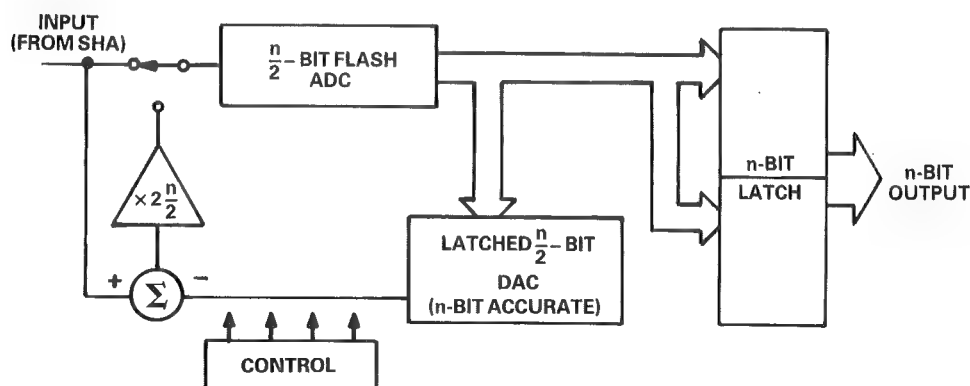


The input signal is applied to one of the  $n/2$ -bit flash converters (which must be accurate to better than  $n$ -bits, despite its relatively low resolution) which provides as its output the  $n/2$  most significant bits of the conversion. These  $n/2$  bits of data go both to the output and to an  $n/2$ -bit DAC (again  $n$ -bits accurate) which gives an analog output equal to the  $n/2$  MSBs of the input, which are subtracted from it, leaving a signal containing only the  $n/2$  LSBs which is applied to a second flash converter of  $n/2$ -bits resolution. Either this second converter is  $2^{(n/2)}$  times as sensitive as the first, or the signal is amplified by  $2^{(n/2)}$  before being applied the converter which provides the LSBs for the output.

It is evident that although the MSBs of the conversion are available as quickly as with a normal flash converter the LSBs are additionally delayed by the propagation delays of the DAC, the subtractor, and the second flash ADC (and the amplifier if one is used). The technique is therefore somewhere between two and three times slower than a simple flash converter but where a simple N-bit converter contains  $2^n$  comparators this one contains only  $2^{(n/2+1)}$  comparators plus, of course, a DAC and a subtractor. A half-flash converter is therefore considerably simpler, uses fewer components, and is less power-hungry than a full flash converter.

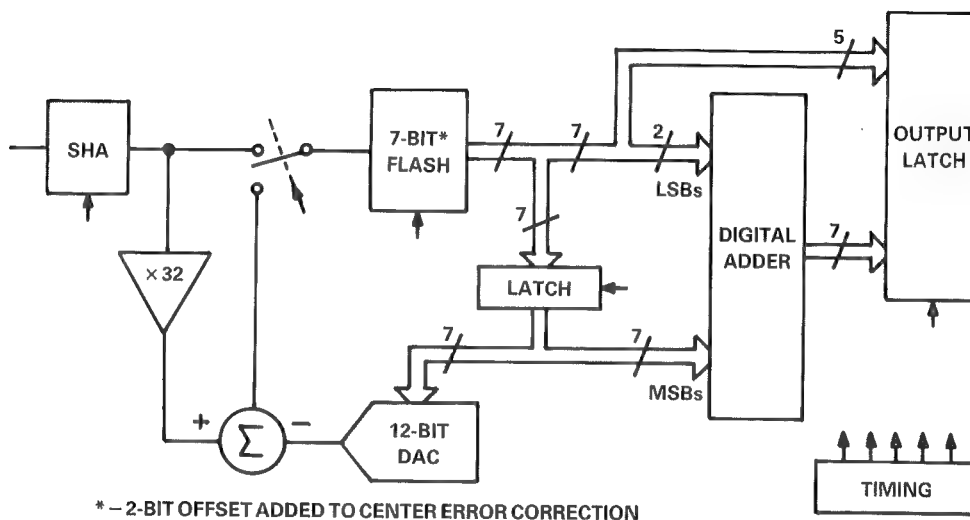
The feedback subrange ADC uses even fewer components, since it contains only one  $n/2$ -bit flash ADC, but is still more complex in theory. The MSBs from the first conversion are latched to the DAC, and the DAC output subtracted from the original signal and the result amplified as before but in this converter the same  $N/2$ -bit ADC is used again for the second conversion. This requires some extra signal switching, timing, and data latches.

### FEEDBACK HALF-FLASH ADC



Even better performance can be achieved by using this basic technique with an extra bit of resolution in the flash converter and using a digital adder for error correction. The AD375 and HAS1201 are two  $1\mu\text{s}$  12-bit ADCs using this architecture.

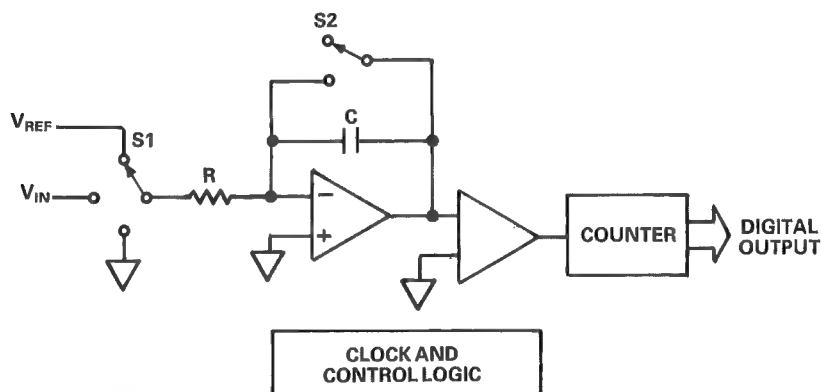
### AD375 – $1\mu\text{s}$ 12-BIT FEEDBACK SUBRANGE ADC WITH DIGITAL ERROR CORRECTION



## INTEGRATING ADCs

Integrating analog-digital converters are slow. They are, however, inexpensive, simple in concept, relatively immune to noise, and can be made to consume very little power. They are the form of ADC generally used in digital voltmeters and all applications where slow transducers (thermocouples, etc.) drive a display.

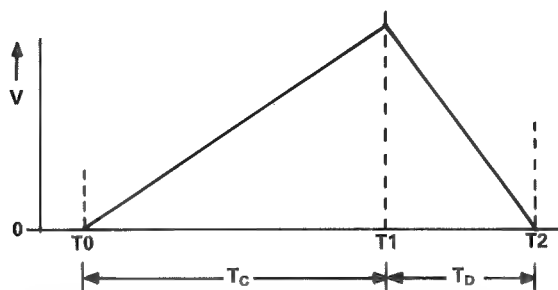
### BASIC INTEGRATING ADC



The basic system consists of an integrator (an operational amplifier and a capacitor C), a comparator, an up/down counter, and a clock and control logic.

The integrator is held discharged. At the start of a conversion it charges from the unknown input voltage, through the resistor R, for a fixed time determined by the clock and the counter. It is then discharged by applying a known reference voltage to the resistor and the time that it takes to discharge is read by the counter. Since the integrating capacitor, the resistor, and the clock frequency are unchanged during the charge and discharge cycles it is evident that the ratio of the charge and discharge times is equal to the ratio of the reference and unknown input voltages. The conversion accuracy is unaffected by the absolute values of R, C, or F and any noise on the input signal is integrated for the whole signal sampling period.

### OPERATION OF INTEGRATING ADC



THE INTEGRATOR CHARGES FOR FIXED TIME  $T_C$  WITH  $V_{IN}$ . THE DISCHARGE TIME WITH A FIXED REFERENCE ( $= V_{REF}$ ) INPUT IS THEN MEASURED ( $T_D$ ).

$$\text{RATIO } \frac{|V_{IN}|}{|V_{REF}|} = \frac{T_D}{T_C}$$

Leakage and offset in the integrator and hysteresis and offset in the comparator do affect the accuracy, though, and most practical integrating ADCs perform a conversion with the integrator input grounded to compute the errors due to these effects and then subtract these errors from the result of the actual conversion. Such complexity requires more logic and switching circuitry, although no more analog components, and so integrating ADCs are usually made with an IC process which is suitable for high density low power logic—CMOS. The use of CMOS, however, sets limits on the noise and accuracy possible from the integrator and comparator, and prevents the integration of very accurate references on the chip. The most accurate integrating converters, therefore, use external operational amplifiers and references and are capable of better than 18-bit accuracy, but even with CMOS amplifiers and references built on a CMOS chip 12- to 13-bit performance is possible.

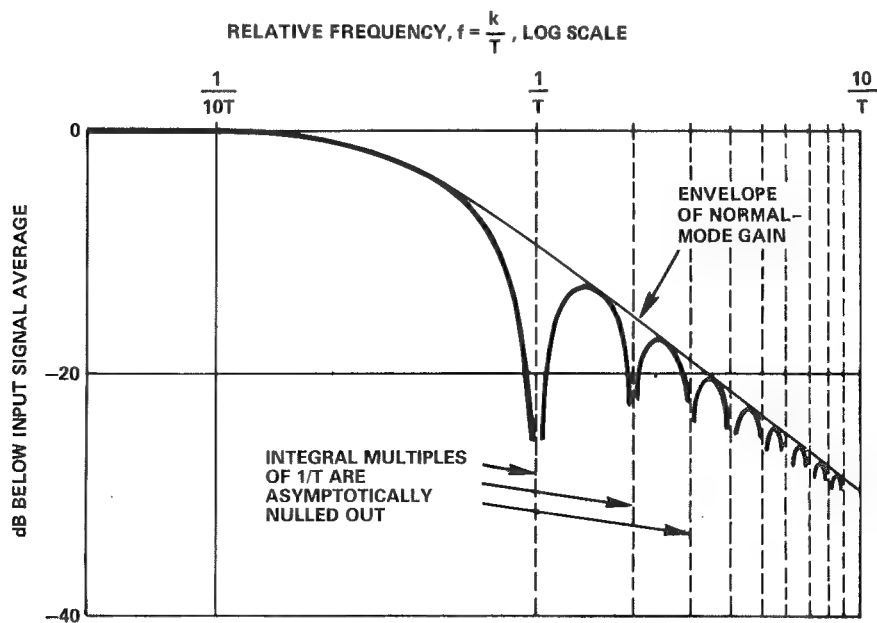


The nature of an integrating ADC is such that its DNL is very good and it does not suffer from missing codes—but its INL and gain accuracy may be far worse than its resolution, leading to the well-known “digital voltmeter effect” where naive engineers infer that a reading is accurate to 2.5 digits when quite simple cross-checks will show that it is only good to 5% but with 2.5 digit resolution.

The basic integrating ADC is unipolar. Where bipolar operation is required it is generally achieved by an extra comparator switching an inverting/noninverting buffer prior to the unipolar ADC, giving a signed rather than true bipolar response. This is, in fact, the most convenient form of data for DVMs, so true bipolar outputs are rarely available from integrating ADCs.

The sampling period,  $T$ , of an integrating ADC is fixed. If the frequency of any ripple on the input to the converter is an integral multiple of  $1/T$  a whole number of cycles will occur during each integration and the net contribution to the charge in the integrator due to ripple will be zero. Thus an integrating ADC has near infinite rejection of input frequencies  $n/T$  where  $n$  is an integer, and with suitable choice of  $T$  (say 16.667ms in the USA and wherever else line frequency is 60Hz and 20ms in Europe and wherever else it is 50Hz) line ripple on the signal input will be disregarded. This is another reason why integrating DVMs are popular—but it is also a strong argument against Europeans buying DVMs in the USA, where they are less expensive, for use in Europe, where the line frequency is different.\*

## NORMAL MODE RESPONSE OF DUAL-RAMP ADC

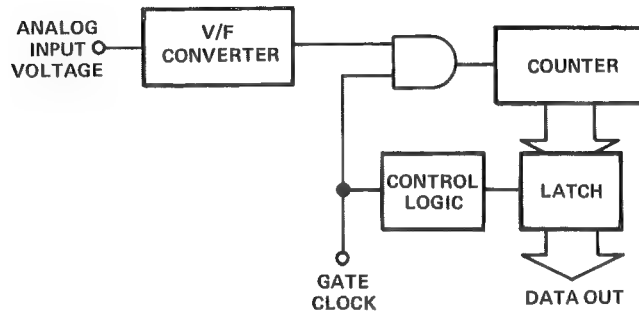


## VOLTAGE-TO-FREQUENCY CONVERTERS

An ADC technique closely related to the integrating ADC and having several of its advantages and disadvantages uses a voltage-to-frequency converter (VFC). A VFC is an oscillator whose output frequency is proportional to an input voltage. Simple VFCs may be made with 555 IC timers or even with neon lamps but their nonlinearity is very bad—purpose-built VFCs, on the other hand, are available with nonlinearity of 0.002% or better. A VFC is not, by itself, an ADC but it forms one with the addition of a counter and a timed gating circuit.

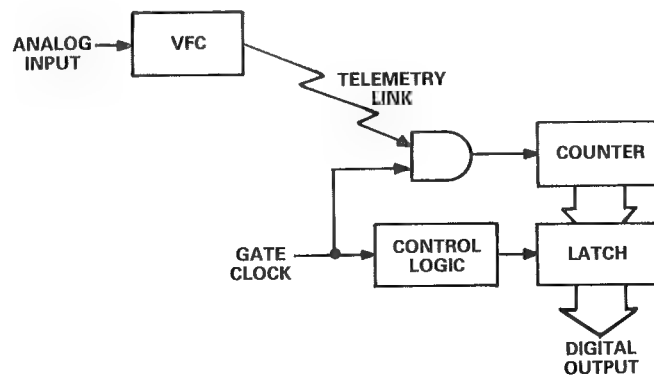
\*If the sampling period is 100ms, of course, the DVM will reject line frequencies of 50Hz, 60Hz and 400Hz.

## VFC USED FOR ANALOG-TO-DIGITAL CONVERSION



Like the integrating ADC, the gated VFC has inherently good DNL (no missing codes), signal integration for noise rejection, and high resolution. In addition it is particularly well-suited for telemetry applications since only a serial data channel is needed between the VFC and the counter/gate circuitry.

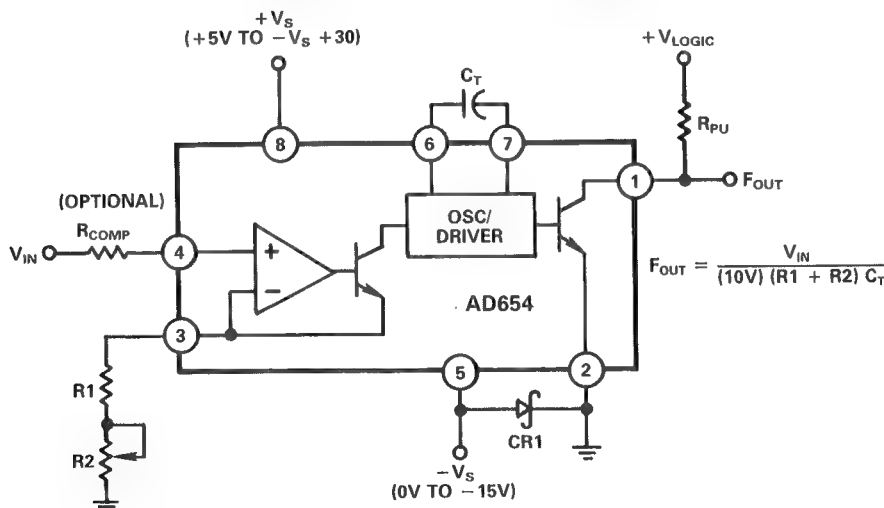
## A VFC IS IDEALLY SUITED TO TELEMETRY APPLICATIONS



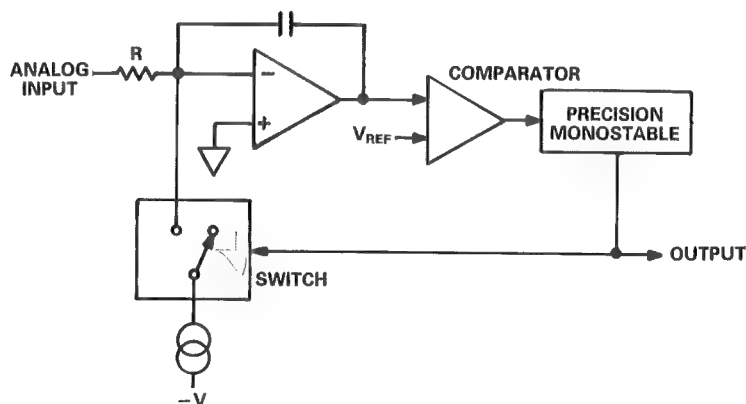
Most VFCs are used in unipolar mode (what is a negative frequency?) but if a bipolar ADC is required to be built from a VFC it is possible to inject an offset so that the VFC input can be positive or negative. This is analogous to a frequency modulated carrier.

The simplest form of VFC is an astable multivibrator whose timing current is set by the applied input voltage. The AD537 and AD654 are examples of such VFCs.

## STANDARD V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

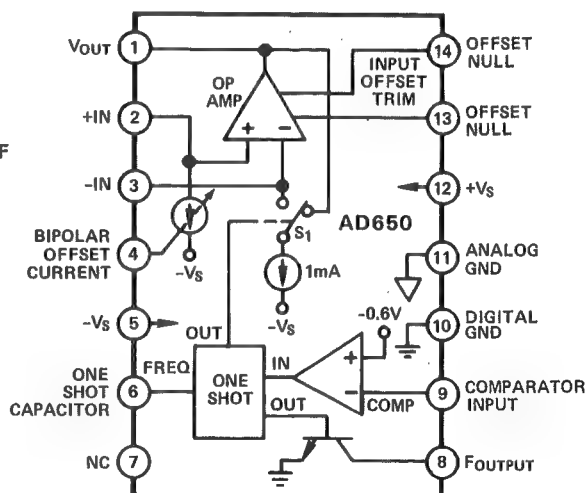


This architecture is similar to that of an integrating ADC in that the input is applied to an integrator but instead of integrating for a fixed time the input to the comparator is set at a reference voltage and when the integrator output passes the reference the comparator triggers a monostable multivibrator and fixed charge (a fixed current switched to the integrator input for a fixed time) removed from the integrator.



Obviously the larger the input voltage the faster the integrator will charge and the more frequently the monostable will fire to discharge it. The input is applied to the integrator at all times, so that all signals occurring at the input are integrated. The circuit works as a VFC and its accuracy is unaffected by variations in the integrating capacitor or the reference voltage—the total charge entering the integrator from the analog input is balanced by the number of charge packets removed when the monostable fires and this balance is uninfluenced by the integration capacitor or the comparator threshold. It is, of course, affected by variations in the monostable period, which is defined by another capacitor, by variations of the current source, and by any nonlinearities in the integrator during the discharge.

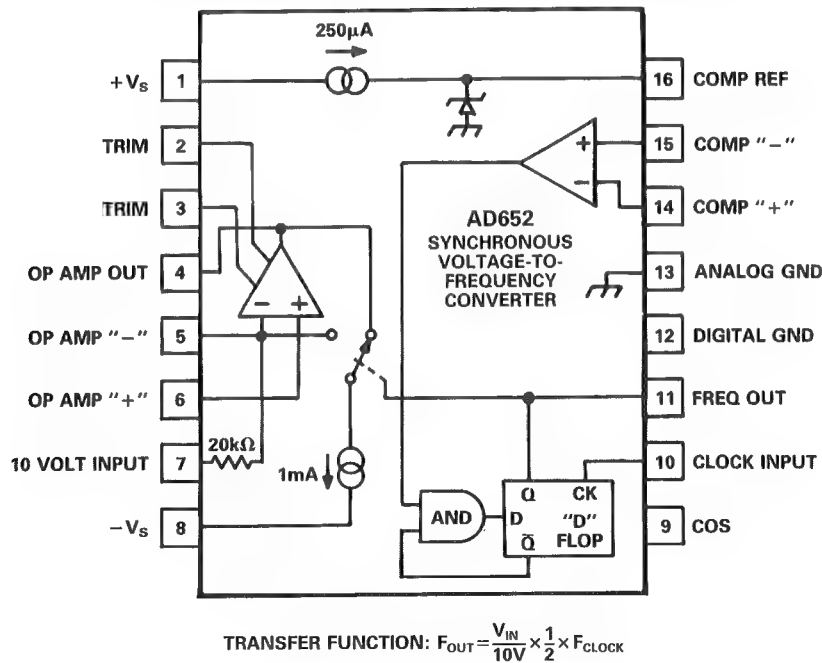
The AD650 contains a circuit intended to minimize switching nonlinearities. Instead of being connected to the integrator only during a pulse from the monostable the precision current source in the AD650 is always connected to the integrator. While the integrator is charging the current source is connected to the integrator output as a load, when the monostable fires the current is diverted to the integrator input where it discharges the integrator. However, the net current flowing in the integrator output is unchanged since the precision current source is still connected to the output, but now via the integration capacitor. This small change in architecture removes the majority of nonlinearities due to switching transients and causes the AD650 to be more than five times more linear than earlier attempts at monolithic VFCs using the same type of architecture.



**V/F Conversion to 1MHz**  
**Unipolar, Bipolar, or Differential V/F**  
**Very High Linearity**  
 0.002% typ at 10kHz  
 0.005% typ at 100kHz  
 0.1% max at 1MHz  
**Input Offset Trimmable to Zero**  
**CMOS or TTL Compatible**  
**Reliable Monolithic Construction**  
**V/F or F/V Conversion**

Nevertheless the gain and linearity of this type of VFC is still dependent on the stability and dielectric absorption respectively of the monostable timing capacitor. These can be made very good but at temperature extremes they are still likely to be the first factors to affect the performance of the VFC. There is no way of avoiding the problem with any type of conventional VFC architecture. A synchronous VFC, however, is unaffected by this particular difficulty.

### AD652 SYNCHRONOUS V-F CONVERTER

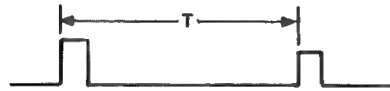


The AD652, a typical synchronous VFC, shows the difference between the two architectures. The AD651 is virtually identical to the AD652 except that its monostable multivibrator has been replaced by a D-type flip-flop driven by an external clock. In a synchronous VFC the integrator charges towards the threshold of the comparator just as in the asynchronous case but now the discharge does not take place as soon as the integrator passes the threshold but on the first clock pulse after it has done so, moreover the discharge pulse is no longer timed by a monostable but lasts for exactly one cycle of the external clock.

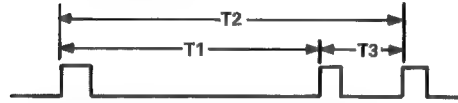
This arrangement removes all reliance on capacitor timing and makes the VFC gain depend only on the stability of the clock frequency and of the current source, yielding a further improvement in linearity and gain stability.

Synchronous VFCs are also particularly convenient for use in microprocessor systems since the VFC clock can be derived from the microprocessor clock and the VFC output read synchronously. They are useless, though, in any application where any amount of spectral purity is required in the VFC output (such as in phase-locked loop circuits) since the effect of clock-synchronism is to introduce massive phase jitter in the VFC output (the effect is equally visible on an oscilloscope or a spectrum analyzer and frequently misleads people inexperienced with synchronous VFCs into believing that the device is faulty).

## DIFFERENCE BETWEEN OSCILLOSCOPE DISPLAYS OF NORMAL VFC AND SYNCHRONOUS VFC



**NORMAL VFC.**  
T VARIES SMOOTHLY AS  
ANALOG INPUT IS ALTERED.

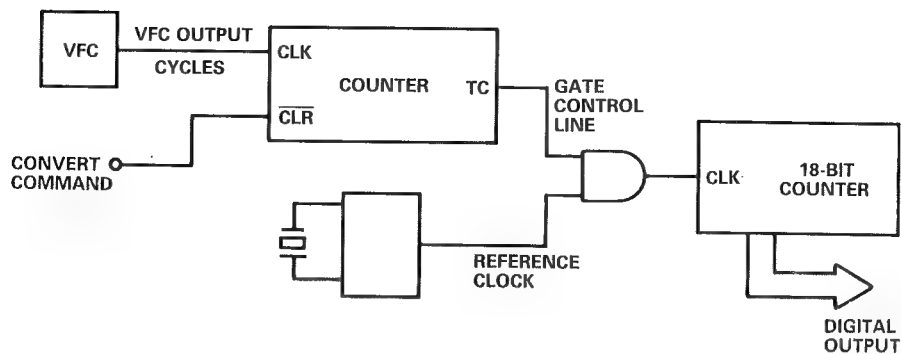


**SYNCHRONOUS VFC.**  
TIMING IS QUANTIZED AND THE RATIO  
OF CYCLES OF LENGTH  $T_1$  AND OF  
LENGTH  $T_2$  VARIES AS ANALOG INPUT IS  
ALTERED ( $T_3 = 1$  CLOCK CYCLE).  
 $T_1 = N T_3$      $T_2 = (N + 1) T_3$

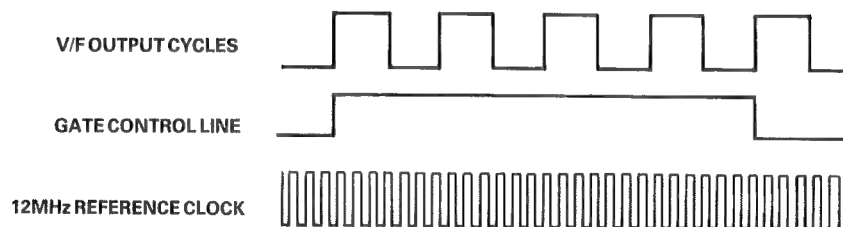
The resolution of a VFC depends on the sampling interval—even though changes in a synchronous VFC are quantized and those in a normal VFC are not the difference is not evident since it is the sampling time and not the quantized/nonquantized nature of the output signal which affects the resolution.

There is one way to beat this speed/resolution dilemma—to time the intervals between pulses of a nonsynchronous VFC. The AD1170 is an 18-bit smart ADC which uses this technique—counting cycles of a 12MHz reference clock for a preset number of cycles of its VFC. The AD1170 is called a “smart” ADC because it contains an 8051 microcomputer and the user can program whatever tradeoff between conversion time and resolution that he requires.

## GATED CLOCK ADC



## TIMING FOR GATED CLOCK ADC

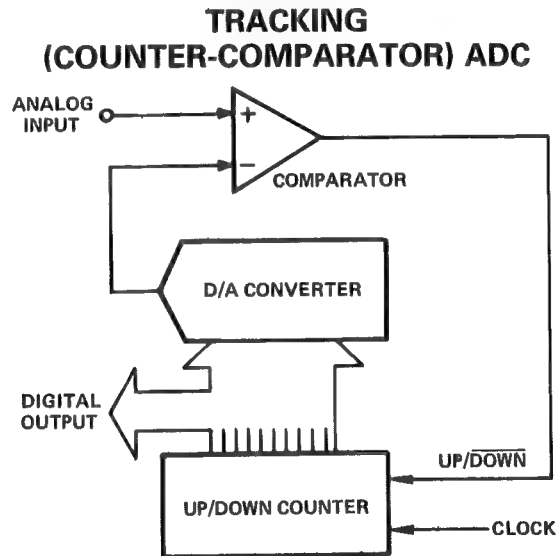


$C = \text{NUMBER OF V/F CYCLES DURING } T_{(INT)}$

$N = \text{NUMBER OF REFERENCE CLOCKS DURING } T_{(INT)}$

## TRACKING ADCs

The two remaining types of ADC both compare the output of a DAC with the analog input signal to determine its amplitude. A tracking ADC controls the DAC with an up/down counter—if the analog input is larger than the DAC output the comparator causes the counter to count up until the two signals are equal, if the analog input is smaller the comparator causes the counter to count down.



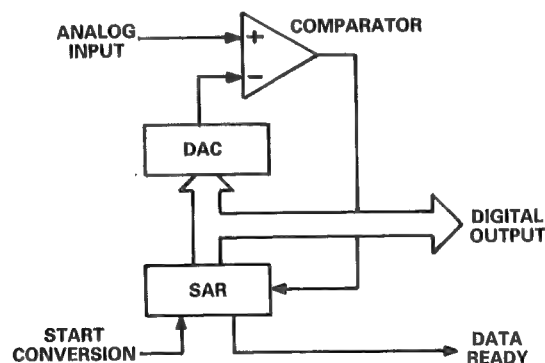
If a single comparator is used the counter will change direction every clock cycle once the DAC output has reached the analog input and the output will cycle above and below the actual value. If two comparators are used, with  $+0.5$  LSB and  $-0.5$  LSB offset respectively in the comparator enabling down counting and the one enabling up counting, then the converter will come to rest when the DAC output is within 0.5 LSB of the analog input.

If the analog input changes no faster than 1 LSB per clock cycle then the converter will track the input signal as it moves—on the other hand if the input steps from zero to full-scale or vice versa then the output will take  $2^n - 1$  clock cycles to follow it. The tracking converter is thus quite fast when working with a slowly-varying input and very slow in adjusting to a step. For this reason they are mostly used in single-channel low speed applications and are rarely manufactured as ICs.

## SUCCESSIVE APPROXIMATION ADCs

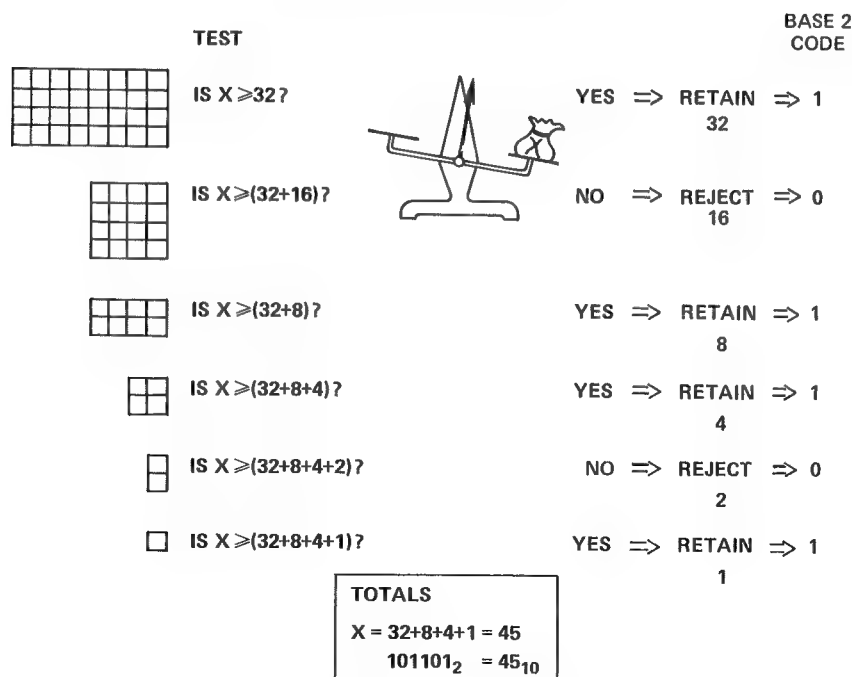
If the counter in a tracking ADC is replaced with a logic function called a successive approximation register (SAR) it produces a much more powerful type of ADC—the successive approximation ADC.

### SUCCESSIVE APPROXIMATION ADC



An SAR has an N-bit parallel output which is connected to the DAC data input. On receipt of a convert command the SAR sets all its bits to logic 0 except the MSB which it sets to logic 1. After a delay during which the DAC and comparator settle the comparator output indicates whether or not the DAC output is greater or less than the analog input. If it is greater the SAR resets the MSB to logic 0, if it is not it leaves it at logic 1. The next bit is now set to logic 1 and the cycle repeated—again if the DAC output is greater than the analog input the bit is reset to logic 0, otherwise not. The procedure is repeated with each bit in turn, from the MSB to the LSB and when it is complete the SAR output, and hence the DAC output, is within 0.5 LSB of the value of the analog input.

## SUCCESSIVE APPROXIMATION ADC ANALOGY



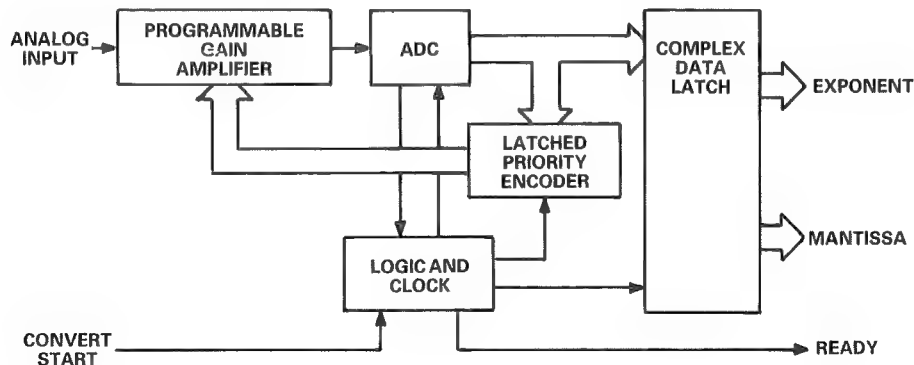
The concept of the successive approximation converter is directly analogous to that of a beam balance with a set of precision weights in successive binary ratio. One performs the measurement by placing the unknown weight on one side of the beam, then testing each known weight against the unknown, starting with the largest and working down. On each test if the weight tips the scale it is discarded, if it does not it is retained. The procedure continues to the smallest weight—if the balance is true and the weights all exact the unknown can be determined with a resolution equal to the smallest weight. (If a weight equal to half the smallest weight is added to the unknown side of the balance—analogue to half an LSB offset in the ADC—it can be shown that the measurement is always accurate to one half the smallest weight).

Since tracking and successive approximation ADCs use DACs they may be made unipolar, bipolar, or signed with little difficulty. Many such ADCs are designed for unipolar and bipolar operation with logic or switch selection of the bipolar offset.

Unlike the tracking converter the successive approximation converter does not deliver an output continuously—it performs discrete conversions. Normally ADCs start a conversion when they receive a logic signal telling them to do so but sometimes they convert continuously, retaining the result of the previous conversion until the new one is ready.

An n-bit SAR is barely more complex than an n-bit counter and easily implemented in most logic families. Therefore to make an N-bit successive approximation ADC we require an n-bit DAC, an n-bit SAR, and a comparator of adequate performance to handle 0.5 LSB differences at n bits. While it is perfectly possible to construct one's own ADC using from the individual components it is rarely economic to do so (it is sometimes economic to attach a DAC and a comparator to a microprocessor which is otherwise underutilized and use it as an SAR but as the price of ADCs drops this becomes less and less beneficial). Successive approximation ADCs are available in monolithic form up to 12-bit and in hybrid form at higher resolution (up to 16-bit). The choice of process used to manufacture a successive approximation ADC will depend on the exact functions required in the converter.

### FLOATING-POINT ADC



A floating-point ADC is not a particular type of converter architecture but is a system which allows any converter architecture to give greater dynamic range. A basic floating-point ADC consists of an ADC preceded by a programmable gain amplifier (PGA) and some logic. A floating-point conversion consists of two conversions: the first takes place with the PGA at minimum gain and the second takes place after the PGA has been set in the light of the result of the first conversion. The output then consists of an exponent, which is derived from the result of the first conversion, and a mantissa, which is the result of the second. This floating-point architecture considerably increases the dynamic range of an ADC but does not increase its resolution.

### AUXILIARY ADC SYSTEMS

As with DACs, when complete ADCs first became available in hybrid or monolithic form they were so welcome that users were quite prepared to surround them with a considerable amount of additional circuitry. Now that circuitry is gradually being built into the ADCs themselves.

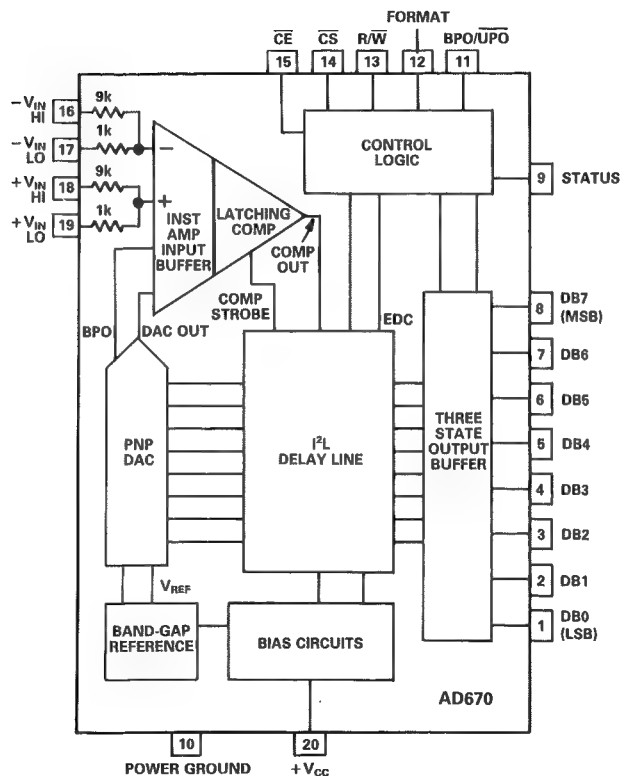
Such circuitry includes references, amplifiers and SHAs, and logic.

As with DACs all ADCs require references and many now contain band-gap buried-zener voltage references, according to the accuracy and stability required, on their chips or within their hybrid packages. Since CMOS processes do not make good references those ADCs which are fabricated in CMOS because of their logic requirements frequently do not contain references, but as second- and third-generation CMOS processes with good analog components (such as Analog Devices' LCCMOS) become more widely used more and more new ADCs do contain their own references.

The input impedance of many ADCs is quite low, and indeed the nature of the comparator in some successive approximation ADCs causes their input impedance to be modulated at the SAR clock rate. Frequently ADCs must be driven with differential signals with common-mode voltages superimposed on them. Furthermore, as discussed above and in the section of the seminar dealing with SHAs, the input of successive approximation ADCs must not move by more than 0.5 LSB during conversion. We thus see that ideally all ADCs should contain buffer amplifiers (which may also be SHAs in the case of successive approximation ADCs) to isolate them from high source impedances, common-mode voltages, and wideband input signals. This is slowly happening but since including an amplifier on a chip increases its size and power consumption and may be impracticable with some IC processes.

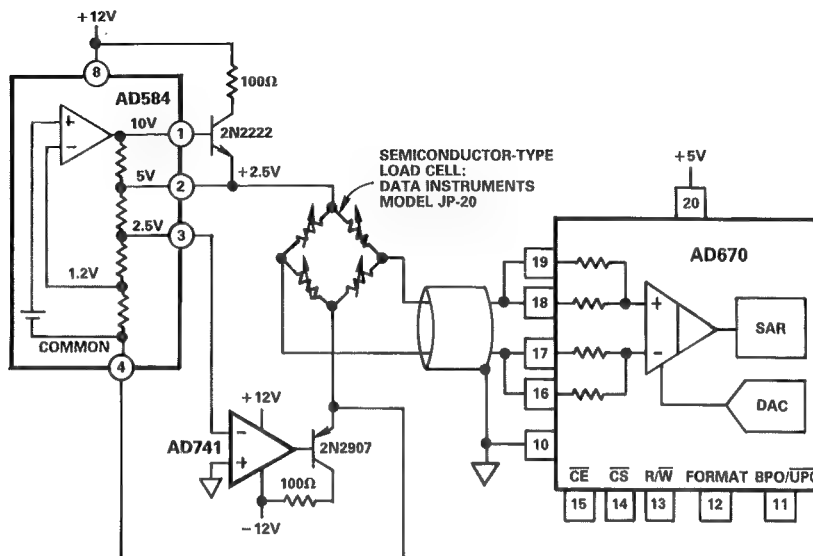


## AD670 BLOCK DIAGRAM



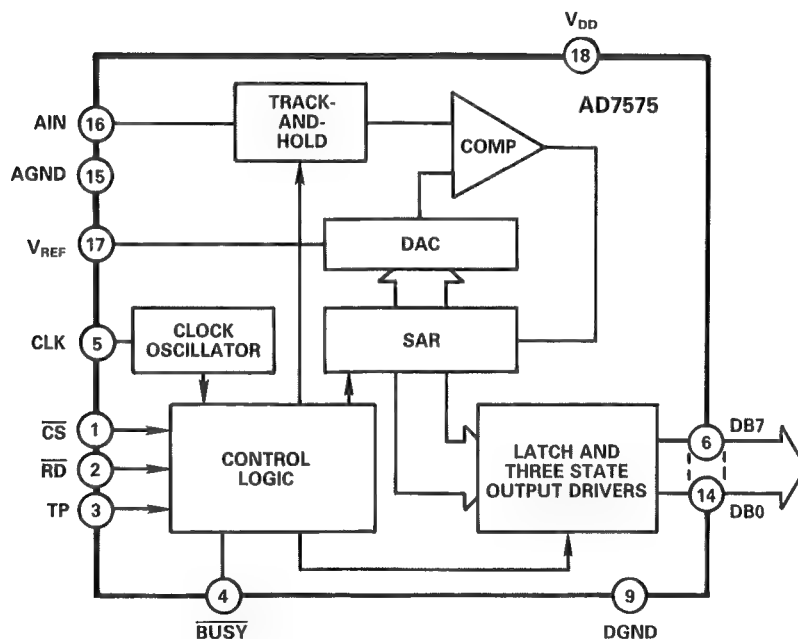
The AD670 is an excellent example of a monolithic ADC containing a differential amplifier. The amplifier has high input impedance, high common-mode rejection, and high gain and allows the AD670, in many applications, to be connected directly to a bridge sensor.

## AD670 LOAD CELL INTERFACE



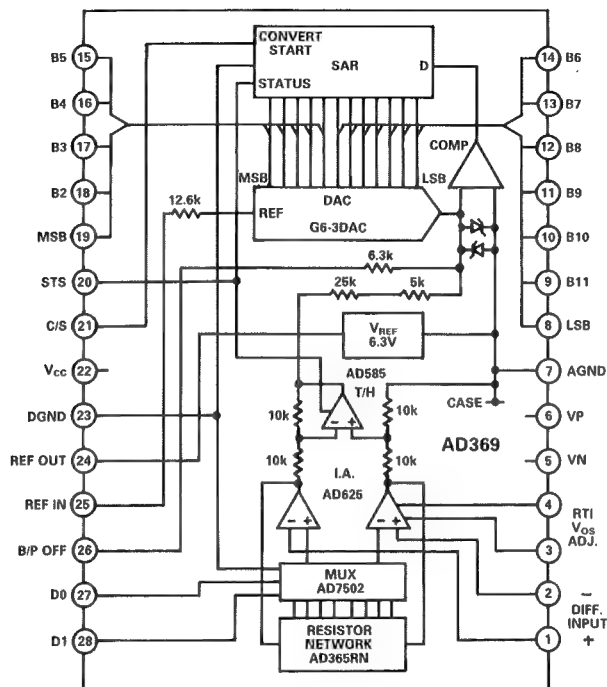
The AD7575 does not contain a differential amplifier but has its own SHA on its chip. It may be used with signal bandwidths of up to 50kHz.

### AD7575 FUNCTIONAL DIAGRAM



The AD369 contains a differential amplifier, a SHA, and a programmable gain amplifier (PGA)—essentially all the amplifiers that an ADC is ever likely to require. The AD369 is not itself a floating-point ADC but may be configured as one with relatively little external circuitry.

### AD369 HYBRID DAS WITH PROGRAMMABLE GAIN



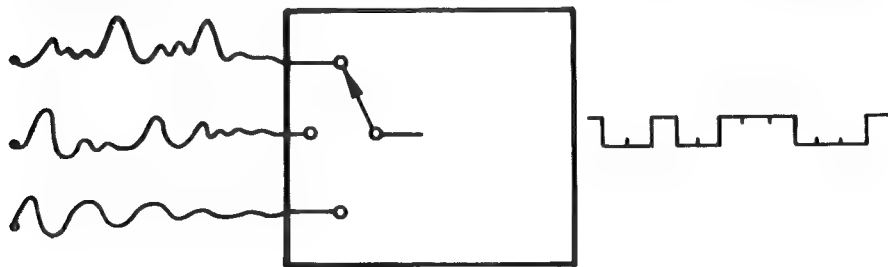
All ADCs contain logic in order to function at all. Today many contain many types of extra logic circuitry to make them more convenient to use. This generally consists of various types of output latches and buffers to ease the interfacing of ADCs to many types of microprocessor and display's. Many integration ADC's contain drivers for LCD and LED displays so that a DVM may consist of little more than a single IC and a display, and other types of ADC are frequently organized so that they may interface with several different widths of data bus. The conversion triggering circuitry is also becoming more sophisticated so that various automatic modes exist where reading data retriggers the converter, or the converter runs continuously but is locked out of the data buffer when it is being read, or other, more complex, schemes.

There are too many conflicting ADC requirements for there ever to be a single ADC for all applications, as data converter technology becomes continuously more sophisticated the possibilities for integrating extra functions within a monolithic ADC will lead to devices which can perform all the tasks which today are performed by a number of different types.

# **DATA ACQUISITION SYSTEMS**



# DATA ACQUISITION SYSTEMS

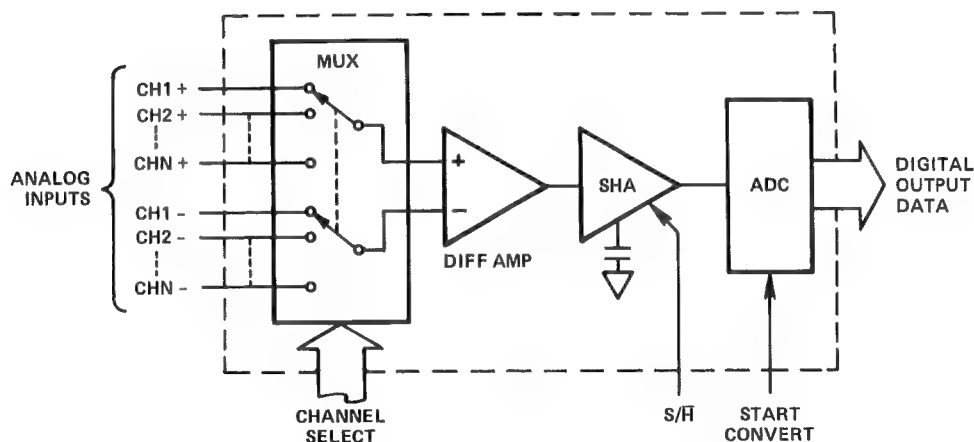


## 1. WHAT IS A DATA ACQUISITION SYSTEM?

Analog “real-world” voltage signals must be converted to a digital “word” form in order to communicate with a computer or microprocessor. Converting analog to digital signals is the essence of data acquisition.

A Data Acquisition System (DAS) may be defined as a circuit composed of an Analog-to-Digital Converter (ADC), preceded by appropriate multiplexing (if necessary), signal conditioning, and a sample-and-hold amplifier (SHA). A typical DAS block diagram is shown below.

## GENERALIZED DATA ACQUISITION SYSTEM



Although system requirements will dictate the actual DAS characteristics, some basic rules do apply. Input impedance of the system should be high, and common-mode rejection should be as effective as possible. The A-to-D conversion must be accurate to the given resolution and speed required. The S/H amplifier must be selected and accounted for based on the desired system parameters.

## **DATA ACQUISITION SYSTEM REQUIREMENTS**

- **Multiple Input Channels**
- **High Input Impedance**
- **Single-Ended or Differential Operation**
- **Sample-Hold Function Included**
- **Maintain Signal Accuracy Commensurate with ADC**
- **Ease of Use**

Each building block has certain performance characteristics. The multiplexer, for example, must have reasonably low “on” resistance, low leakage current, and a break-before-make operation. It is also desirable to include overvoltage protection, since many Data Acquisition Systems will encounter input signals which are outside the expected range.

## **DAS MUX REQUIREMENTS**

- **Low  $R_{ON}$**
- **Low Leakage Current**
- **Overvoltage Protection**
- **Break-Before-Make Action**

The differential amplifier (or single-ended buffer, if differential operation is not needed) should feature high common-mode rejection, low input bias current, low offset voltage, and sufficient linearity.

## **DAS DIFF AMP REQUIREMENTS**

- **Good CMR**
- **Low Bias Current**
- **Low Offset**
- **High Linearity**

The sample-hold amplifier should have the characteristics of low offset voltage, high linearity, fast acquisition and aperture times, and low sample-to-hold offset. Also, its associated hold capacitor should have sufficiently low dielectric absorption to prevent errors due to the “analog memory” effect.

## **DAS SHA REQUIREMENTS**

- **Low Offset Voltage**
- **Low S/H Offset**
- **High Speed**
- **Low D.A. Capacitor**

The ADC requirements are, of course, dictated by system performance goals. Conversion speed becomes important in large multi-channel systems, since only one channel can be converted at any given time. ADC accuracy is important in any system, and when the DAS under consideration is to be interfaced to a microprocessor, easy interface connections are desirable.

## **DAS ADC REQUIREMENTS**

- **High Speed**
- **High Accuracy**
- **Easy Interface**

A full data acquisition system may include additions such as the sensors which interface with the actual environment of interest (i.e., temperature, pressure, strain of materials, sound, atmospheric content). On the other side of the system is the digital data processing. Hardware interface with the designated processor is required to complete the task of data acquisition. In addition, hardware to implement control functions and calibration/error adjustment may be added to the system if needed.

## 2. APPLYING HYBRID TECHNOLOGY TO DAS CONSTRUCTION

Since each building block in a DAS has performance requirements which are best filled by different technologies, hybrid technology allows chips manufactured with incompatible technologies to be combined in a small, IC-size package.

### ADVANTAGES OF HYBRID DAS CONSTRUCTION

- Smaller Than Boards or Modules
- Can Use Multiple Technologies
- Low Cost
- Grounding/Decoupling Handled Internally

The AD369 is a good illustration of successful integration of a 12-bit DAS.

### AD369 FEATURES

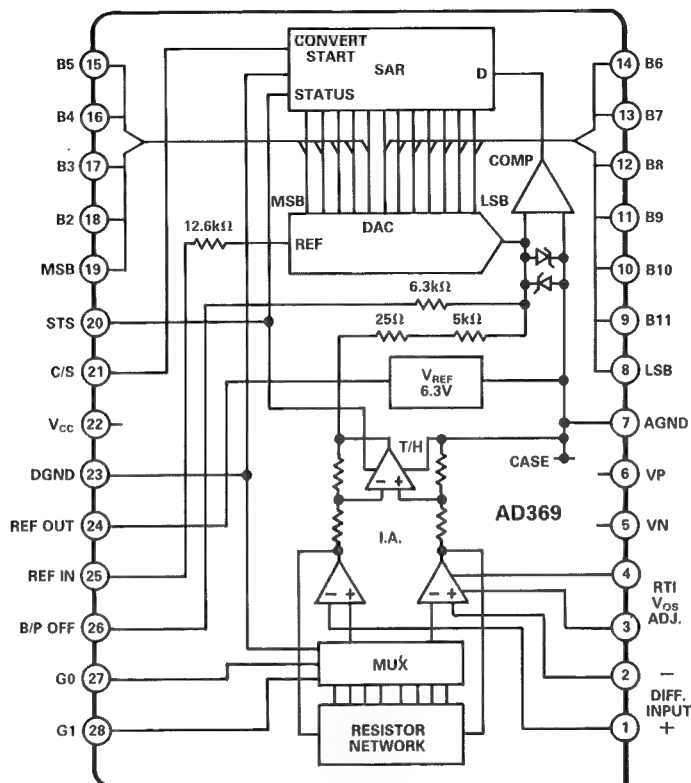
**Includes: Programmable Gain Instrumentation  
Amplifier, Track and Hold Amplifier  
12-Bit A/D Converter**

**Digitally Controlled Gain (1, 10, 100, 500)  
50kHz Throughput Rate**

**Small Size: 28-Pin Metal Hermetic Double DIP  
Guaranteed No Missing Codes Over Temperature  
True 12-Bit Linear; Error  $\leq 1/2\text{LSB}$  (B-Grade)  
Unipolar or Bipolar Operation**

**Low Power: 775mW  
Differential Input  
Internal Hold Capacitor**

### AD369 BLOCK DIAGRAM



This hybrid 12-bit data acquisition system conditions and converts an analog signal into a 12-bit digital word. Evolution of this device was made possible by utilizing several of Analog Devices' monolithic ICs and encapsulating them in a space saving 28-pin metal hermetic package. The AD369 consists of a resistor network, multiplexer, instrumentation amplifier, and track-and-hold amplifier, the output of which drives a successive approximation analog-to-digital converter.



The AD7502 CMOS multiplexer and the thin-film resistor network form the gain switching network for the AD625 programmable instrumentation amplifier. By applying a binary address input to the TTL compatible G0 and G1 control lines, gains of 1, 10, 100, and 500 are realized. As shown in the table below, the AD369 accepts full-scale voltage ranges of 10, 1, 100mV, and 20mV corresponding to gains of 1, 10, 100, and 500 respectively. With a gain of 500, full-scale range of the device is 20mV corresponding to 4.88 $\mu$ V per LSB.

## INPUT VOLTAGE RANGE SELECTION

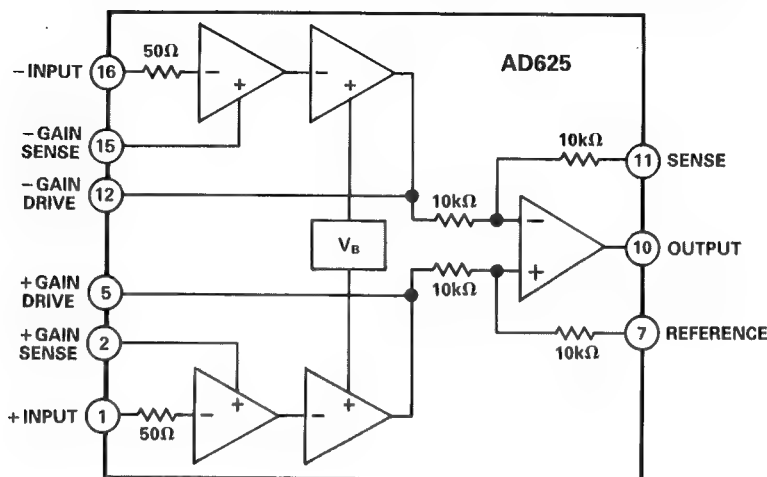
Gain Code		Programmable Gain Amplifier	Analog Input Voltage Range				One Least Significant Bit (LSB) Value
G0	G1	Gain	Unipolar	Bipolar			
0	0	1	0	+10V	-5V	+5V	2.44mV
0	1	10	0	+1V	-0.5V	+0.5V	0.24mV
1	0	100	0	+100mV	-50mV	+50mV	24.4μV
1	1	500	0	+20mV	-10mV	+10mV	4.88μV

The onboard thin-film resistor network has several advantages over discrete resistors. It not only minimizes P.C. board space but also enhances gain accuracy. Through the use of laser wafer trimming, these resistors can be matched to within 0.005%. With respect to the 0.02% inherent gain error of the AD625, the contribution of gain error due to the resistor network is negligible. Compared with discrete metal film resistors with 1% matching or resistor network packs with at best 0.015% matching, there is a definite advantage to using thin-film resistors when considering performance and cost.

Temperature effects also contribute to gain error. Using discrete resistors, thermal gradients in conjunction with mismatched temperature coefficients must be considered when the ambient temperature deviates from 25°C. For example, based upon an ambient temperature of 25° rising to 85°, and using discrete resistors with a typical T.C. of 50ppm/°C, an error of 3000ppm occurs. This error combines with the gain T.C. of 5ppm/°C for the AD625 to yield a total gain error of 3300ppm disregarding the effects of T.C. matching. Alternatively, the AD369's thin-film resistor network with T.C. of 25ppm/°C effectively reduces gain error by 1/2. In addition, the excellent T.C. matching of the thin-film resistors (5ppm/°C) further reduces gain error.

The nucleus of the analog section of the AD369 is the AD625 instrumentation amplifier depicted below.

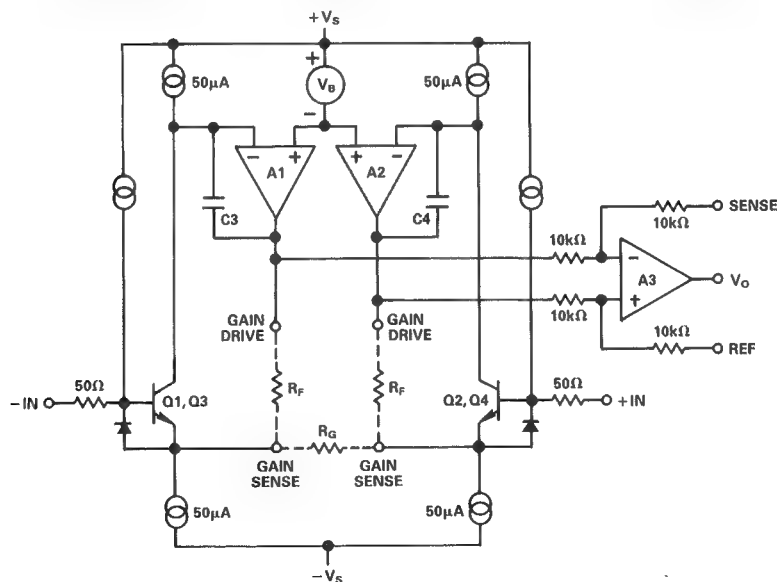
## AD625 INSTRUMENTATION AMPLIFIER



This monolithic instrumentation amplifier is based on a modification of the classic three-op-amp design. Referring to the preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of these amplifiers maintains the collector currents of Q1-Q4 constant. Thus, the input voltage appears across  $R_G$ , the gain setting resistor. As a result, a differential voltage is produced at the outputs of A1 and A2 which is given by the gain  $(2R_F/R_G + 1)$  times the differential portion of the input voltage. A3 configured as a unity gain subtractor, develops a single-ended output ( $V_{OUT}$ ) referred to the potential at the reference pin and free from common-mode signals.

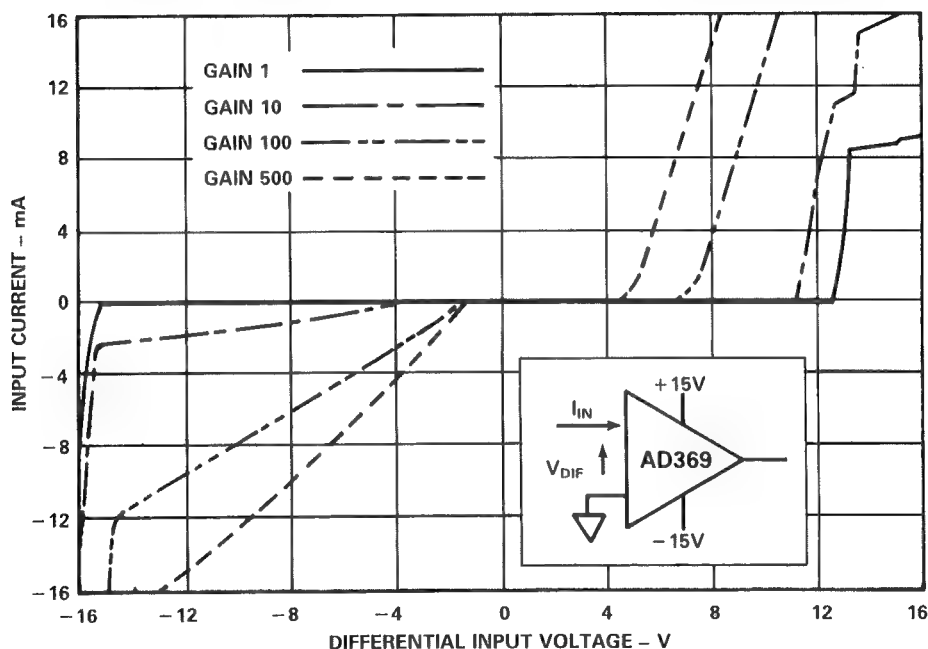
Resistor  $R_G$  determines the transconductance of the input preamp stage. Decreasing  $R_G$  for larger gain increases the transconductance. With this design, a very high open loop gain of  $3 \times 10^8$  at gain of 500 is developed. In addition, the gain-bandwidth product, determined by C3, C4 and the input transconductance, increases with gain to enhance frequency response. Moreover, input voltage noise, a critical parameter in a data acquisition system, is reduced to  $40\text{nV}/\sqrt{\text{Hz}}$  being determined by the collector currents of Q1-Q4.

## SIMPLIFIED CIRCUIT OF THE AD625



In many applications, the DAS front end will be exposed to input voltages that exceed the linear range of operation for the in-amp. Some form of input protection is required to limit input current to less than 20mA and to prevent the input voltage from exceeding either supply by one  $V_{BE}$ . Under differential overload conditions,  $(R_G + 100\Omega)$  appears in series with two diode drops (1.2V) between the plus and minus inputs in either direction. With no external protection at gain of 500, the maximum continuous overload voltage is approximately 2.5V.

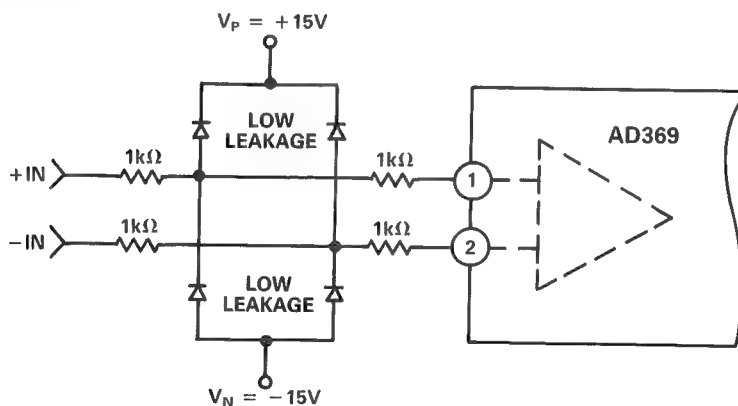
## INPUT CURRENT VS. DIFFERENTIAL INPUT VOLTAGE WITHOUT INPUT PROTECTION



1k $\Omega$  resistors in series with each input would safely limit the current for input voltages in the range of  $V_P = +15$  to  $V_N = -15$ V. The figure below shows the external components necessary to protect the AD369 regardless of gain. The four low leakage diodes limit the differential overload voltage to  $\pm 0.6$ V when the input voltages exceed the supplies. Input protection, however, is at the expense of degraded noise performance. The four 1k $\Omega$  resistors will degrade the noise performance to:

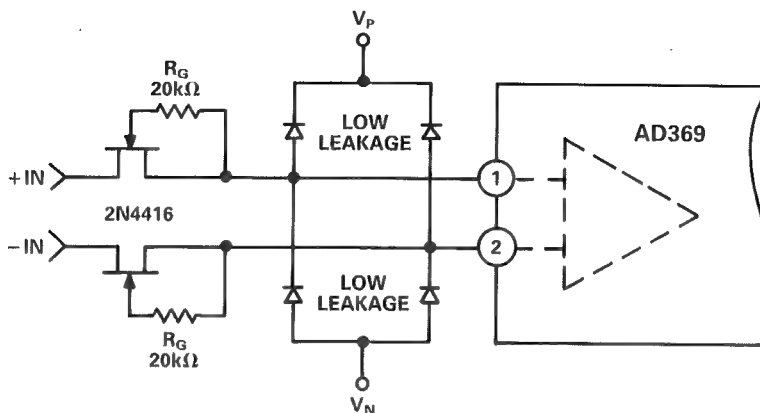
$$\sqrt{4KTR + (4\text{nV}/\sqrt{\text{Hz}})^2} = 7.9\text{nV}/\sqrt{\text{Hz}}$$

## INPUT PROTECTION CIRCUIT FOR AD369



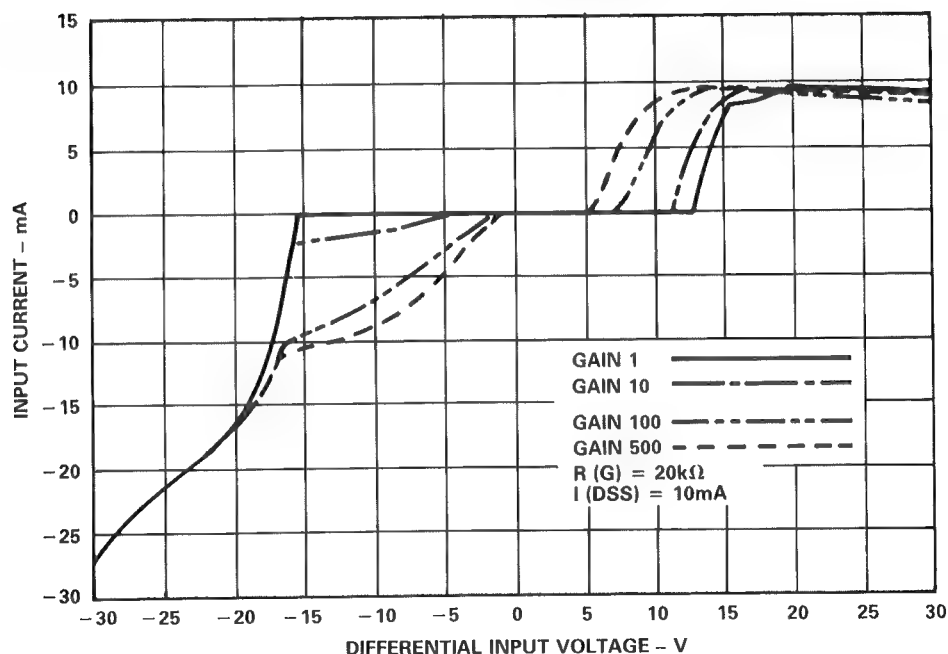
An alternate approach is to replace the resistors with low-cost FETs. FETs such as the 2N4416 with low  $I_{DSS}$  (9mA) and low on-resistance (170 $\Omega$ ) should be used. The 20k $\Omega$  resistor, in series with the gate, limits the reverse  $I_{DSS}$  current without introducing noise. Typical noise performance with this FET is 5.2nV/ $\sqrt{\text{Hz}}$ .

## LOW NOISE INPUT PROTECTION CIRCUIT FOR AD369



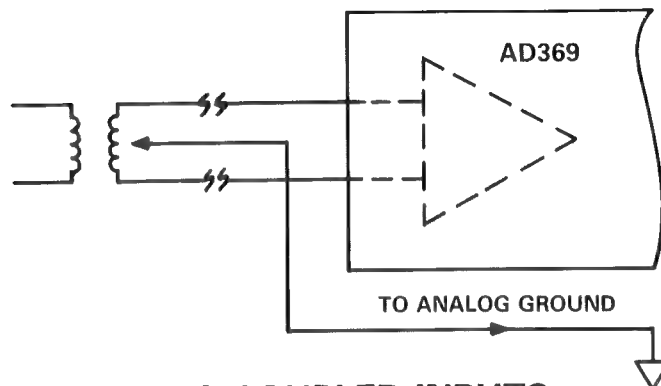
# AD369

## INPUT PROTECTION WITH 2N4416 FETs AND FD333 CLAMPING DIODES

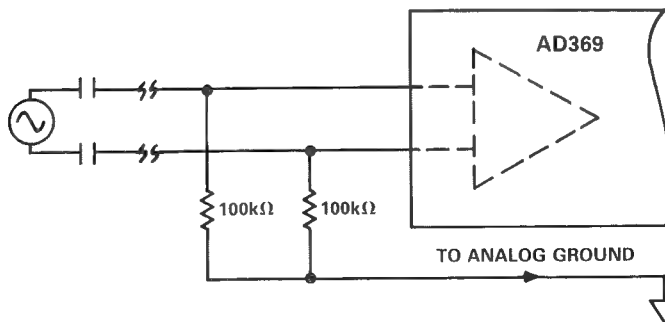


The AD369 DAS requires a direct return path for the input bias currents of the PGA input transistors. Failure to provide this path results in charging stray capacitances which appear as output drift or saturation. Therefore floating sources such as transformer coupled inputs must be returned to ground. AC coupled inputs require a different approach. The two  $100k\Omega$  resistors, however, do produce an offset voltage since input offset current flows through these resistors. This input offset voltage is RTI (i.e., referred to input) and after multiplication by gain contributes considerably to system error.

## GROUND RETURNS FOR BIAS CURRENTS WITH TRANSFORMER COUPLED INPUT

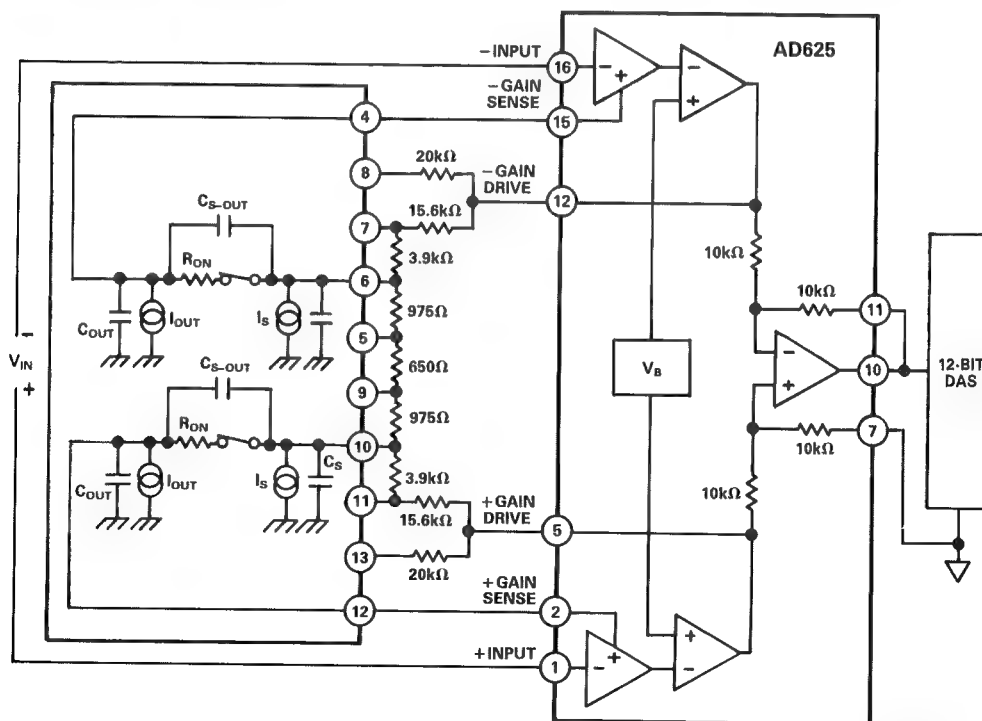


## WITH AC COUPLED INPUTS



Historically, the major problem in gain switching amplifiers has been the on-resistance ( $R_{ON}$ ) of the multiplexer. Since this resistance is in series with the gain setting resistor  $R_G$ , additional gain error and drift will occur. However, the AD625 incorporates gain drive and sensing thereby removing the multiplexer's on-resistance from the signal path. As evident from Table II, the total contribution of error at gain of 500 due to multiplexer on-resistance and leakage current is  $10.21\mu V$  appearing as an input offset voltage. Nulling of offset is achieved with a  $10k\Omega$  potentiometer connected between Pin 3, Pin 4 and the positive supply.

## SPGA WITH MULTIPLEXER ERROR SOURCES



Induced Error	AD625C	AD7502KN	Specifications Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Current 40nA	Switch Resistance 170Ω	$40nA \times 170\Omega = 6.8\mu V$	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	$60nA \times 6.8\Omega = 0.41\mu V$	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ	Differential Leakage Current ( $I_S$ ) + 0.2nA - 0.2nA	$2(0.2nA \times 20k\Omega) = 8\mu V/16$	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ	Differential Leakage Current ( $I_{OUT}$ ) + 1nA - 1nA	$2(1nA \times 20k\Omega) = 40\mu V/16$	2.5μV

## AD369 SYSTEM TIMING SPECIFICATIONS

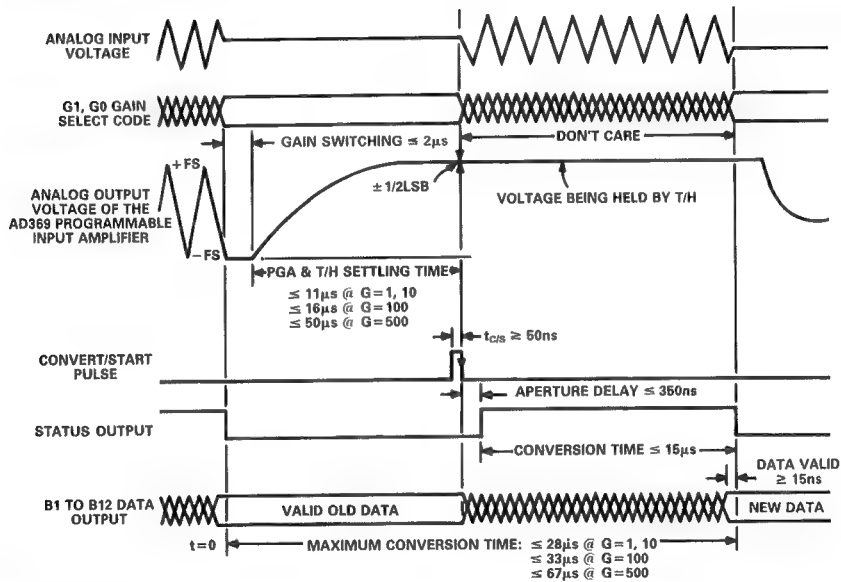
To perform data acquisition with the AD369, the user must first select the amplifier gain. This is accomplished by entering a two-bit binary word which serves as the gain code. After the correct code is entered, a maximum switching time period of  $2\mu s$  will elapse and the output stage of the instrumentation amplifier will begin to settle. Settling time for the PGA is dependant on gain; the maximum time being in the gain of 500 mode.

The Convert-Start (C/S) pulse may be submitted after the gain settling time has elapsed. The C/S pulse must be a minimum of 50ns wide; the falling edge initiates the conversion process and, after the SHA aperture delay time of 350ns maximum, the Status output goes high. Since the amplifier settling time is much greater than the SHA acquisition time, the acquisition time of the SHA has no effect on the timing on the first conversion. Conversion time from the falling edge of the C/S pulse is  $15\mu s$ , maximum.

A low output on the status line indicates a completed conversion; the SHA now returns to the tracking mode. The digital data is valid at the output for at least 15ns prior to the falling edge of the Status pulse. This gives sufficient set-up time at the output to assure accurate data transmission to an external latch if immediate extraction (triggered by falling edge of the Status pulse) is desired. This feature of the DAS enables the user to maximize

throughput rates when using the AD369 under microprocessor control. Data is valid at the output until the next falling edge of a C/S pulse. A timing diagram for the first conversion is shown below.

## AD369 TIMING DIAGRAM WITHOUT PIPELINING

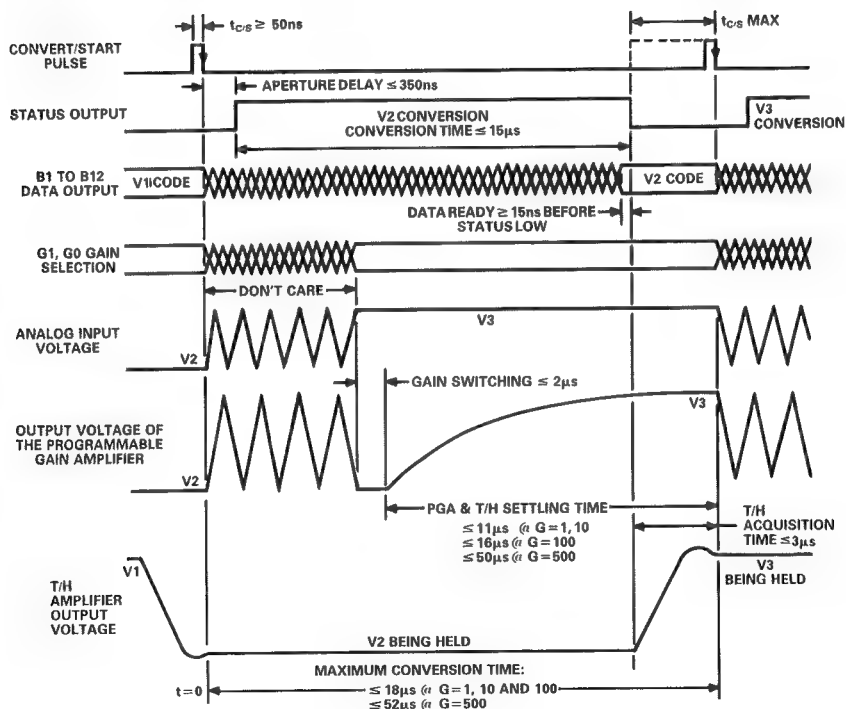


DAS throughput rates are maximized by “pipelining” the acquisition process, as shown below. As soon as a conversion has been initiated by a falling edge of the C/S pulse, the system develops into a “don’t care” state and a new set of conditions may be imposed. The figure shows the timing when a new gain is selected after the falling edge of the C/S pulse. A new voltage begins to settle at the output of the PGA no more than  $2\mu s$  later. Since the conversion has already begun, the amplifier settling time occurs concurrently with the previous A-to-D conversion.

At gains of 1 and 10, the output of the amplifier will settle before the conversion time. In these cases, once the status output goes low indicating a completed previous conversion and the SHA goes into the tracking mode, the user must allow a maximum of  $3\mu s$  acquisition time before the next falling edge of the C/S pulse can be submitted.

In the gain 100 and 500 modes, the settling time is long enough such that by the time the proper time has elapsed for settling, the SHA acquisition time will already be accounted for ( $t_{ACQ}$  and  $t_s$  are added “RMS”).

## AD369 TIMING DIAGRAM WITH PIPELINING



## NOISE CONSIDERATIONS

Assuming normally distributed or white noise, the rms noise voltage  $E_N$  of a system is a function of its noise bandwidth  $BW_N$ . The correlation between  $-3\text{dB}$  bandwidth ( $BW$ ) and  $BW_N$  is dependant upon the frequency response of the system under consideration.

For a  $6\text{dB/octave}$  (one-pole) filter, the ratio is  $\pi/2 = 1.57$ . For a “brick wall” filter, it is one. The noise correlation is  $E_N = e_n \sqrt{BW_N}$ , where  $e_n$  is the noise density ( $\text{nV}/\sqrt{\text{Hz}}$ ).

The noise of the input signal must also be added to the noise of the DAS. Again, in calculating the rms noise contribution of the signal, the  $BW_N$  of the source must be considered. If not filter limited before the AD369 input, the  $BW_N$  of the PGA must be used, which is about  $\pi/2$  times its  $-3\text{dB}$  bandwidth, assuming the one-pole roll-off.

Input protection resistors will also contribute to the total system noise. The rms noise voltage of a  $1\text{k}\Omega$  resistor over a noise bandwidth of  $1\text{Hz}$  is  $4\text{nV}$ . So, the noise voltage of a resistor,  $R(\text{k}\Omega)$  and a noise bandwidth,  $BW_N(\text{Hz})$  is:  $E_N(R) = 4\text{nV} \sqrt{R \times BW_N}$ .

The total system rms noise is given by the equation:

$$E_N(\text{system}) = \sqrt{E_N(\text{AD369})^2 + [G \times E_N(R_{\text{IN}})]^2 + [G \times E_N(\text{sig})]^2}$$

Once the system rms noise value is known, the probability of the peak-to-peak value of the noise exceeding an LSB is given to Table III.

### PROBABILITY OF NOISE EXCEEDING ONE LSB

LSB/ $E_N$	Probability
1.0	62.0%
2.0	32.0%
3.0	13.0%
4.0	4.6%
5.0	1.2%
5.15	1.0%
6.0	0.27%
6.6	0.10%

## ERRORS DUE TO SYSTEM BANDWIDTH LIMITATIONS

There will be applications in which the AD369 is used to digitize sinusoids. The overall bandwidth of the AD369 is limited by the input stage of the instrumentation amplifier. The  $3\text{-dB}$  bandwidth will vary according to which gain mode is chosen. In the  $G = 1$  mode, the DAS has a  $3\text{-dB}$  roll-off at  $1\text{MHz}$ . For  $G = 500$  operation, the value drops to  $40\text{kHz}$ .

A data acquisition system with 12 bits of resolution will incur errors in precision due to frequency response limitations well before the  $3\text{-dB}$  point. An extreme example is where an error of one LSB occurs. This frequency can be derived by using the equation of the absolute value of output to input voltage for the PGA:

$$|V_O/V_I| = G / [1 + jf/f_A] = G / [1 + (f/f_A)^2]^{.5},$$

where  $f_A$  is the  $3\text{-dB}$  point and  $f$  is the input frequency. The amplifier frequency response is assumed to be a single-pole roll-off. Substituting  $4095/4096$  ( $FS = 10\text{V}$ ) for  $V_O/V_I$  and solving for  $f(\text{LSB})$  yields:

$$f(\text{LSB}) = f_A/45.25$$

The PGA will have reached the limits of 12-bit precision for signal frequencies of  $f(\text{LSB})$ . The frequency can be doubled for every two bits of precision sacrificed:

$$f(3\text{LSBs}) = 2 * f_A/45.25, f(5\text{LSBs}) = 4 * f_A/45.25, \text{ etc.}$$

From a total system accuracy viewpoint, this degree of dynamic precision is usually not required. For example, one LSB of roll-off in a 12-bit system is  $-0.002\text{dB}$  from a full-scale input of  $10\text{V}$ . Nevertheless, the concept is valid and should be kept in mind when converting time-varying signals.

## "BUILD" VS. "BUY"

While it is clear that a system such as the one depicted earlier can be constructed from its individual components, the "build" vs. "buy" should consider the following trade-offs:

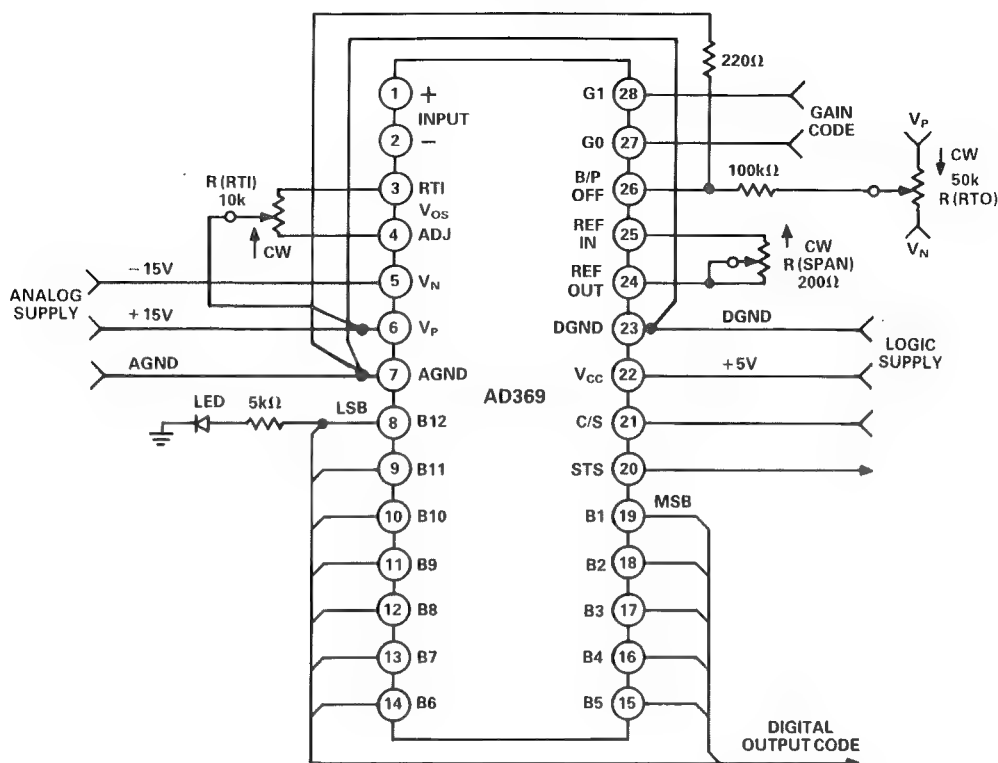
## "BUILD" VS. "BUY" FOR N-CHANNEL DAS

	"BUILD"	"BUY"
Cost Per Channel	Lower for $N < 3$	Lower for $N \geq 3$
Board Space Needed	Less for $N < 3$	Less for $N \geq 3$
Guaranteed Specs?	No	Yes
Layout Problems	Considerable	Few
Nonrecoverable		
Engineering Cost (NRE)	Higher	Lower

## APPLYING THE AD369

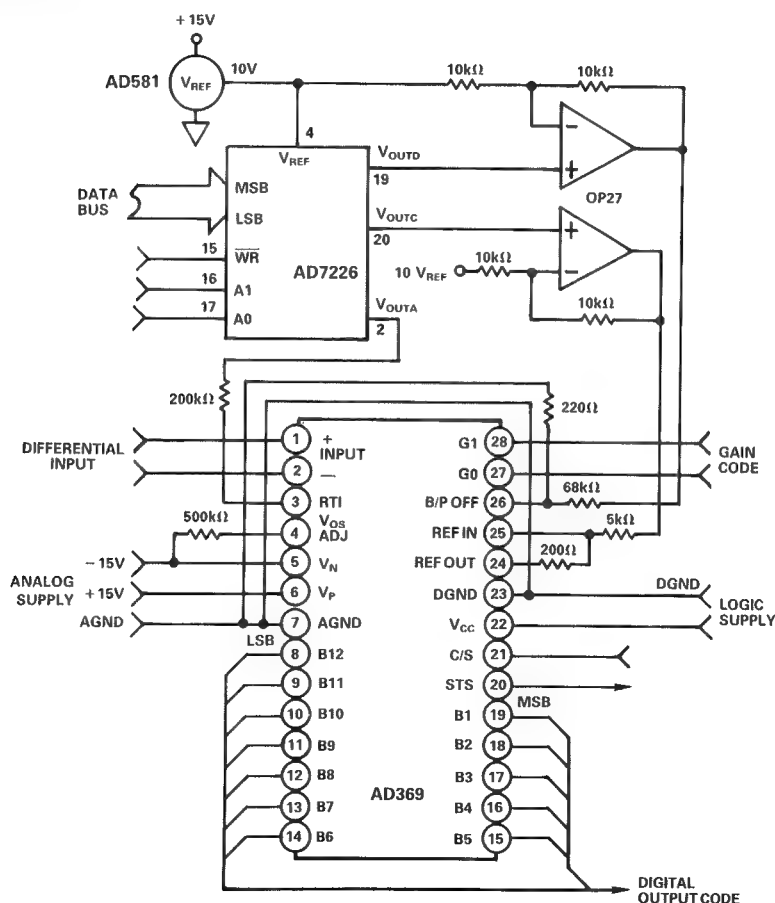
Although the AD369 may be trimmed for gain and offset with three potentiometers, this process may be automated. The three potentiometers are replaced with an AD7226 Quad 8-bit CMOS DAC using only three of the DACs. Using this system, the gain and offset error of the AD369 may now be corrected under digital control. Once the three 8-bit words are determined, they may be stored in memory for auto-calibration in the field. Temperature offsets may be cancelled by using an AD590. Temperature Transducer. The ambient temperature is measured and based upon this temperature, a microprocessor then addresses three locations in memory which hold the 8-bit word values for proper trimming.

## AD369 IN THE UNIPOLAR MODE WITH RTI $V_{OS}$ , RTO $V_{OS}$ AND SPAN TRIMPOTS



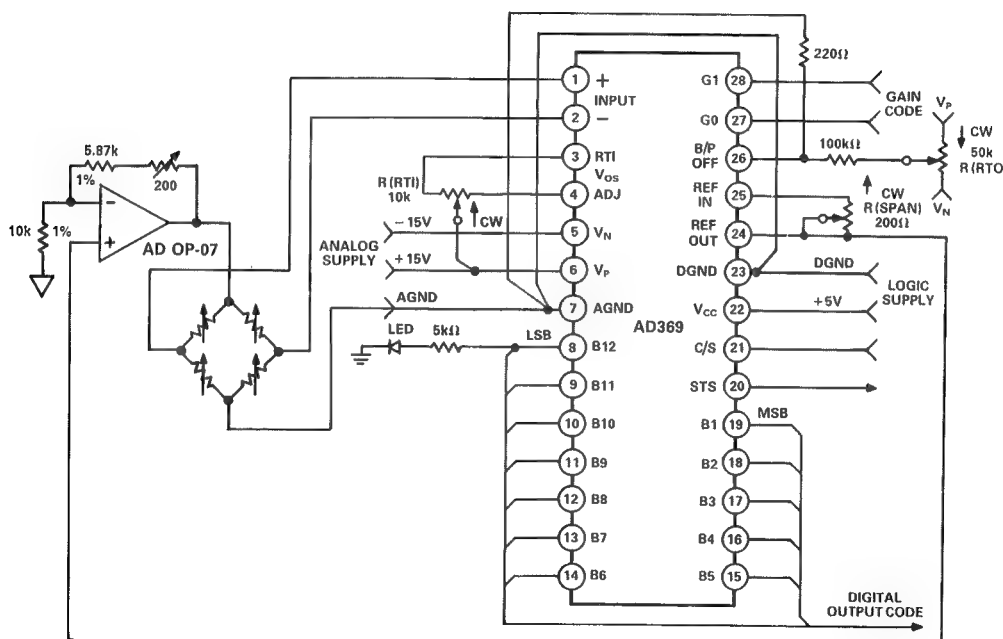


## AD369 IN THE UNIPOLAR MODE WITH D/A CIRCUIT REPLACING TRIMPOTS



The AD369 is easily interfaced to a load cell. In the circuit shown, the AD369 6.3V internal voltage reference is applied to a noninverting gain stage of 1.6 to deliver 10V across the load cell. The cell's output will be 20mV for a force of 10kg. With the AD369 set to gain of 500, the resolution will be 2.44 grams per LSB over the 10kg range.

## LOAD CELL INTERFACE TO AD369



## MULTIPLEXED ANALOG INPUTS TO AD369

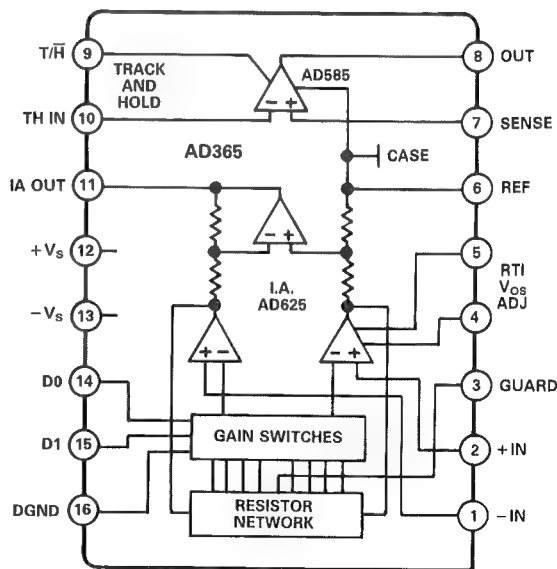
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In many systems the conversion time will dominate the throughput. The fast acquisition time of the AD365, when used with a high-speed A/D converter, allows accurate digitization of high-frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. The figures below show the use of an AD365 with the AD578 and AD574A.

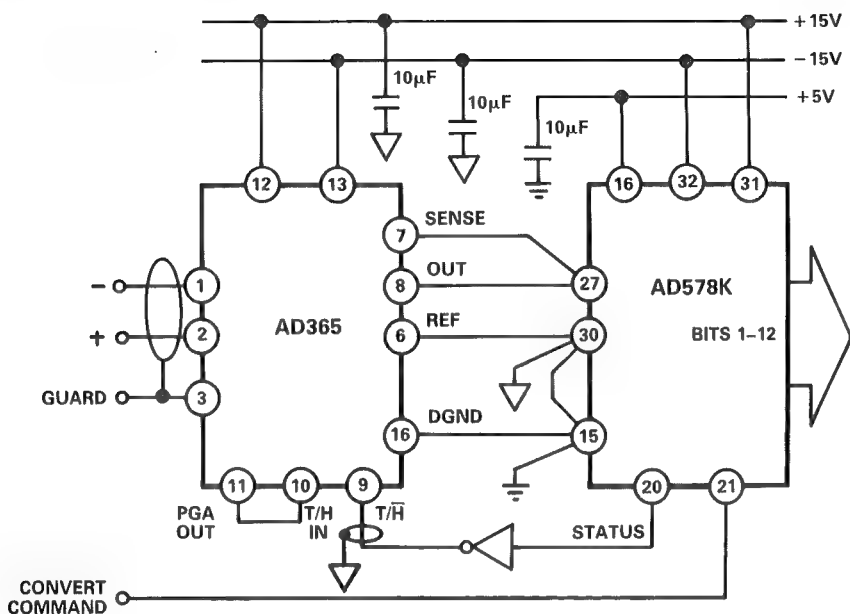
## AD365 FEATURES

**Software Programmable Gain (1, 10, 100, 500)**  
**Low Input Noise (0.2 $\mu$ V p-p)**  
**Low Gain Error (0.05% max)**  
**Low Nonlinearity (0.005% max)**  
**Low Gain Drift (10ppm/ $^{\circ}$ C max)**  
**Low Offset Drift (2 $\mu$ V/ $^{\circ}$ C RTI max)**  
**Fast Settling (15 $\mu$ s @ Gain 100)**  
**Small 16-Pin Metal DIP**

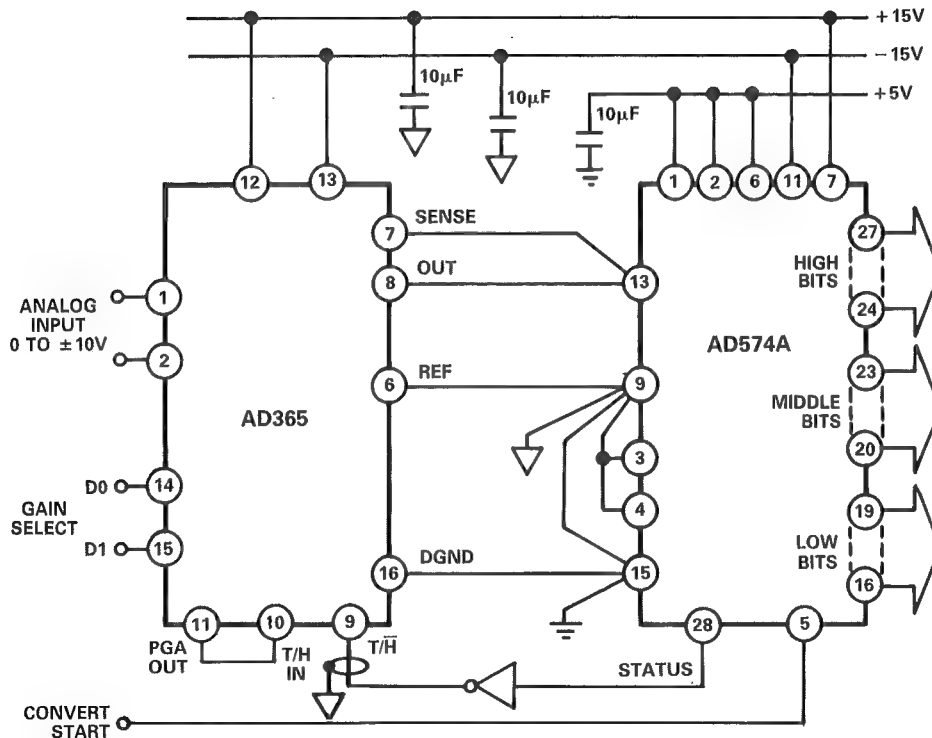
## AD365 FUNCTIONAL DIAGRAM



**A/D CONVERSION SYSTEM, 117.6kHz  
THROUGHPUT 58.8kHz MAX SIGNAL INPUT**



## 12-BIT A/D CONVERSION SYSTEM, 26.3kHz THROUGHPUT RATE, 13.1kHz MAX SIGNAL INPUT



### HIGH-RESOLUTION DATA ACQUISITION SYSTEM

Slow, time varying, low-level signals from pressure transducers and thermocouples often require a DAS with greater than 12 bits of resolution. Moreover, the wide dynamic range of output voltages from such sensors necessitates a programmable gain amplifier to drive the A/D converter. Using the dual slope integrating conversion technique, the AD367 provides a building block for any high-resolution system. Its input stage is programmed via a 6-bit digital code to accommodate an input range of 0.417 to 10V. The AD367 output is a pulse width whose duration is proportional to the input voltage and the gain selected. The active-low output pulse is used to gate a separate counter which accumulates pulses from a high-speed clock. This partition of the analog-to-digital conversion function into analog processing section and digital counting greatly reduces the potential for crosstalk between the noisy digital function and the low-level signal processing performed by the analog front end. This preserves the inherent rejection of high frequency normal mode noise that is a prime advantage of the dual slope conversion technique.

### AD367 FEATURES

- Differential Input – Programmable Gain Amplifier**
- 6 Bit (1 of 64) Gain Control**
- Internal – 10V Reference**
- 15 Bit Integral Nonlinearity**
- $\pm 305\mu V$  Resolution**
- 10ms Conversion Time**
- External Integration Capacitor**
- Programmable Conversion Time**

Conversion accuracy is independent of the length of the clock period and the integrating capacitance. Theoretical accuracy depends only on the absolute value of the reference and the stability of the clock. Even changes in other components such as the comparator input offset voltage have no effect as long as they do not change during a conversion. Differential nonlinearity is excellent since the technique is analog and inherently free from discontinuities.

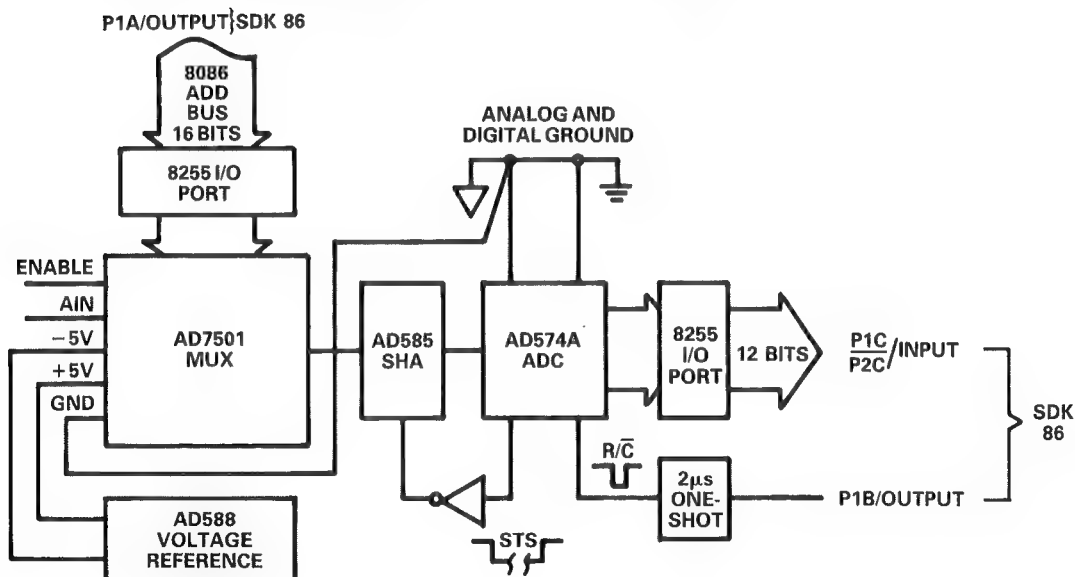
## SOFTWARE AUTO CALIBRATION

The Analog Devices monolithic high-precision voltage reference, AD588, just recently introduced into the marketplace, is already setting the standard for other references to follow boasting an initial untrimmed error of 1mV, a maximum guaranteed temperature drift coefficient of 1.5 parts per million per °C and offering industry's favorite voltages of  $\pm 5V$ . The AD588 does indeed offer a practical and economical solution to the question "Where do I get a precision 10V reference at a reasonable price?"

The AD588 at present has sufficiently stable and absolute attributes allowing it to be used as a system reference voltage. Additionally, the attractive price of the AD588 allows the device to be used in local applications such as an on-board reference for data acquisition systems.

Data acquisition systems are generally used to monitor a number of electrical signals whose voltage values represent a physical parameter such as temperature or pressure. The AD588, being a precision voltage reference, can be used as a measuring stick to gage the absolute value of the unknown voltage from which the precise temperature or pressure can be determined. The measurement and quantification of the unknown is achieved by comparing the difference between the reference signal and the unknown signal, and correcting the unknown signal based upon the measured value of the reference signal. This is accomplished effectively in microprocessor based systems and is known as autocalibration. In the data acquisition system, for example, numerous errors such as multiplexer signal path leakage, sample-to-hold offset voltage and the offset and gain error associated with the analog-to-digital converter can be compensated. The principle involved is simply to measure and preserve voltage values as a result of stimulating the system with a known, stable reference voltage, signal ground, and the voltage representing a parametric value. The preserved values represent the absolute values plus system errors, which can be factored out mathematically. This autocalibration technique is accomplished using the AD588 reference in conjunction with an Intel 8086 microprocessor based system. Attached is a flow chart and an assembly language program describing the sequence of events for the autocalibration of a data acquisition system.

# MICROPROCESSOR CONTROLLED DATA ACQUISITION SYSTEM WITH AUTO CAL



# AUTOCALIBRATION SOFTWARE ROUTINE FOR SDK-86

1571:0100	0100	FC	CLD	1571:016C	90	NOP	
1571:0101	BF0005	MOV	DI,0500	1571:016D	90	NOP	
1571:0104	B80400	MOV	AX,0004	1571:016E	A10405	MOV	AX,[0504]
1571:0107	A30003	MOV	[0300],AX	1571:0171	8B1E0006	MOV	BX,[0600]
1571:010A	B080	MOV	AL,80	1571:0175	2BC3	SUB	AX,BX
1571:010C	BAFFFF	MOV	DX,FFFF	1571:0177	7210	JB	0189
1571:010F	EE	OUT	DX,AL	1571:0179	A10605	MOV	AX,[0506]
1571:0110	BAF9FF	MOV	DX,FFF9	1571:017C	8B1E0406	MOV	BX,[0604]
1571:0113	A10003	MOV	AX,[0300]	1571:0180	2BC3	SUB	AX,BX
1571:0116	EE	OUT	DX,AL	1571:0182	A30805	MOV	[0508],AX
1571:0117	BAFBFF	MOV	DX,FFFB	1571:0185	90	NOP	
1571:011A	BOFF	MOV	AL,FF	1571:0186	90	NOP	
1571:011C	EE	OUT	DX,AL	1571:0187	EBOF	JMP	0198
1571:011D	F6D0	NOT	AL	1571:0189	90	NOP	
1571:011F	EE	OUT	DX,AL	1571:018A	90	NOP	
1571:0120	90	NOP		1571:018B	A10605	MOV	AX,[0506]
1571:0121	90	NOP		1571:018E	8B1E0406	MOV	BX,[0604]
1571:0122	90	NOP		1571:0192	03C3	ADD	AX,BX
1571:0123	B80900	MOV	AX,0009	1571:0194	A30805	MOV	[0508],AX
1571:0126	48	DEC	AX	1571:0197	90	NOP	
1571:0127	75FD	JNZ	0126	1571:0198	90	NOP	
1571:0129	B89B9B	MOV	AX,9B9B	1571:0199	90	NOP	
1571:012C	BAFEFF	MOV	DX,FFFE	1571:019A	90	NOP	
1571:012F	EF	OUT	DX,AX	1571:019B	90	NOP	
1571:0130	BAFCFF	MOV	DX,FFFC	1571:019C	A10005	MOV	AX,[0500]
1571:0133	ED	IN	AX,DX	1571:019F	8B1E0205	MOV	BX,[0502]
1571:0134	AB	STOSW		1571:01A3	2BC3	SUB	AX,BX
1571:0135	B80000	MOV	AX,0000	1571:01A5	A30606	MOV	[0606],AX
1571:0138	A10003	MOV	AX,[0300]	1571:01A8	A10805	MOV	AX,[0508]
1571:013B	48	DEC	AX	1571:01AB	8B1E0006	MOV	BX,[0600]
1571:013C	75C9	JNZ	0107	1571:01AF	F7E3	MUL	BX
1571:013E	90	NOP		1571:01B1	8B1E0606	MOV	BX,[0606]
1571:013F	90	NOP		1571:01B5	F7F3	DIV	BX
1571:0140	90	NOP		1571:01B7	A30806	MOV	[0608],AX
1571:0141	B80008	MOV	AX,0800	1571:01BA	92	XCHG	DX,AX
1571:0144	A30006	MOV	[0600],AX	1571:01BB	A31006	MOV	[0610],AX
1571:0147	F8	CLC		1571:01BE	B80200	MOV	AX,0002
1571:0148	A10405	MOV	AX,[0504]	1571:01C1	A31206	MOV	[0612],AX
1571:014B	8B1E0006	MOV	BX,[0600]	1571:01C4	B80100	MOV	AX,0001
1571:014F	2BC3	SUB	AX,BX	1571:01C7	A31406	MOV	[0614],AX
1571:0151	730A	JNB	015D	1571:01CA	BA0000	MOV	DX,0000
1571:0153	A10405	MOV	AX,[0504]	1571:01CD	A10606	MOV	AX,[0606]
1571:0156	8B1E0006	MOV	BX,[0600]	1571:01D0	8B1E1206	MOV	BX,[0612]
1571:015A	93	XCHG	BX,AX	1571:01D4	F7F3	DIV	BX
1571:015B	2BC3	SUB	AX,BX	1571:01D6	A31606	MOV	[0616],AX
1571:015D	90	NOP		1571:01D9	8B1E1006	MOV	BX,[0610]
1571:015E	A30406	MOV	[0604],AX	1571:01DD	F8	CLC	
1571:0161	90	NOP		1571:01DE	2BC3	SUB	AX,BX
1571:0162	F8	CLC		1571:01E0	730D	JNB	01EF
1571:0163	90	NOP		1571:01E2	8B1E0806	MOV	BX,[0608]
1571:0164	90	NOP		1571:01E6	A11406	MOV	AX,[0614]
1571:0165	90	NOP		1571:01E9	03C3	ADD	AX,BX
1571:0166	90	NOP		1571:01EB	A30806	MOV	[0608],AX
1571:0167	90	NOP		1571:01EE	90	NOP	
1571:0168	90	NOP		1571:01EF	90	NOP	
1571:0169	90	NOP		1571:01F0	90	NOP	
1571:016A	90	NOP		1571:01F1	F4	HLT	
1571:016B	90	NOP					

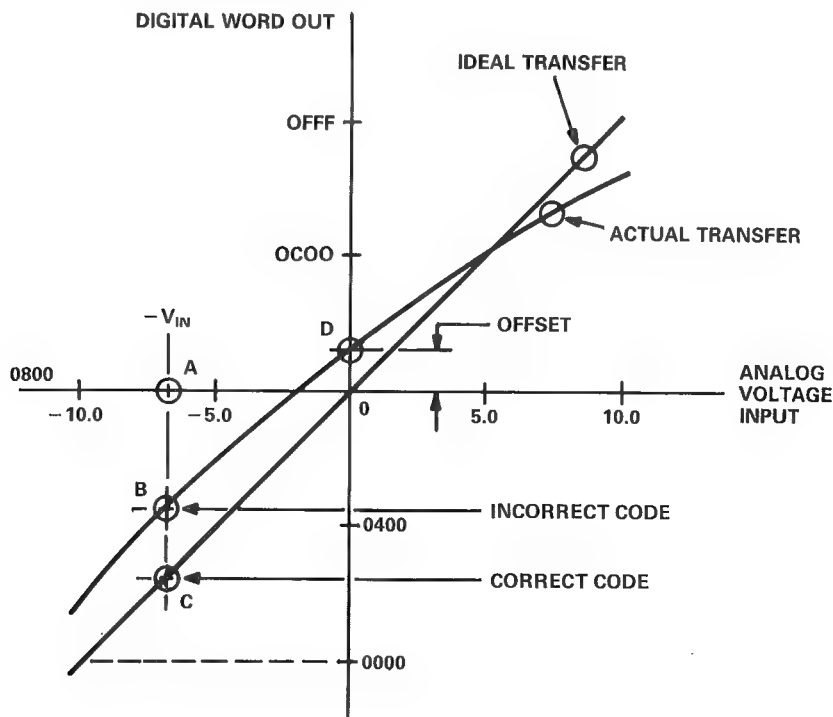
The autocal program is structured such that various memory locations are used for analog inputs, temporary storage resulting from in-programming computations, constants, and the final result. Below is a table to describe the memory locations' contents.

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Prior to elaborating on the software per se, it is instructive to review the figure below describing graphically the concept of analog-to-digital conversion. Note the ideal transfer curve passes through the origin and is without offset. This ideal transfer curve may be considered mathematically as a straight line curve of the form  $Y = mX + b$  where the slope "m" is unity and the "Y" intercept "b" is zero as the curve passes through the origin and hence must be zero. The slope of the ideal transfer curve being one demands that the digital output word have a one-to-one correspondence with the input analog value. The actual transfer curve, however, is indeed different from the ideal. Considering the actual transfer curve with respect to the  $Y = mX + b$  analogy, it is obvious the slope "m" is not unity or even constant but is nonlinear, and the "Y" intercept is not zero but some value called "offset". Further note that the set up is for an output in offset binary to accommodate negative input voltages. Point A represents a minus input voltage. The corresponding digital code is represented by point C. Point B represents an incorrect output code. The purpose of the autocalibration technique is to correct for the deficiencies of the actual curve (Point B), and make the system respond as if it were ideal (Point B).

## ADC TRANSFER FUNCTION



The autocal program is written in five individual sections described briefly as follows: this sectioning of the autocal program was done to assist in debugging.

### Section One

This section moves data into RAM; the programming is established for a minimum configuration and samples +5V (reference), -5V (reference), analog ground, and the analog signal of interest by defining the I/O ports, selecting appropriate MUX channels, starting conversions, and reading data.

### Section Two

Section two computes the magnitude of the offset, delta, which is the difference between the digital output code for 0V input and the ideal digital code for a 0V input. The ideal condition would be to have offset equal to zero.

### Section Three

Section three describes initial phases of signal correction and corrects the analog input signal by subtracting the offset error term. It should be pointed out that the corrections are done through math manipulations and not through fancy analog circuit tricks.

## Section Four

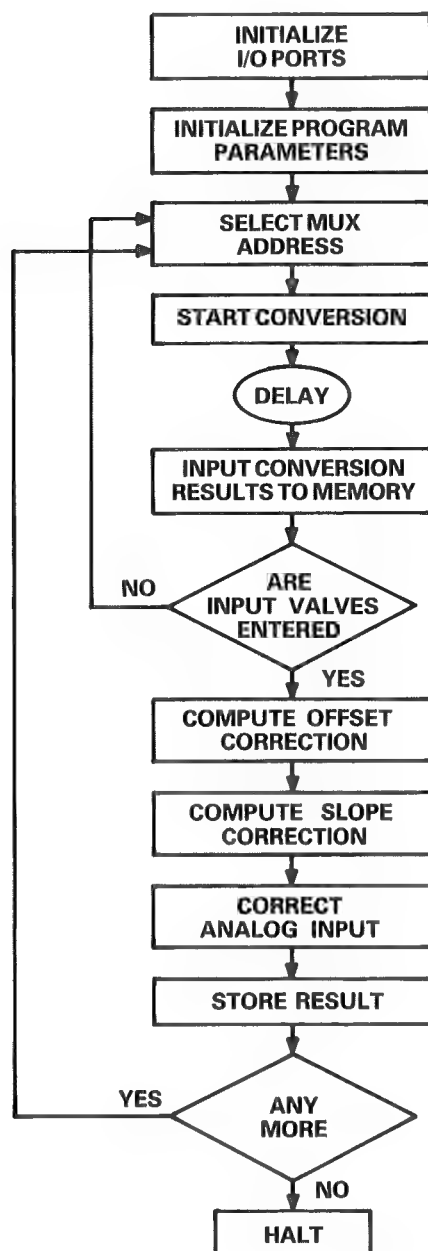
Section four computes the slope of the data acquisition system, and applies a slope correction factor to the offset corrected signal. The ideal slope is one and simply means the digital output word has a one-to-one relationship with the analog input signal. The slope correction factor is the inverse of the actual transfer slope. The actual transfer slope is calculated by first finding the difference between the digital codes corresponding to +5V (reference) and -5V (reference), and dividing this difference by the ideal code corresponding to ten.

## Section Five

Since part of this routine requires mathematical division a rounding error exists, and this fifth part of the program modifies the result to account for any rounding error.

## Results

The results were encouraging. Not only did the autocal technique eliminate the need for trimming the AD574ASD to achieve  $\pm 1\text{LSB}$  performance, the autocal technique also maintained 1LSB performance as the AD574ASD's temperature was varied between  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$ .



# HIGH-PERFORMANCE A/D CONVERTERS

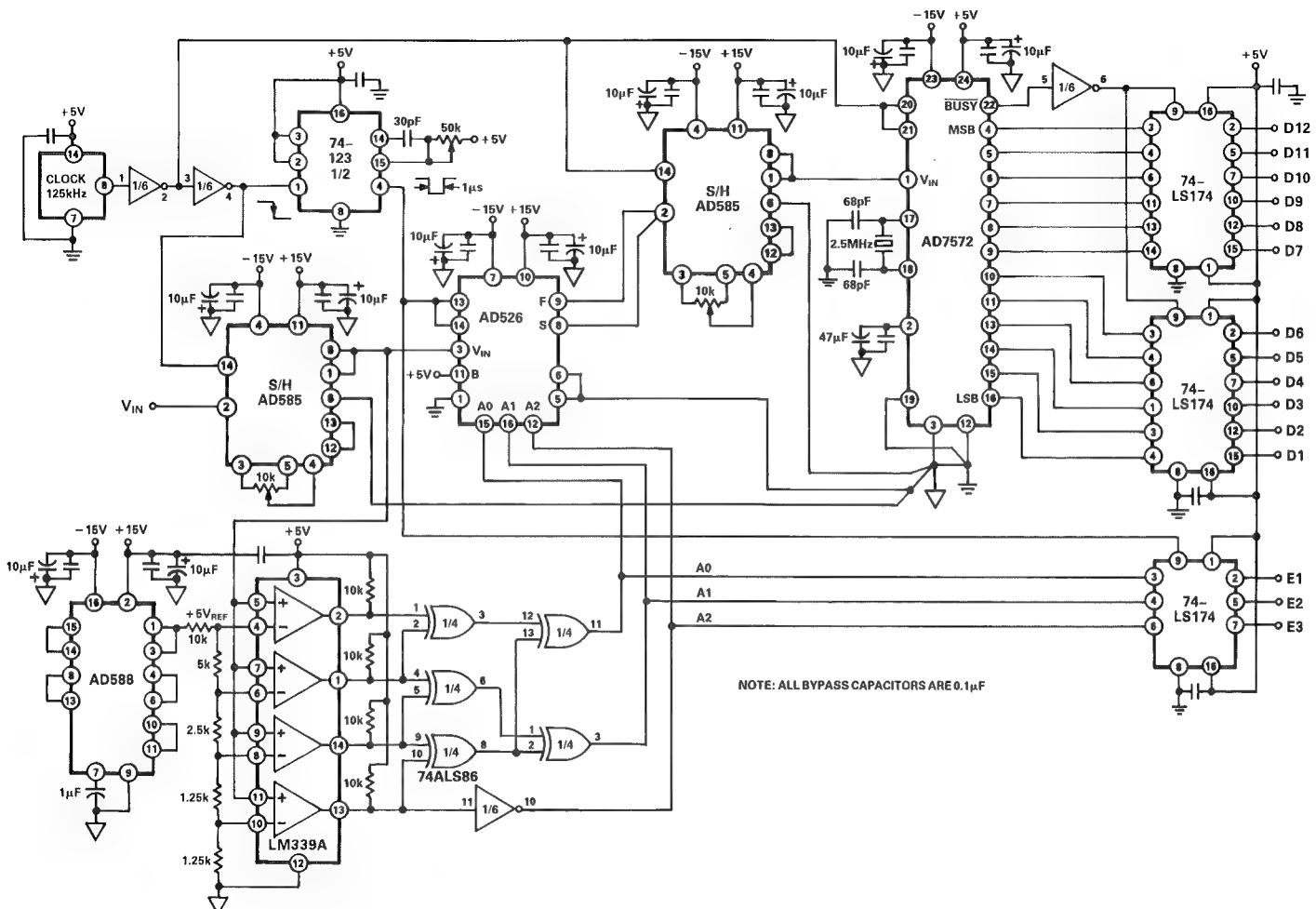
## FLOATING POINT CONVERSION

High-resolution converters are used in systems to obtain high accuracy, improve the system resolution, or increase the dynamic range. There are a number of high-resolution converters available in the market with a throughput rate of 66.6kHz that can be purchased as a single component. However, in order to achieve higher throughput rates, alternative conversion techniques must be employed. A floating point A/D converter improves both the throughput rate and the dynamic range of a system by utilizing a low resolution, high-speed A/D converter, and acquiring data in two parts. In a floating point A/D converter the output data is presented as a 16-bit word, the lower 12 bits from the A/D form the mantissa and the upper 4 bits from the digital signal used to set the gain form the exponent. In the figure, an AD526 programmable gain amplifier, in conjunction with the comparator circuit, scales the input signal to a range between half scale and full scale for the maximum usable resolution.

The dynamic range of a converter is the ratio of the full-scale input range to the smallest signal the converter can detect which is the LSB value. With a floating point A/D converter, the smallest value of the LSB corresponds to the value of the LSB of the converter when the PGA is programmed for its highest gain. The floating point A/D converter has a full-scale range of 5V, a maximum gain of 16V/V from the AD526 and a 12-bit A/D converter, this corresponds to:  $LSB = FSR / (GAIN * 2^N)$ ,  $LSB = (5V / [16 * 4096])$  OR  $76\mu V$ . The dynamic range in dBs is based on the log of the product of the amplifier gain and the converter's dynamic range. In the figure, the dynamic range is 96dB ( $20 \text{ LOG } [2^{12} * 2^4]$ ).

The floating point A/D converter achieves its high throughput rate of 125kHz by overlapping the acquisition time of the first sample/hold amplifier and settling time of the AD526 with the conversion time of the A/D converter. This conversion technique relies on the fast-settling characteristics of the AD526 after the flash autoranging (comparator) circuit quantizes the input signal. The 16-bit ( $LSB = 1$  part in 65536) converter diagrammed in the figure consists of a pair of sample/hold amplifiers (the AD585s), flash converter, a five-range programmable gain amplifier (the AD526), and a fast 12-bit A/D converter (the AD7572). The first sample/hold

## FLOATING POINT ADC 125kHz SAMPLE RATE



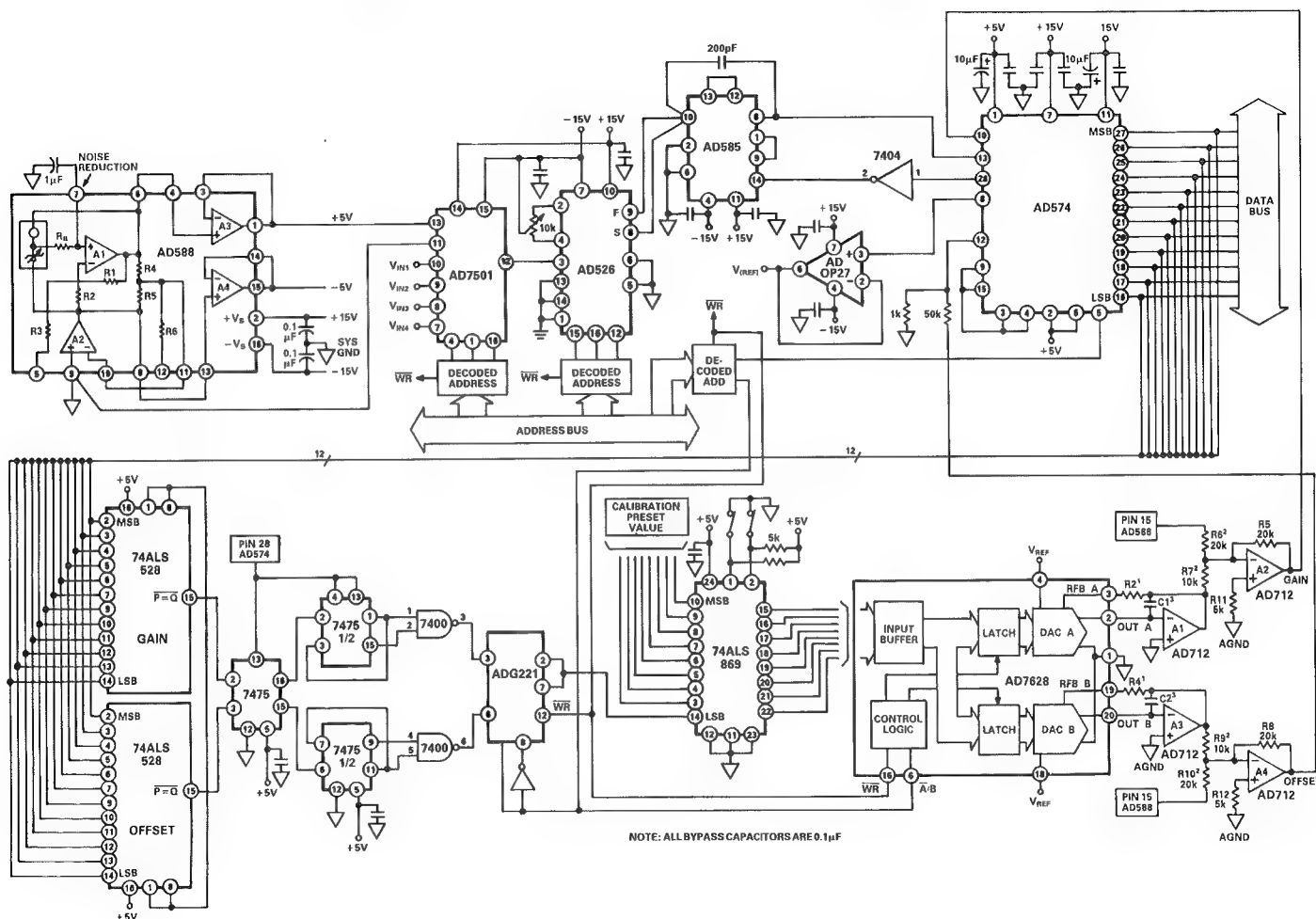
amplifier holds the signal for the flash autoranger, which determines which binary quantum the input falls within, relative to full scale. Once the AD526 has settled to the appropriate level then the second sample/hold amplifier can be put into hold which holds the amplified signal while the AD7572 performs its conversion routine. The acquisition time for the AD585 is 3 $\mu$ s and the conversion time for the AD7572 is 5 $\mu$ s for a total of 8 $\mu$ s or 125kHz. A 16-bit register holds the 3-bit output from the flash autoranger and the 12-bit output of the AD7572.

## HIGH-ACCURACY A/D CONVERTERS

Very high-accuracy and high resolution floating point A/D converters can be achieved by the incorporation of offset and gain calibration routines. There are two techniques commonly used for calibration, a hardware circuit as shown in the figure and/or a software routine. In this application, the microprocessor is functioning as the autoranging circuit, requiring software overhead. Therefore, a hardware calibration technique was applied which reduces the software burden. In this floating point design the software is used to set the gain of the AD526, requiring multiple conversions from the AD574. In operation, the signal is converted, and if the MSB is not equal to a logical 1, the gain is increased by a number of binary steps, up to the maximum gain. This maximizes the full-scale range of the conversion process and insures a wide dynamic range.

The calibration technique uses two point correction, offset and gain. The hardware is simplified by the use of programmable magnitude comparators the 74ALS528, an 74ALS528 can be "burned" for particular code. The 74ALS528 will then produce a low going pulse when the conversion result and the programmed code are equal. In order to prevent under or over range hunting during the calibration process, the equivalent offset and gain codes are different from the endpoint codes. A calibration cycle consists of selecting whether offset or gain is to be calibrated, then selecting the appropriate multiplexer channel to apply the reference voltage to the signal channel. Once the operation has been initiated, the counter, a 74ALS869, drives the D/A converter in a linear fashion, providing a small correction voltage to either the gain or offset trim points. The output of the A/D converter is then compared to the value preset in the 74ALS528 to determine a match. Once a match is detected then the counter is stopped and the code at the D/A converter is latched until the next calibration cycle. Calibration cycles are under the control of the microprocessor in this application and should be implemented only during periods of converter inactivity.

## HIGH-ACCURACY A/D CONVERTER





# **MICROPROCESSOR INTERFACE**



## INTERFACING TO MICROPROCESSORS

Very often, digital information must be exchanged between a data acquisition component and a microprocessor. A fast-growing application area is the microprocessor-based measurement and control system. Let's examine a generalized system to illustrate the interface of a digital-to-analog or analog-to-digital converter to a processor. Afterwards, we will explore some specific interfaces to some of the more popular microprocessors.

The central processing unit is the heart of the system. It requests instructions prepared by the programmer, calls for data, and makes decisions related to the instructions. Based on the data, the processor then determines appropriate actions to be performed by other parts of the system. Since there are many peripherals within a given system, the microprocessor must be capable of selecting a particular device. It identifies each device by means of a unique address code. A typical microprocessor might have 16 binary address lines providing 65,536 addressing codes. Data to and from the processor is carried across a bidirectional 8 or 16 bit wide data bus. Many processors also provide a serial data path. Several microprocessors use a multiplexed address/data bus on which both address and data are transmitted on the same signal paths. In this case, the first portion of the bus cycle transmits the address. Data transfer occurs later in the cycle. This architecture is popular for microprocessors with an 8-bit data bus.

All microprocessors have memory which is usually external. Digital signal processors often have some internal memory to complement external memory. The memory is used by the CPU as its primary source of instructions and also as a means to store information generated for later use. Many of the address locations in a typical system are storage locations in the memory. When a memory location is addressed, the memory may store the information that resides on the data bus. This is called MEMORY WRITE. Addressing stored information to be placed on the data bus for use by the CPU constitutes a MEMORY READ. In addition, the microprocessor provides the system with control information. The control bus issues read or write command signals and indicates a valid address.

Another important link in the system is the set of Input-Output (I/O) interfaces. These interfaces include all the information channels between the system and the real world. There are digital ports through which programs and control commands may be loaded and from which digital data may be transmitted. Many systems also use analog signal ports to measure and control external real-world phenomena.

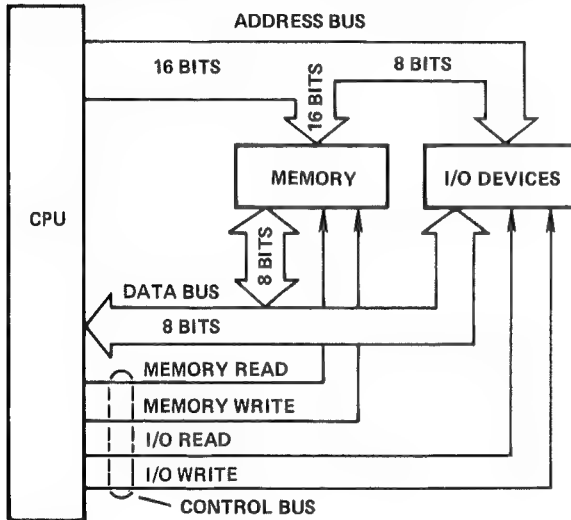
Digital I/O may be interfaced to the processor by means of one or more of the following three techniques:

- Accumulator or Isolated I/O
- Memory Mapped I/O
- Direct Memory Access

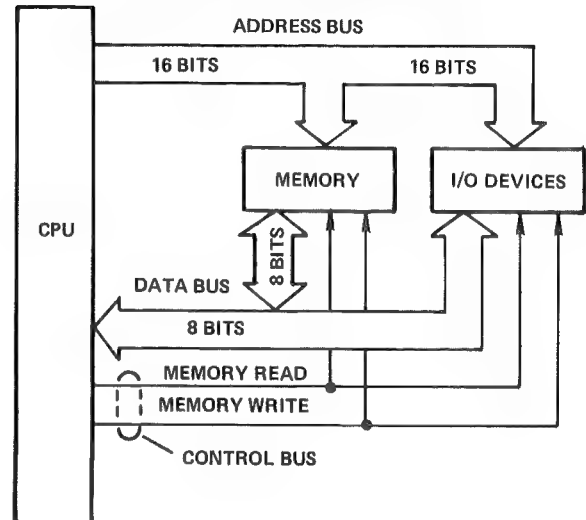


## ACCUMULATOR I/O

### ACCUMULATOR OR ISOLATED I/O



### MEMORY-MAPPED I/O



## ACCUMULATOR I/O

Accumulator I/O simplifies address decoding. Separate control signals isolate all I/O addresses from memory addresses. In 8085 and Z80 systems, only 256 input and output addresses are available. This 8-bit addressing for I/O increases program execution speed and simplifies programming. Isolated I/O allows flexibility in system hardware design. The system designer has the ability to combine different I/O devices within the I/O space regardless of their speed. Slower I/O will require Wait States which extend the bus cycle thus slowing throughput. The processor extends the current bus cycle until the I/O device issues a READY or DTACK indicating that the cycle should be terminated. Since isolated I/O must pass all data through the accumulator, programming flexibility is limited.

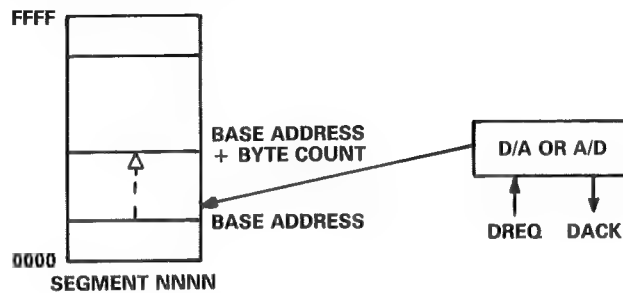
## MEMORY MAPPED I/O

For memory mapped I/O, each input or output function is treated as a location of memory. Full decoding of all address bus signals provides more I/O capability at the expense of address decode complexity. Memory mapped I/O can transfer data without the use of the accumulator thus facilitating ease of programming.

## DIRECT MEMORY ACCESS

Direct memory access (DMA) is the fastest method for data transfer. Throughputs of 360kbytes/sec are achievable for many microprocessors using DMA. The DMA controller must know where in memory the data from the requesting device is to be stored. This is referred to as the "Base Address". In addition the "Byte or Word Count" or number of items to be stored must be known. Each time the controller processes a DMA request, it "robs" a bus cycle from the processor, issues the appropriate address to memory, and sends an acknowledge signal to the requesting device. The requesting device now can gate its data onto the processor's data bus. The controller will then increment the base address and decrement the byte or word count awaiting the next DMA operation. No software interaction is required permitting the processor to perform other tasks. In DMA operation, only sequential groups of data may be transferred per DMA channel. Many controllers can, however, accommodate several DMA channels. In the case of converter interfacing using DMA, the converter usually represents a single byte or word being transferred to or from a block of memory.

## DEVICE-TO-MEMORY DMA MEMORY DIAGRAM



1-BYTE SOURCE TO N-BYTE DESTINATION

## GENERAL CONSIDERATIONS FOR INTERFACING

Several key parameters must be determined to successfully interface a D/A or A/D converter to a microprocessor. Power supply requirements, logic compatibility, timing parameters, support hardware, and data formats all need careful consideration. Let's explore some of these issues in greater detail.

## GENERAL INTERFACE CONSIDERATIONS

- Power Supply Requirements
- Logic Compatibility
- Timing
- Hardware
- Data Formats

### POWER SUPPLY REQUIREMENTS

With the increasing popularity of the personal computer, it seems natural that they have become a prime candidate to host a data acquisition system. The majority of these computers provide  $\pm 12$  Volt power supplies to support RS-232 interfaces and may be used to power low current external devices. Many older data acquisition products, however, are not capable of operation with supplies less than  $\pm 15$  Volt  $\pm 5\%$  and some may also require a  $+5$  Volt source. Today however, manufacturers have addressed this problem with products that are specified and tested with both 12 and 15 Volt supplies. Moreover, some newly developed monolithic products are capable of single supply operation at  $+12$  or  $+5$  Volts. In either case, to achieve optimal performance, proper grounding and decoupling in conjunction with good PC board layout should be incorporated. Quite often, a switching type supply will generate substantial electromagnetic interference to degrade accuracy of the data acquisition system. The user should refer to publications dealing with shielding techniques to alleviate this problem.

## POWER SUPPLY REQUIREMENTS

- Dual Supply Operation
- Single Supply Operation
- Low Noise

## LOGIC COMPATIBILITY

Today's microprocessor compatible data conversion products require 5 Volt TTL digital inputs. A logic level high is guaranteed 2.4V minimum with a logic level low at 0.8V max. Some older CMOS D/A converters such as the AD7523 and AD7524 have different logic levels for each specified power supply voltage. The AD7524, for example, when powered by a 5V supply, will have TTL compatible inputs. When powered by a +15V supply, the logic levels will shift to +13.5V minimum and 1.5V maximum for logic high and logic low respectfully. In any system, the designer should ensure that the digital logic has adequate output drive to meet the needs of the converter.

## LOGIC COMPATIBILITY

- 5 Volt TTL or CMOS
- Logic Levels as a Function of Supply Voltage
- Low Digital Input Currents

## TIMING PARAMETERS

Special attention to timing parameters during the design stage of a data acquisition system will limit problems during the production phase. Control signal pulse widths, set-up times, and hold times should conform with timing specifications for the device. Avoid designing to "typical specifications" as these parameters could vary from device to device. If operation over a wide temperature range is expected, shifts in timing may occur. Some CMOS D/A converters will exhibit power supply dependent timing specifications. These devices will generally have faster timing specifications with  $V_{DD}$  at 15 Volts as compared to 5 Volts. In some applications, all control inputs to data acquisition component may not be used. Unused inputs should be hardwired high or low per the device specification.

## TIMING PARAMETERS

- Avoid Designing to Typical Specifications
- Analyze Temperature Effects
- Analyze Power Supply Voltage Effects
- Terminate Unused Digital Inputs

## SUPPORT HARDWARE

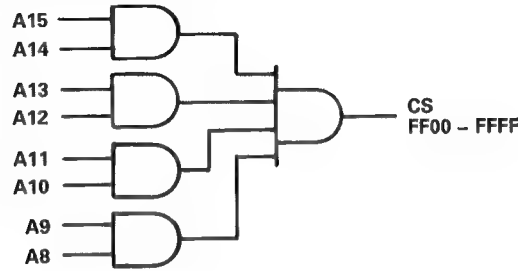
In order to interface a D/A or A/D converter to a processor, additional hardware is usually required. External logic may be used to condition the digital control signals from the processor. Microprocessor compatible D/A converters incorporate on-board data latches. A/D converters with microprocessor compatibility also include these latches with three-state outputs.

## SUPPORT HARDWARE

- Address Decoding

The amount of external hardware for address decoding is determined by the I/O technique employed and the number of peripherals in the system. Memory mapped I/O will require more address decode logic than accumulator I/O since all address signals must be decoded. A simple approach for Memory Mapped I/O would be decoding of only the upper 8 address lines of a 16-bit address bus. If, for example, the upper 8 address lines are gated as shown below, any one of 256 addresses from FF00H through FFFFH will decode. The disadvantage is that one peripheral occupies 256 memory locations wasting 255 which could be used for other functions. The same decode logic used with an 8086 or 8088 microprocessor will accommodate accumulator I/O when the upper 8 address lines are replaced by their lower counterparts. These processors can address any one of 256 port locations through the direct I/O instruction and can be interfaced to peripherals using the I/O, read and write control signals. Many other possibilities exist and depend upon available hardware, board space, and system architecture.

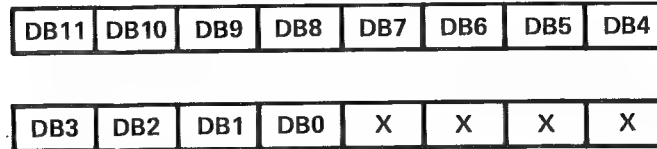
## DECODE LOGIC FOR UPPER 8 ADDRESS LINES OF 16-BIT BUS



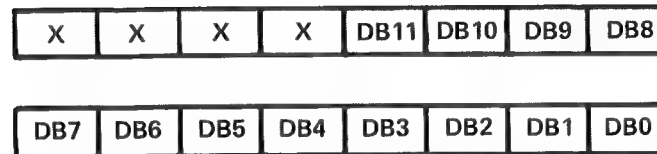
## DATA FORMATS

The vast majority of today's microprocessors incorporate either an 8- or 16-bit data bus. An 8-bit peripheral such as a D/A or A/D converter connects directly to an 8-bit bus; however, higher resolution devices require some form of data formatting. A 12-bit D/A connected to an 8-bit bus must have a double-buffered input structure. Two input registers are loaded; the first with the 8 MSBs and the second with the 4 LSBs. The contents of these registers are then loaded into the DAC register at which time the analog output updates. The entire transfer is accomplished in two write operations. The format for the 12 bits of data may be left or right justified. Left justification places the MSB (DB7) at the MSB position of the first address with the LSB (DB0) appearing as DB4 for the next address. Right justification places the MSB on DB3 of the first address with the LSB appearing as the LSB (DB0) of the next address. Some CMOS D/A converters, such as the AD7548, allow the flexibility of either left or right justification via TTL control. Others, such as the AD667, offer this flexibility through pin-strapping. Interfacing a data acquisition device with resolution less than 16 bits to a 16-bit data bus also requires the designer to select a format. The device is wired to the processor's bus for either left or right justification.

### LEFT JUSTIFIED



### RIGHT JUSTIFIED



A serial data format provides a convenient means of data transmission over long distances. In large systems, a serial data format can often simplify backplane wiring and allow more signals to be passed over the bus. Moreover, serial data acquisition devices have smaller package outlines permitting a higher circuit density. All serial devices require a clock to strobe the data. The CMOS AD7543 12-bit DAC, packaged in a 16-pin DIP, uses an external clock whereas the AD575 10-bit A/D operates from an internal or external clock.

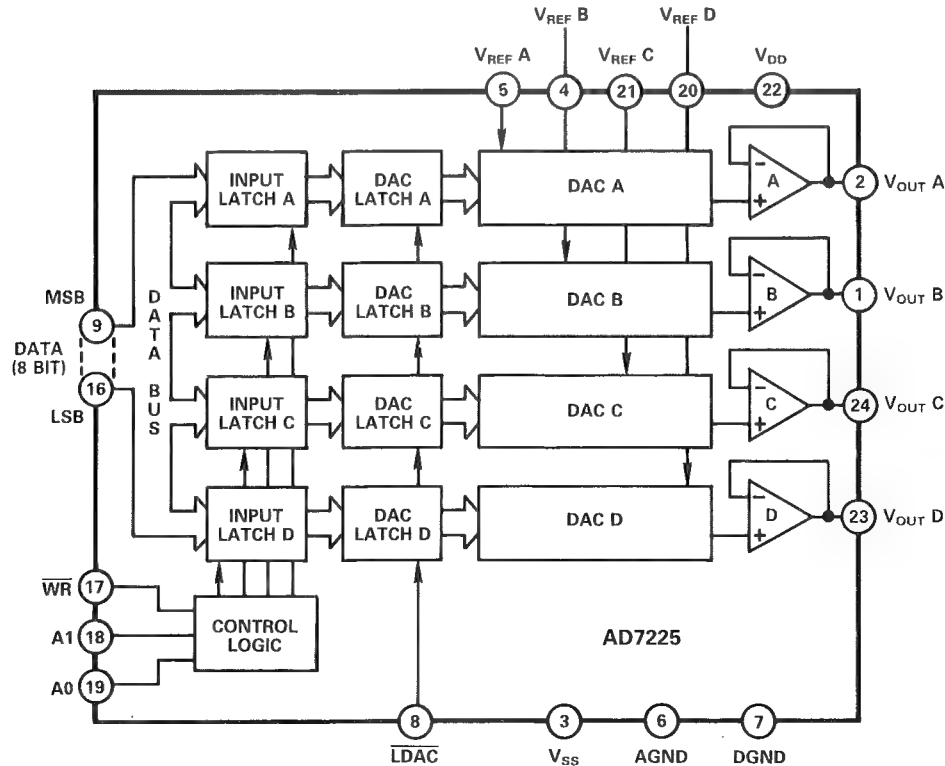
## INTERFACING A DIGITAL-TO-ANALOG CONVERTER

Digital-to-analog converters are easily interfaced to microprocessors. Address decoding and some external logic are all that is required to successfully interface the device. Some examples follow to illustrate this point.

### 8-BIT DATA BUS INTERFACING

#### AD7225 LC<sup>2</sup>MOS Quad 8-Bit DAC with Separate References

### AD7225 FUNCTIONAL BLOCK DIAGRAM



The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the data bus. When the  $\overline{WR}$  is LOW the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of  $\overline{WR}$ .

The data held in the DAC register determines the analog output of the converter. The rising edge of  $\overline{LDAC}$  controls data transfer from input register to DAC register for all four DACs. The  $\overline{LDAC}$  signal is level triggered and therefore the DAC registers may be made transparent by tying  $\overline{LDAC}$  LOW.  $\overline{LDAC}$  is an asynchronous signal independent of  $\overline{WR}$  but proper hold time for  $\overline{LDAC}$  must be given to latch the correct data.

Interfacing the AD7225 to an 8085 or 8088 microprocessor is easily accomplished. These processors employ a multiplexed address/data bus. An external latch such as the 8282 latches the lower address byte on the falling edge of ALE. The upper address byte is valid the entire bus cycle and is also decoded with the lower address byte to configure the AD7225 as memory mapped I/O. A0 and A1 connect directly to the DAC to select one of four input registers to be loaded. The high speed digital interface of the AD7225 is compatible with 8MHz processors.

8085A/  
8088

A15

A8

WR

ALE

AD7

AD0

ADDRESS DECODE

LATCH

EN

ADDRESS BUS

AD7225\*

A0

A1

LDAC

WR

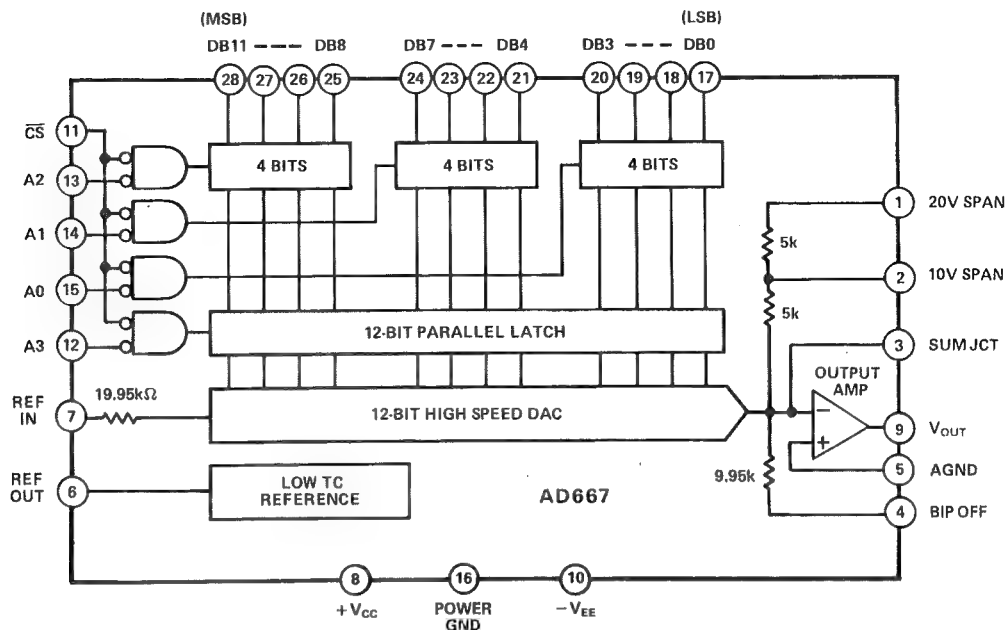
DB7

DB0

ADDRESS/DATA BUS

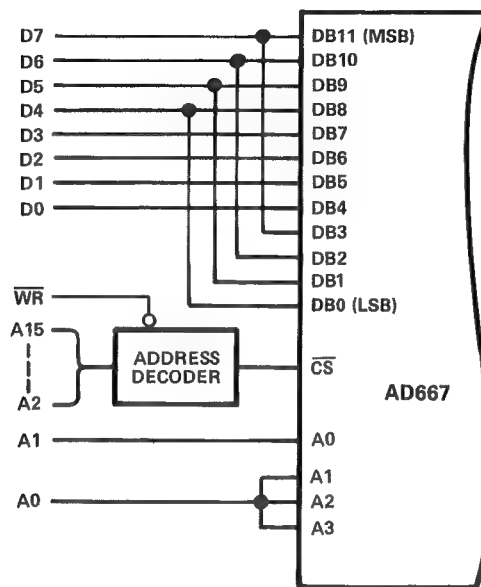
\*LINEAR CIRCUITRY OMITTED FOR CLARITY

## AD667 FUNCTIONAL BLOCK DIAGRAM



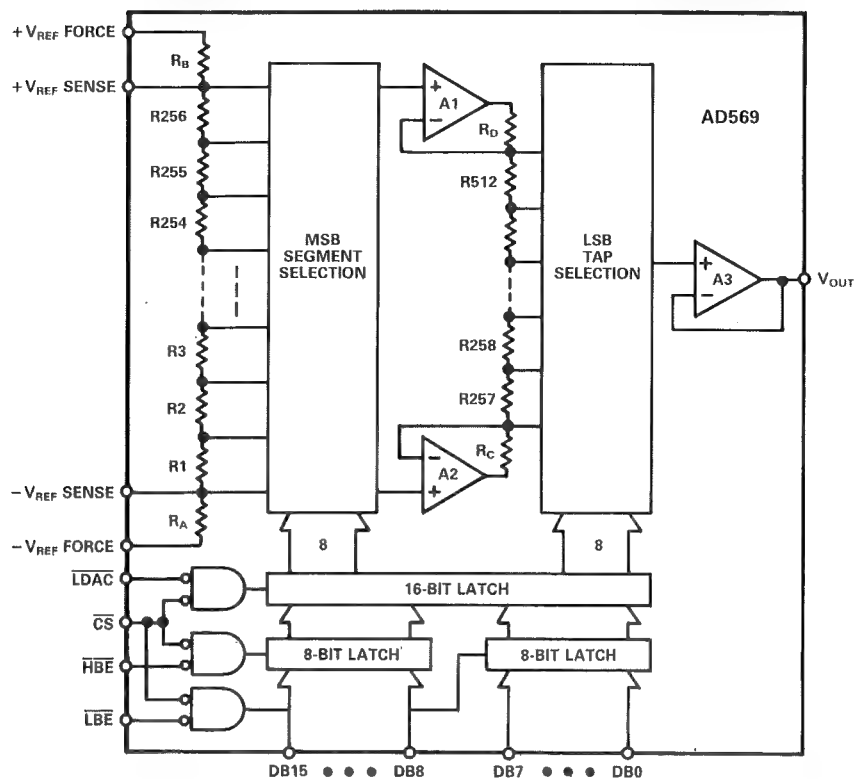
VIII - 7

## LEFT-JUSTIFIED 8-BIT BUS INTERFACE



## AD569 16-Bit Microprocessor Compatible D/A Converter

### AD569 FUNCTIONAL BLOCK DIAGRAM



Instrumentation and process control systems often require high resolution converters (>12 bits) to be interfaced directly to a computer. In many instances a personal computer with an 8-bit data bus such as the IBM PC will serve as the controller. Unless the converter is specifically designed to accommodate this narrow bus external hardware will be required. Obviously one solution is to select a converter such as the AD569 with a double buffered input structure. Two write cycles are required to load (in any sequence) the high byte and low byte input registers and to update the DAC register. In addition the high speed control inputs of the AD569 permit operation with today's high speed processors.

## AD569 8-BIT BUS INTERFACE



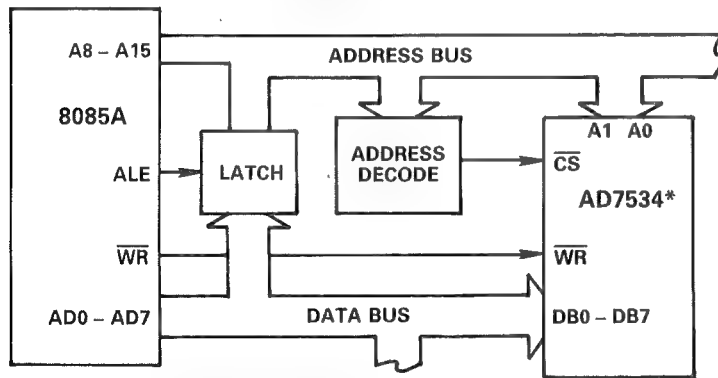


The AD7534 14-bit D/A converter is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard chip select and memory write logic is used to access the converter. Address lines A0 and A1 control the internal register loading and transfer.

A typical interface circuit for the AD7534 and the 8085A microprocessor is given below. The microprocessor treats the converter as four memory locations being selected by address lines A0 and A1. A sample program for loading the D/A with a 14-bit word is shown. The converter resides at locations 3000 through 3003.

The six MSBs are written into location 3001, and the eight LSBs are written to 3002. A write instruction to 3003 loads the full 14-bit word to the DAC register and updates the analog output.

## AD7534 – 8085A INTERFACE



\*LINEAR CIRCUITRY  
OMITTED FOR CLARITY

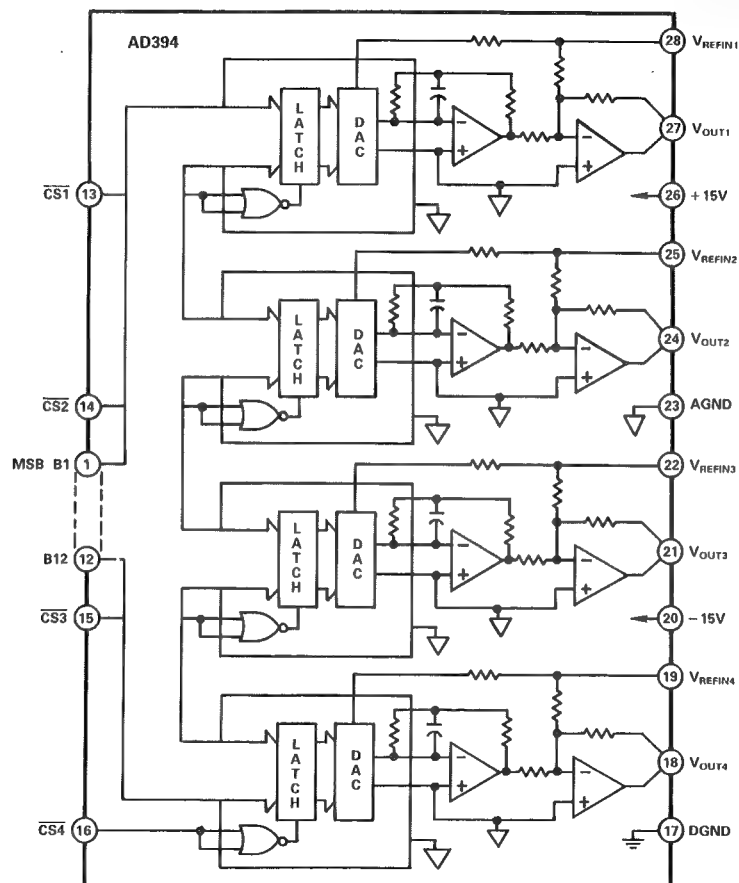
## PROGRAM LISTING FOR AD7534 – 8085A INTERFACE

Address	Op-Code	Mnemonic
2000	26	MVIH, # 30
01	30	
02	2E	MVIL, # 01
03	01	
04	3E	MVIA, # "MS"
05	"MS"	
06	77	MOV M, A
07	2C	INR L
08	3E	MVIA, # "LS"
09	"LS"	
0A	77	MOV M, A
0B	2C	INR L
0C	77	MOV M, A
200D	CF	RSTI

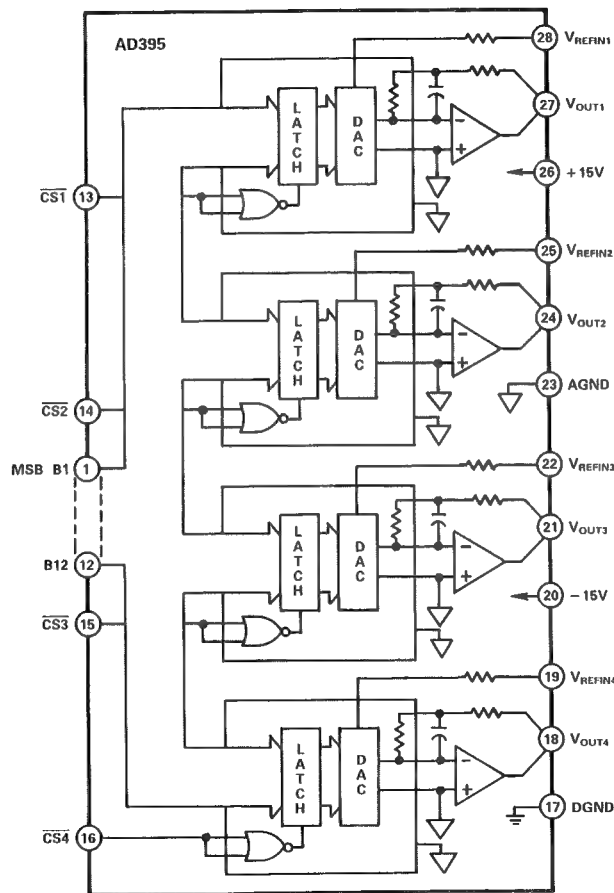
## 16-BIT DATA BUS INTERFACING

### AD394/395 Quad 12-Bit D/A Converter

## AD394 (BIPOLAR) FUNCTIONAL BLOCK DIAGRAM



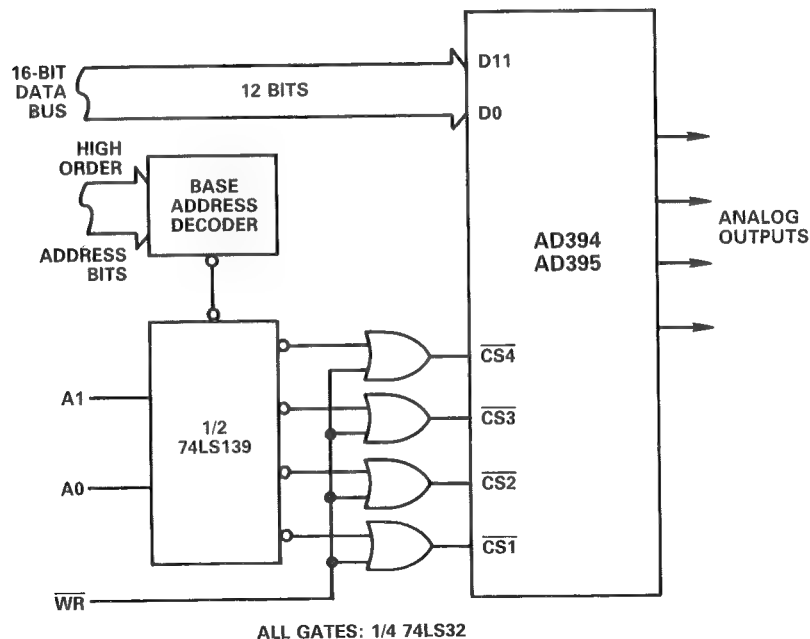
## AD395 (UNIPOLAR) FUNCTIONAL BLOCK DIAGRAM



The AD394/395 quad 12-bit D/A converters are easily interfaced to 16-bit wide data buses. The devices' individual latches allow for multi-DAC interfacing to a single data bus.

As shown below, a system write signal is used to control the decoded address lines and a 74LS139 decoder driven from the least significant address bits provides the CS1 through CS4 control signals. Address lines A0 and A1 each select a single DAC of the four contained within the AD394 or AD395. The use of a separate address line for each DAC allows several DACs to be simultaneously accessed. The address lines are gated by the microprocessor  $\overline{WR}$  (400ns minimum) and the appropriately decoded base address.

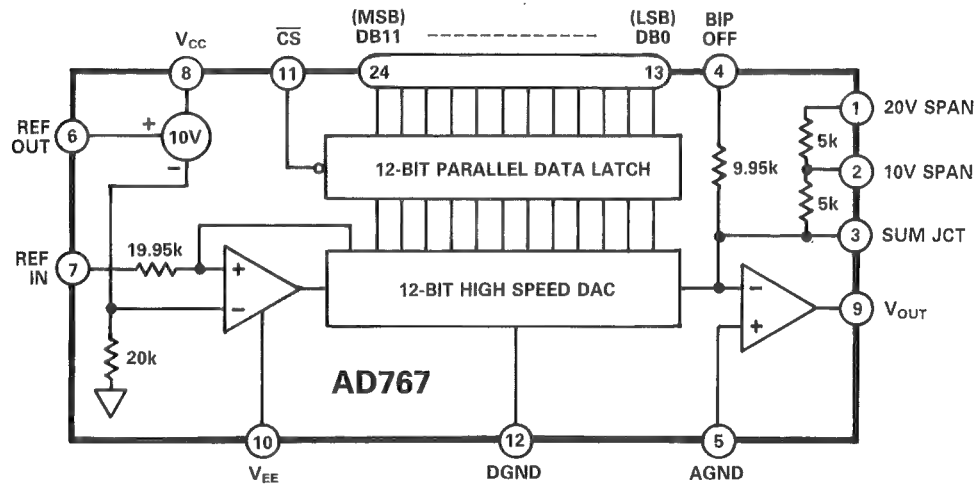
### AD394, AD395 16-BIT BUS INTERFACE



In the circuit shown above, A0 represents the least significant word address bit. Data may reside in either the 12-MSBs (left justified) or the 12-LSBs (right justified). Left justification is useful when the data word represents a binary fraction of full scale while right-justification usually represents an integer value between 0 and 4095.

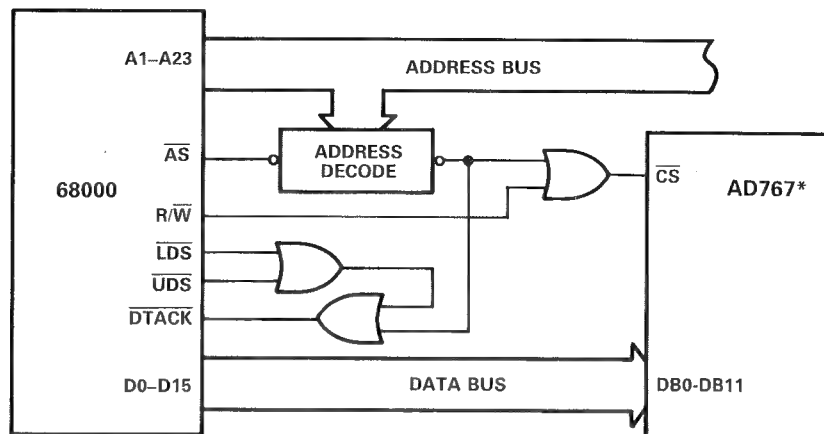
#### AD767 12-Bit Microprocessor Compatible D/A Converter

#### AD767 FUNCTIONAL BLOCK DIAGRAM



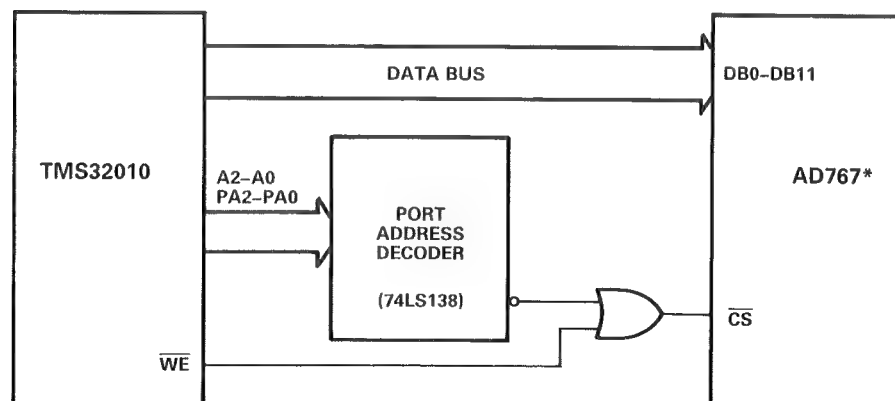
The AD767 with its 40ns minimum  $\overline{CS}$  pulse width may be easily interfaced to any of today's high speed microprocessors. The 12-bit single buffered input register will accept 12-bit parallel load data either right or left justified from processors such as the 68000, 80186, TMS320 series, and the Analog Devices ADSP2100.

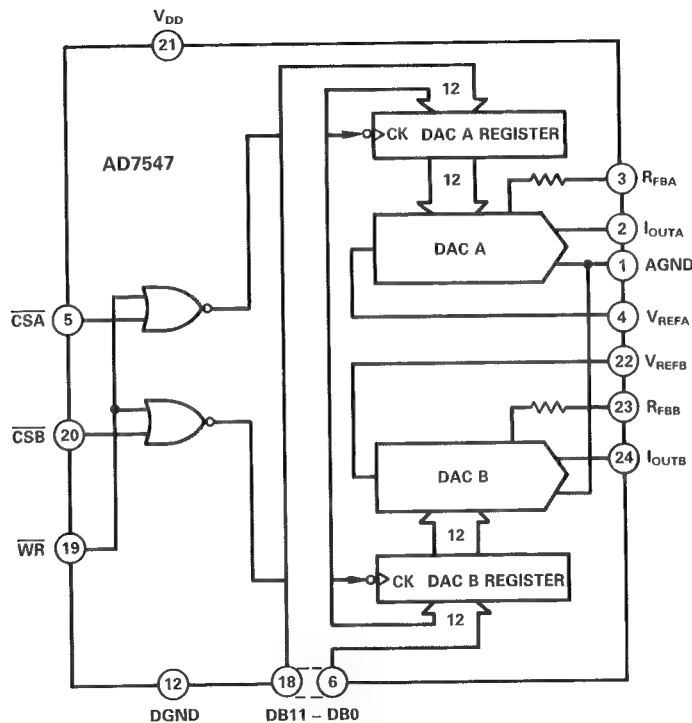
#### 68000 – AD767 INTERFACE



\*LINEAR CIRCUITRY  
OMITTED FOR CLARITY

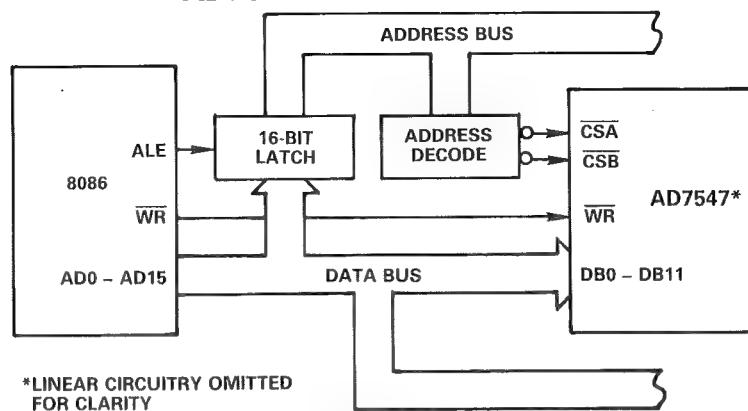
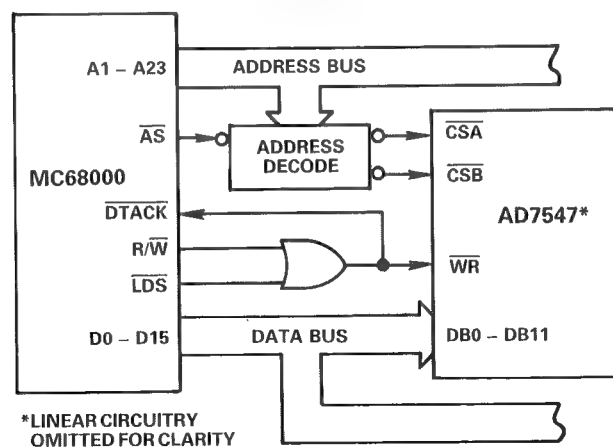
#### TMS32010 – AD767 INTERFACE

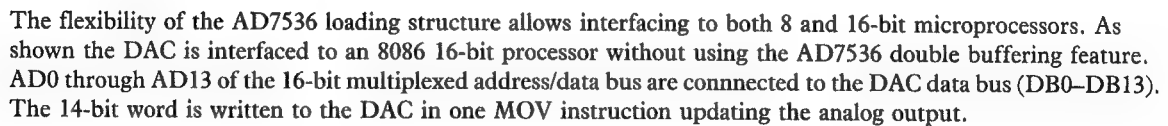


**AD7547 FUNCTIONAL BLOCK DIAGRAM**

The AD7547 is designed for direct interfacing to 16-bit microprocessors with a minimal amount of external hardware. Shown below are interface circuits for two of the most popular 16-bit microprocessors, the 68000 and the 8086.

Data is loaded into the DAC registers on the rising edge of an 80ns minimum WR pulse. Data setup and hold time are 60 and 25ns respectively.

**AD7547 – 8086 INTERFACE****AD7547 – MC68000 INTERFACE**



\*LINEAR CIRCUITRY  
OMITTED FOR CLARITY

## AD7536 – MC68000 INTERFACE



## INTERFACING A/D CONVERTERS

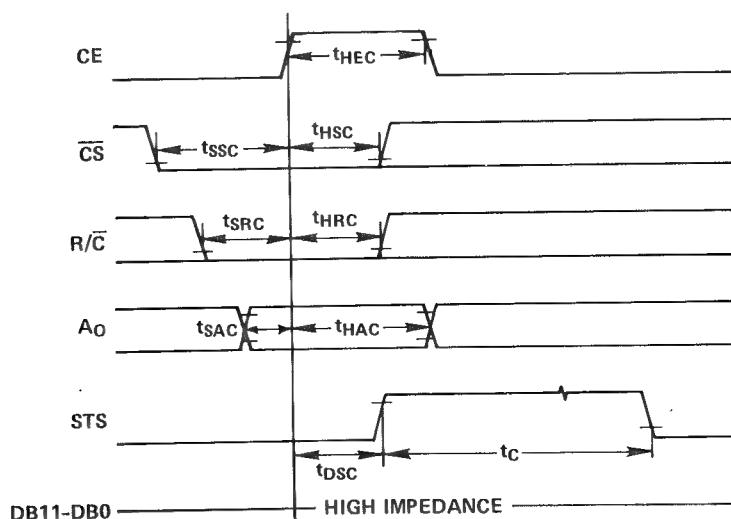
The general considerations for interfacing DACs to microprocessors also apply to ADCs. Whereas a DAC interface consists of a unidirectional transfer of data and control information, the interface of an ADC is bidirectional. Let's investigate this bidirectional interface and some of the common problems associated with it.

### TIMING PARAMETERS

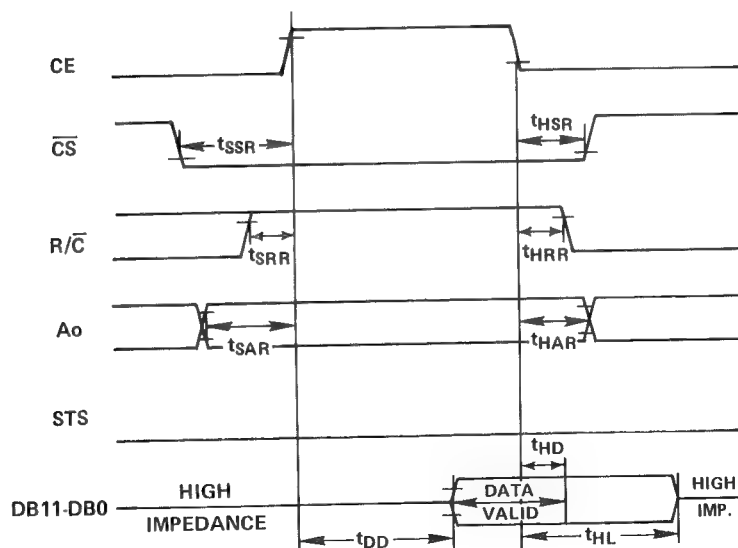
Early microprocessors operated with clock frequencies ranging from 1 to 4MHz and generated control signals with pulse widths of several hundred nanoseconds. As a result, interfacing to an A/D required a handful of logic gates and a few lines of software. Today, however, with microprocessor clock frequencies approaching 25MHz, the designer must carefully analyze all timing parameters. Many older A/D converters will not interface directly with high speed processors due to their faster bus timing. These converters can be interfaced with the addition of a timer or a peripheral interface adapter placed between the processor and converter.

Understanding the converter's timing diagram is the key to a successful interface. Shown below is a typical convert start timing diagram for a 12-bit A/D converter. Note that all timing specifications are referenced to the rising edge of chip enable, (CE).  $\overline{CS}$ ,  $R/\overline{C}$ , and  $A_0$  must be asserted prior to the rising edge of CE and remain valid sometime thereafter to start a conversion. Read cycle timing functions is similar with additional specifications (bus access  $t_{DD}$  and bus float delay  $t_{HL}$ ) associated with the bidirectional aspects of the interface.

### CONVERT START TIMING



### READ CYCLE TIMING



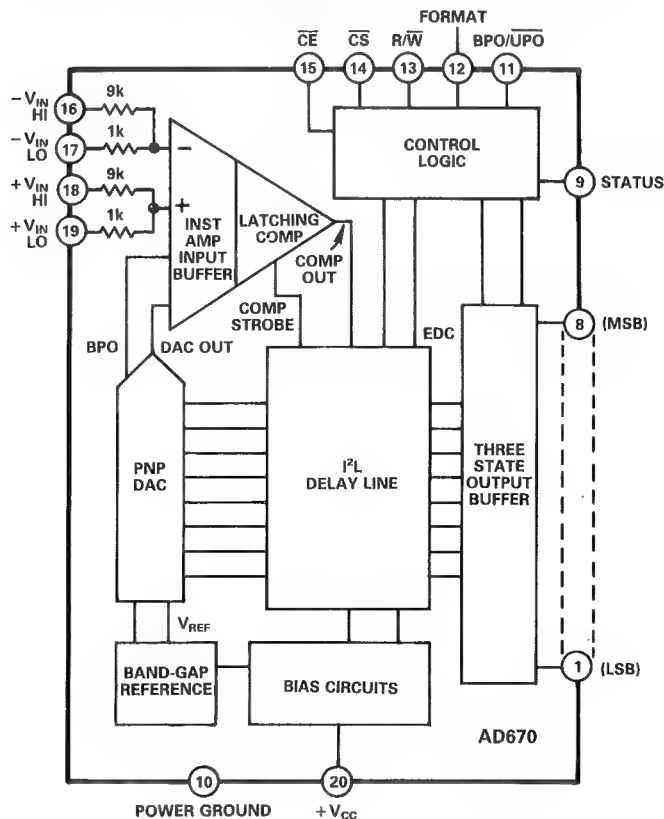
Bus access time defines the amount of time required for the converter's data bus to change from high impedance to valid data. This specification becomes most critical with high speed digital signal processors which may require access times of 100ns or less. Recent developments in converter technology, such as the AD7572 with 90ns access time, have made progress in bus access.

Along with bus access time one must also consider the bus float delay. Bus float delay is defined as the amount of time required for the converter to return the data bus to the high impedance state. This parameter is important to prevent bus contention when dealing with high speed processors. Today, bus float delays of 75ns are becoming the rule rather than the exception. Devices like the AD7572 with its 75ns maximum hold time alleviate many bus interface problems and minimize additional hardware.

## 8-BIT DATA BUS INTERFACING

### AD670 Signal Conditioning 8-Bit ADC

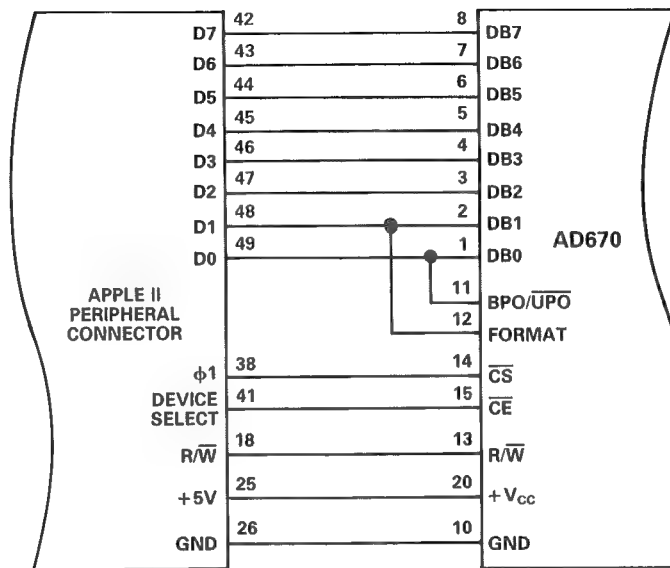
#### AD670 FUNCTIONAL BLOCK DIAGRAM



In many applications low level signals from transducers require signal conditioning prior to analog-to-digital conversion. A 1mV to 100mV signal by itself cannot utilize the full dynamic range of an 8-bit 10V full scale converter. If however, the signal is amplified by 1000, the same 8-bit converter can now provide meaningful data. Typically an external instrumentation amplifier serves as the gain stage but the AD670 incorporates an internal instrumentation amplifier. With its pin-programmable amplifier, the AD670 can resolve either 1mV or 10mV per LSB. In addition, a TTL compatible control signal allows the user to select unipolar or bipolar input signals.

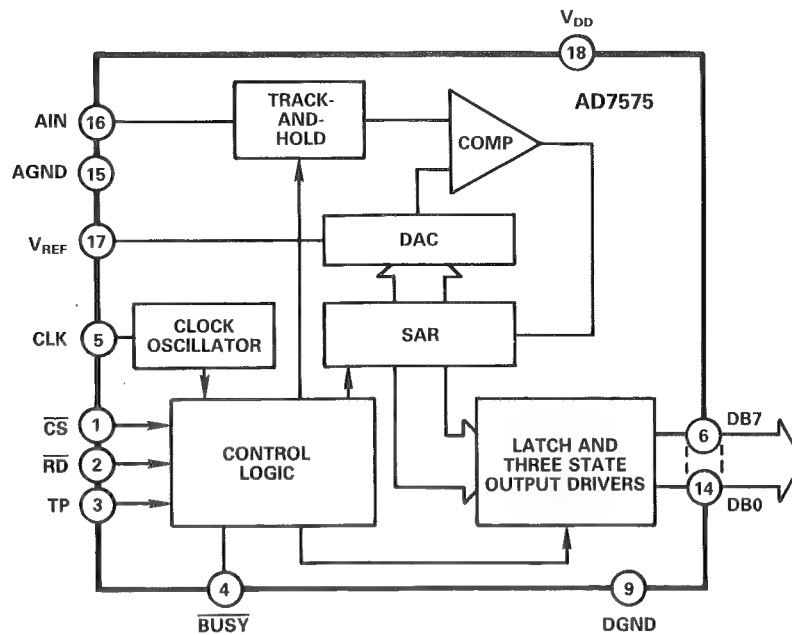
Most signal conditioning applications will use dedicated microcontrollers or the slower microprocessors. In many instances interfacing to a personal computer which provides access to control and data bus may be convenient. The Apple II is shown interfaced to the AD670. A unique feature of this interface is the ability to select data format via software. A POKE 49360, 2 statement prior to conversion selects a 2's complement data format.

## APPLE II INTERFACE



## AD7575/76 LC<sup>2</sup>MOS Microprocessor Compatible ADC

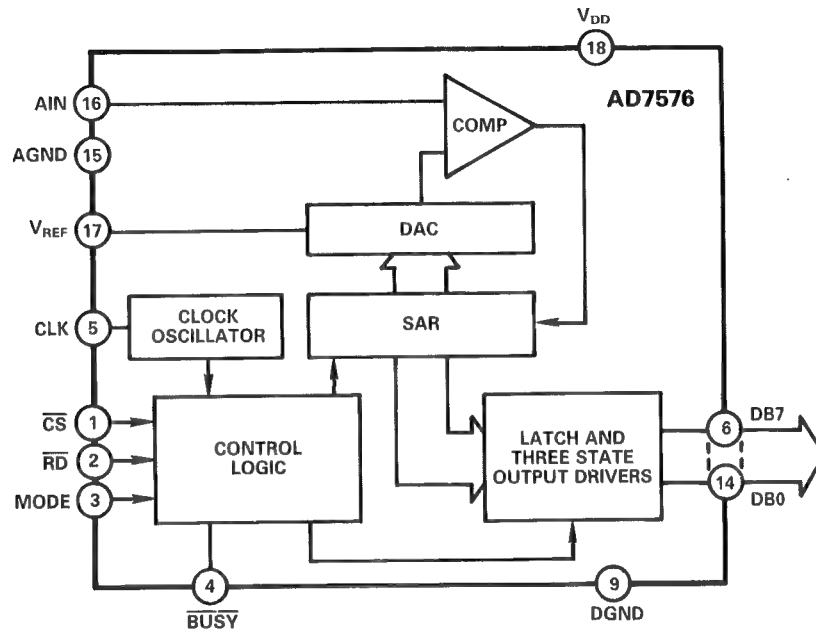
### AD7575 FUNCTIONAL BLOCK DIAGRAM



The AD7575 and AD7576 family of 8-bit converters offers complete flexibility when interfacing to 8-bit processors. These devices can be easily configured as a memory mapped device or can be interfaced as SLOW-MEMORY or ROM. Each mode of interfacing will be described in detail.



## AD7576 FUNCTIONAL BLOCK DIAGRAM



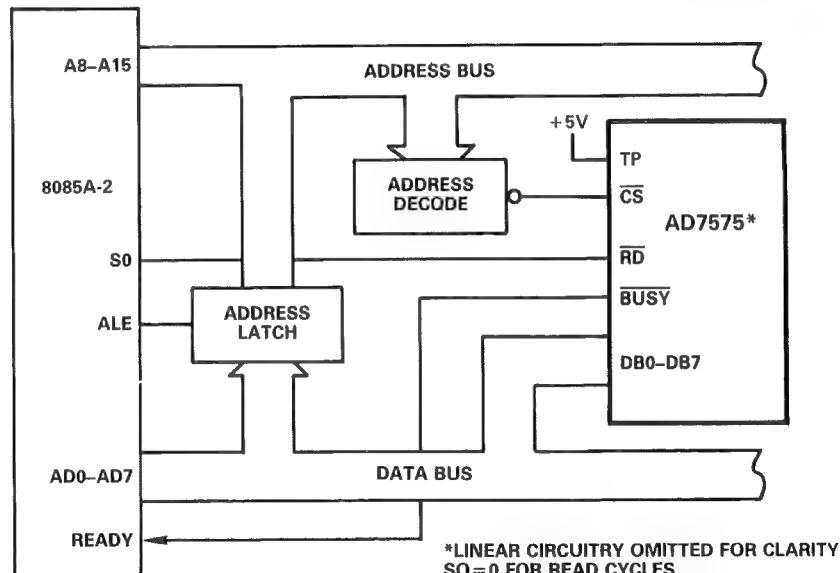
### SLOW-MEMORY INTERFACE

The first interface option is designed for use with microprocessors such as the 8086 or 68000 which can be forced into a WAIT STATE for a minimum of 5 microseconds for the AD7575 and 10 microseconds for the AD7576. The processor starts a conversion and is halted until valid data is read from the converter. Conversion is initiated by executing a memory READ to converter's address bringing  $\overline{CS}$  and  $\overline{RD}$  LOW.  $\overline{BUSY}$  goes LOW placing the processor into a wait state.  $\overline{BUSY}$  remains LOW for the duration of the conversion and returns HIGH at which time the processor finishes the memory READ and acquires the newly-converted data.

The major advantage of this interface is that it allows the processor to start conversion, wait, and then read data with a single read instruction. The fast conversion times of these converters ensures that the processor is not held in a wait condition too long.

Faster versions of many processors test the condition of the READY input soon after the start of an instruction cycle. For the READY input to force the processor into a WAIT state, the converter's  $\overline{BUSY}$  must go LOW early in the bus cycle. If using the 8085-A2, the processor's S0 status signal gives the earliest indication that a READ operation is to occur. The connection diagram for the 8085-A2 Slow-Memory interface is shown below.

### AD7575 TO 8085A-2 SLOW MEMORY INTERFACE



## ROM INTERFACE

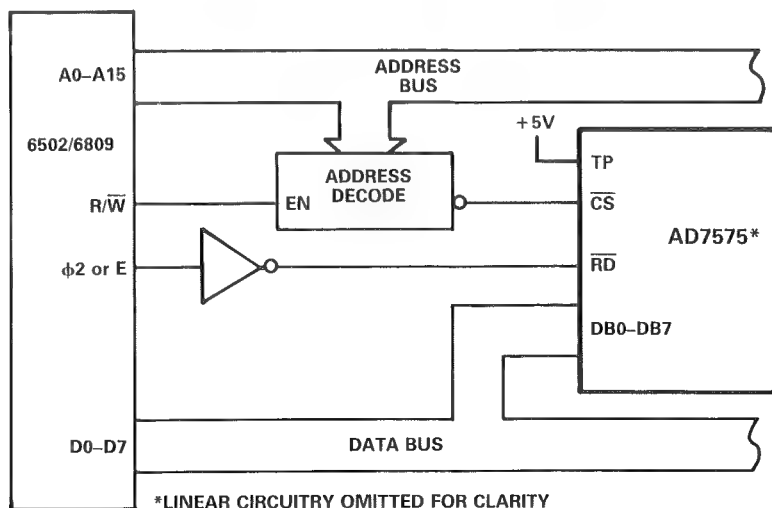
The alternative interface option avoids placing the processor into a WAIT state. A conversion is started with the first READ instruction and the second READ instruction accesses the data and starts a new conversion.

Conversion is initiated by executing a memory READ to the converter placing  $\overline{CS}$  and  $\overline{RD}$  LOW. Data from the previous conversion becomes available but may be ignored. Busy goes LOW indicating conversion in progress and returns HIGH after completion. The  $\overline{BUSY}$  signal may be used to generate an interrupt or polled by the processor. For the converter to operate correctly in the ROM mode  $\overline{CS}$  and  $\overline{RD}$  should not go LOW before  $\overline{BUSY}$  returns HIGH.

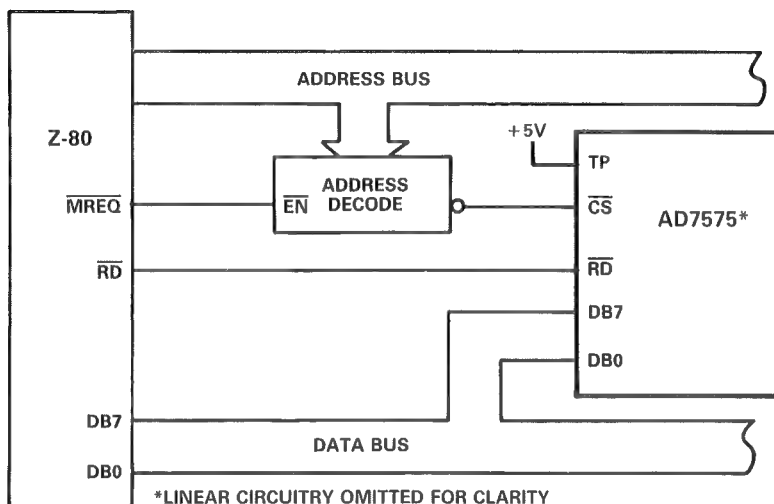
Normally the second READ starts another conversion. If  $\overline{CS}$  and  $\overline{RD}$  are brought LOW within one external clock period of  $\overline{BUSY}$  going HIGH then a second conversion does not occur.

The disadvantage with this interface option is that the age of the data is unknown. That is, the data read is the result of a conversion which was initiated by the previous read cycle.

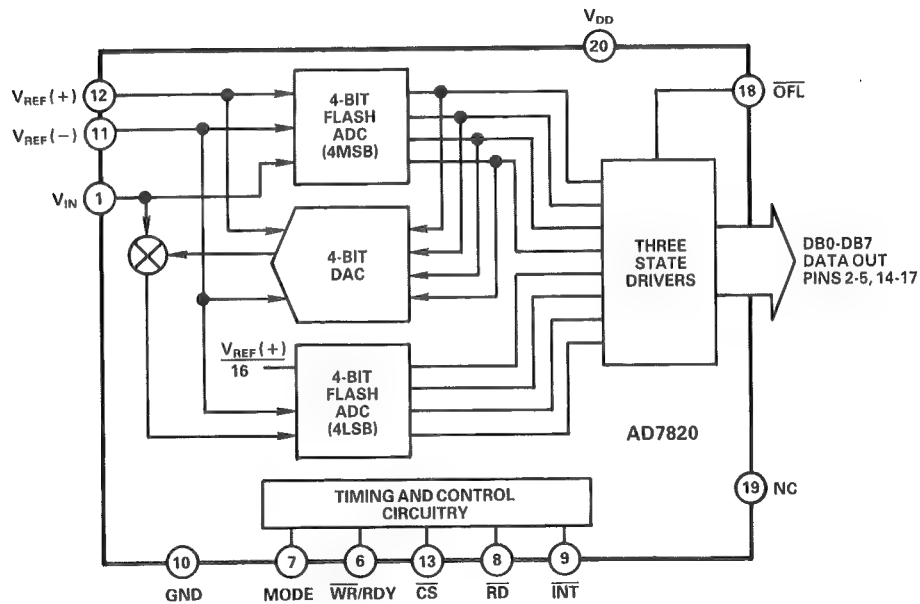
### AD7575 TO 6502/6809 ROM INTERFACE



### AD7575 TO Z-80 ROM INTERFACE



## AD7820 FUNCTIONAL BLOCK DIAGRAM



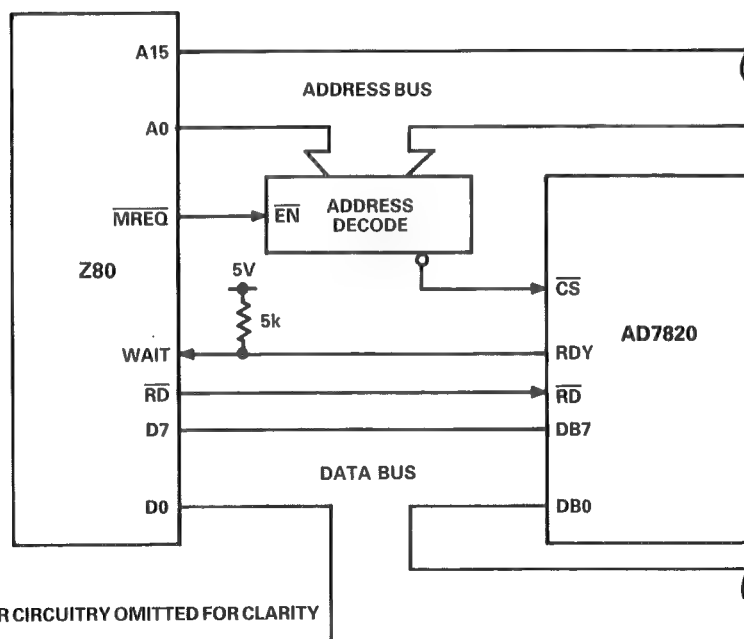
The AD7820 interface techniques are very similar to those shown for the AD7575/76. Here again, two interface modes are available depending upon the status of the **MODE** pin. With this pin **LOW** the AD7820 is in the **RD** mode whereas a **HIGH** places the converter in the **WR-RD** mode.

## RD MODE

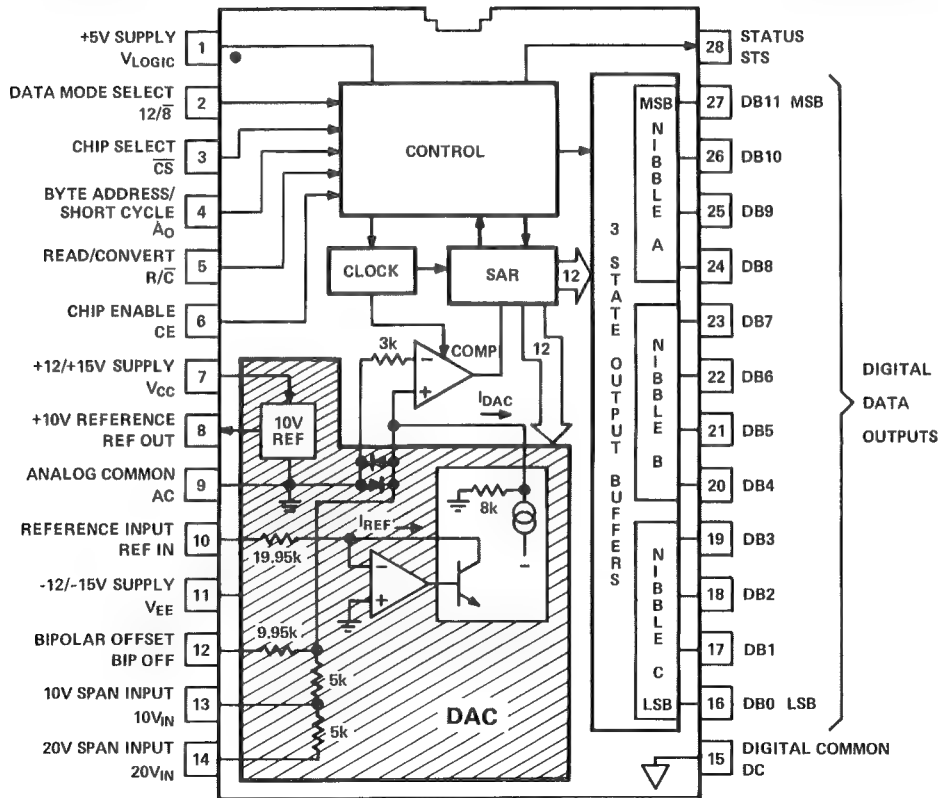
In the RD mode conversion is initiated by pulling  $\overline{\text{RD}}$  LOW and holding it there 1.6 microseconds until output data appears. Pin 6 of the converter, RDY, provides a status output and can be used to put the processor into a WAIT state. RDY is an open drain output which goes LOW after the falling edge of  $\overline{\text{CS}}$  and returns to the high impedance state at the end of conversion.

A typical interface to a Z80 is shown below. A LD B, (xxxx) statement will start conversion. At the beginning of the instruction cycle when the converter's address is decoded, RDY goes LOW to force the processor into a WAIT state. Upon completion of conversion RDY returns HIGH and the conversion result is stored in the processor's B register.

## AD7820-Z80 INTERFACE



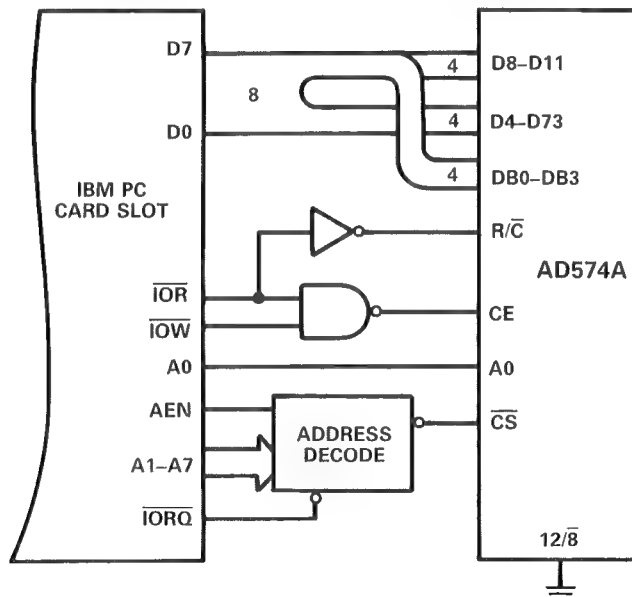
## AD574A BLOCK DIAGRAM AND PIN CONFIGURATION



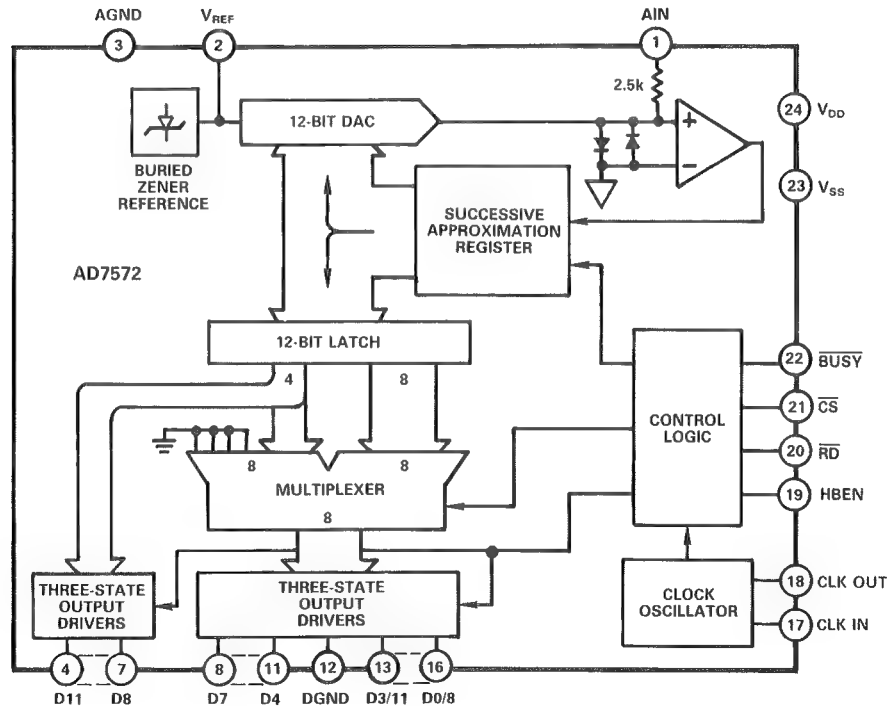
The AD574A has become the industry standard for 12-bit A/D converters. Developed by Analog Devices in the late 1970's this device has probably interfaced to more processors than any other converter in its class.

The AD574A appears below interfaced to a 4MHz. 8088 processor of an IBM PC. Since the converter resides in I/O space its address is decoded from only the lower 10 address lines and must be gated with AEN to mask out internal DMA cycles which use the same I/O space. This active LOW is applied to  $\overline{CS}$ .  $\overline{IOR}$  and  $\overline{IOW}$  are used to initiate the conversion and read data. They are gated together to drive the  $\overline{CE}$ .  $A_0$  selects the 2 adjacent memory locations which store the 8 MSBs and 4 LSBs of the left-justified data.

## IBM PC – AD574A INTERFACE



## AD7572 FUNCTIONAL BLOCK DIAGRAM



Major breakthroughs in CMOS technology paved the way to the development of the AD7572 A/D converter. Using a mixed bipolar-CMOS process, improvements in conversion speed as well as faster bus timing were all made possible. In addition, this converter became the first CMOS A/D to incorporate an internal buried zener reference.

Conversion start and data read operations are controlled by three TTL compatible inputs:  $\overline{CS}$ ,  $\overline{RD}$ , and HBEN. These three signals are internally gated such that a LOW on all inputs will begin a conversion. Once a conversion is started it cannot be restarted until the present conversion is finished. During conversion a LOW  $\overline{BUSY}$  output indicates a conversion in progress.

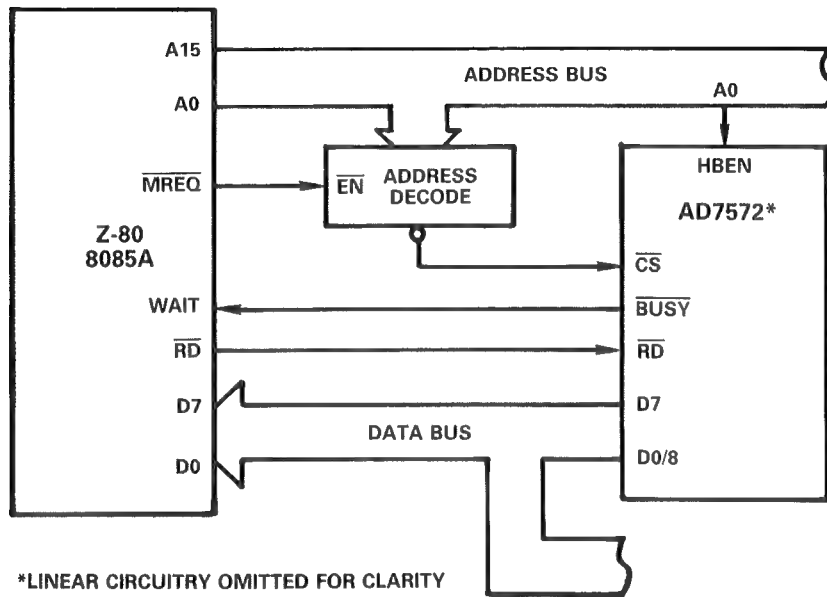
There are two modes of operation available for interfacing the device to a processor. They are the Slow Memory Mode and the ROM mode which were previously described in the section on the AD7575/76. The only difference however is the AD7572's data format which can be 12 bit parallel or two bytes of right-justified data.

The AD7572 is easily interfaced to a Z80 or 8085A. As shown, the converter is operating in the Slow Memory Mode and a two byte read is required. An 8-bit latch such as an 8282 is used to demultiplex the address/data bus with the decoded address providing the AD7572  $\overline{CS}$ . An even address (A0 LOW) will start a conversion and read the low data byte. An odd address will read the corresponding high data byte. All this is accomplished with a single 16-bit LOAD instruction:

LDHL (B000) for the 8085A  
LDHL (B000) for the Z80

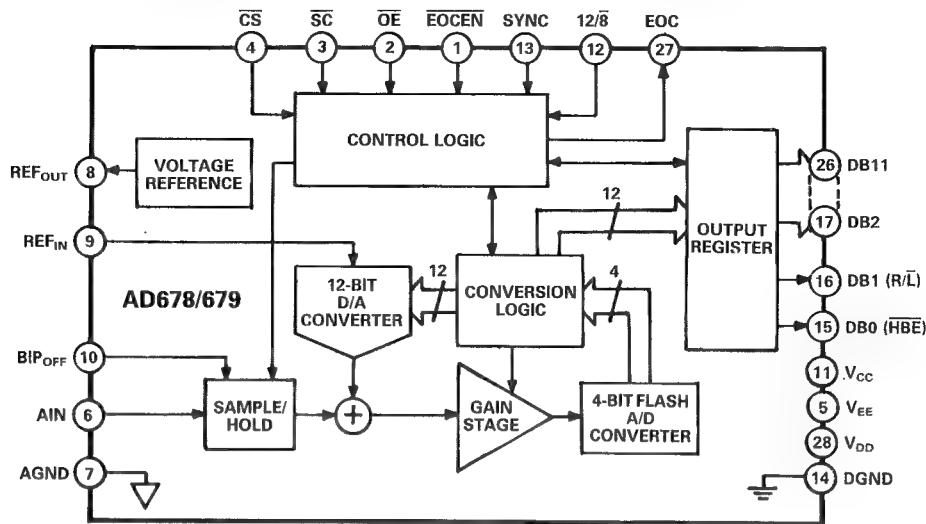
This instruction will load the converter's data (address B000) into the HL register pair. During the first read operation,  $\overline{BUSY}$  forces the processor to wait for completion of conversion. The high data byte is then read with a second read operation without the addition of wait states.

## AD7572 – 8085A/Z80 INTERFACE



## AD678/679 Monolithic 12/14-Bit Sampling A/D Converter

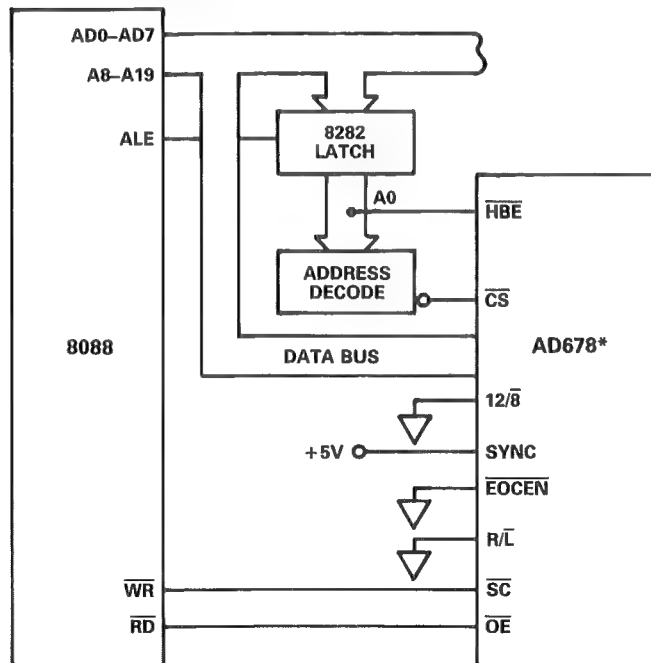
### BLOCK DIAGRAM OF AD678/679 SAMPLING 12/14-BIT A/D CONVERTER



The AD678 12-bit A/D converter and the AD679 14-bit converter are the newest addition to Analog Devices' family of high resolution converters. Within a 28-pin package, the device incorporates a sample-and-hold amplifier, voltage reference, and three state output buffers. The high speed digital control logic and fast bus access time ensures operation with the fastest processors. Moreover, the converter may be configured to support 8- or 16-bit bus interfacing with selectable right or left justified data. In addition, the three-state output data buffers may be enabled during conversion allowing data from the previous conversion to be read into the processor via DMA.

Interfacing the AD678 to an 8088 microprocessor is easily accomplished. A 74LS374 address latch is used to demultiplex the address/data bus and the decoded address provides a LOW  $\overline{CS}$  to the AD678. A LOW  $\overline{WR}$  pulse initiates a conversion and 5 microseconds later conversion is complete. The processor now issues a  $\overline{RD}$  to an even decoded address ( $A_0 = \text{LOW}$ ) enabling the 8 MSBs. Since the  $R/\overline{L}$  control is hardwired LOW this data will be left-justified. A second  $\overline{RD}$  to the next decoded address ( $A_0 = \text{HIGH}$ ) outputs the 4 LSBs with 4 trailing zeroes.

### 8088 – AD678 INTERFACE

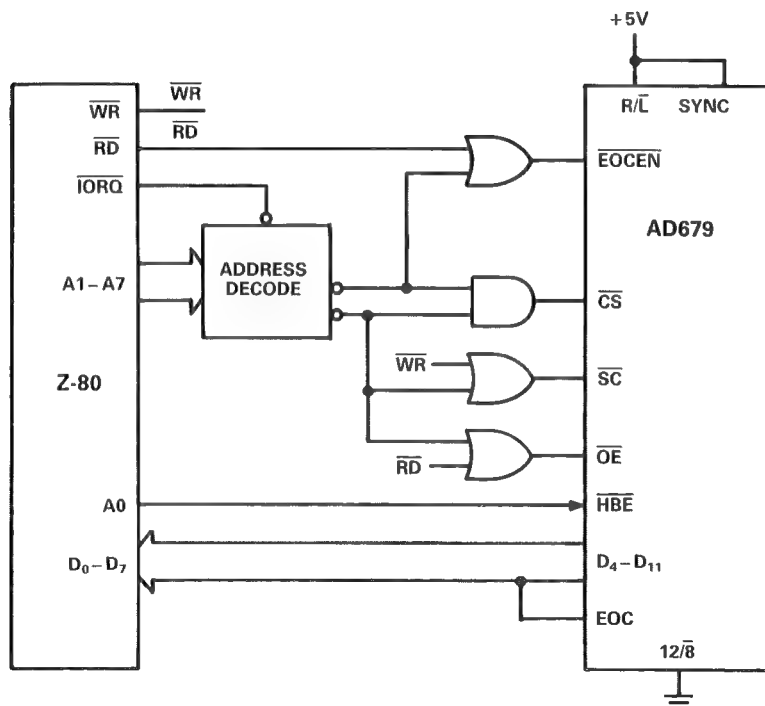


\*LINEAR CIRCUITRY OMITTED FOR CLARITY

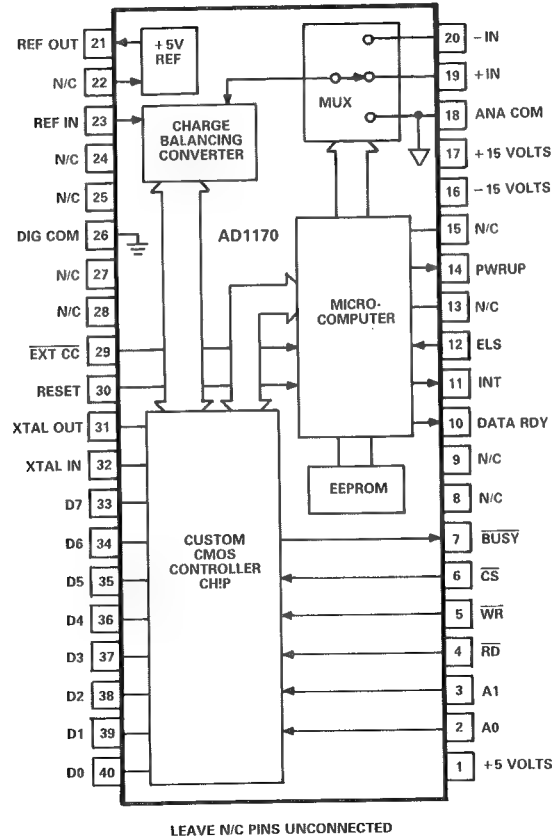
Using an I/O or memory-mapped configuration, the AD678 can be interfaced to the Z80 microprocessor. As shown, the converter occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit,  $A_0$ , is used to select the high and low-order bytes of the result. The  $R/\overline{L}$  control is tied high resulting in right-justified output data.

The Z80 processor will automatically insert a single wait state during I/O operations. This feature allows the AD679 to be used with the Z80 having a clock speed up to 8MHz.

### AD679 TO Z-80 INTERFACE



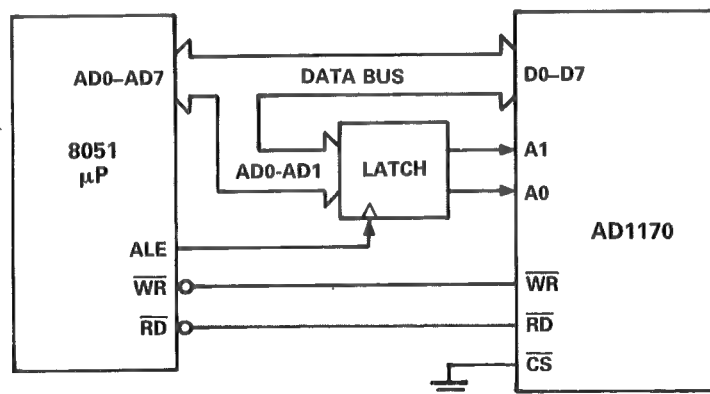
## AD1170 FUNCTIONAL BLOCK DIAGRAM



Many high precision applications require more than 16 bits of resolution that is available in monolithic technology. In addition, many of today's 16-bit converters can only achieve 14 bits of accuracy and most often require external trimming for gain and offset. In some instances where external trimming is not feasible, then a software routine to calculate gain and offset errors might be used. Such a routine is illustrated in the Data Acquisition Subsystem section of this book. But these routines require additional memory and software overhead not to mention the time spent debugging the program. The AD1170 however provides an easy solution to high resolution A/D conversion. Using a charge balancing conversion technique and self calibration of gain and offset, the AD1170 offers 16 bits of accuracy in a  $1.25 \times 2.5 \times 0.55$  inch package.

As shown, the AD1170 is interfaced to an 8051 microcomputer. An external latch is used to latch the two lowest order address bits from the multiplexed data bus. The indirect external data command MOVX is the only instruction required to access the converter.

## 8051 – AD1170 INTERFACE





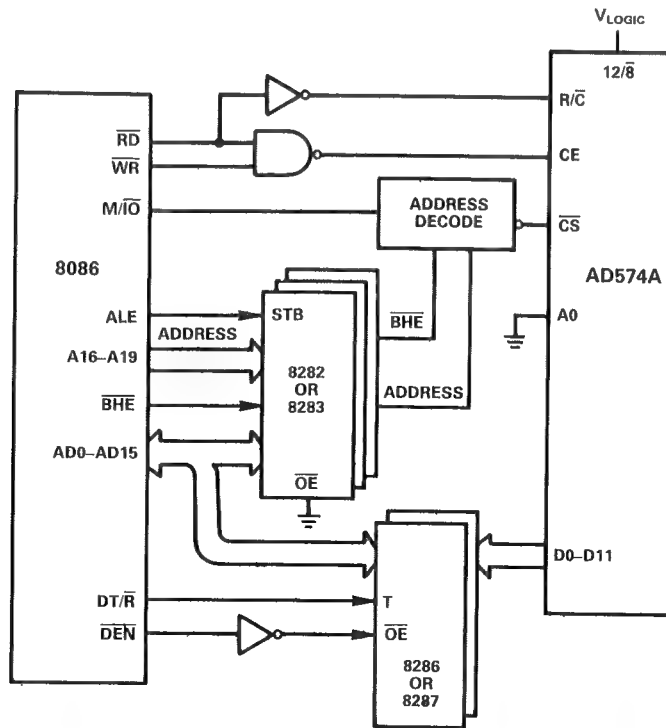
## 16-BIT BUS INTERFACING

### AD574A 12-Bit A/D Converter

Interfacing an AD574A to a 16-bit data bus is quite similar to the 8-bit interfacing techniques previously shown. When using a 16-bit bus the data mode select pin (12/8) should be connected to  $V_{\text{LOGIC}}$  and A0 is hardwired LOW. The data format is selected by the user either left or right justified by wiring the 12 data outputs to the 12 MSBs or 12 LSBs of the bus.

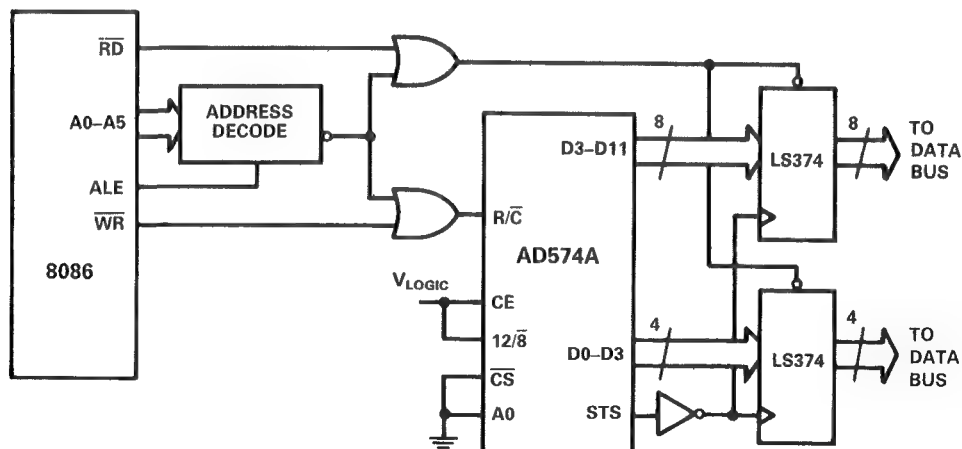
An 8086 interface is shown below. An 8282 latch is connected to the multiplexed address/data bus to demultiplex the address bus and an 8286 provides data bus buffering. This technique is strongly recommended with any multiplexed bus to prevent possible bus contention and to minimize digital feedthrough noise. Note that no wait states are needed for 8086 clock frequencies up to 6MHz.

### 8086 – AD574A WITH BUFFERED BUS INTERFACE



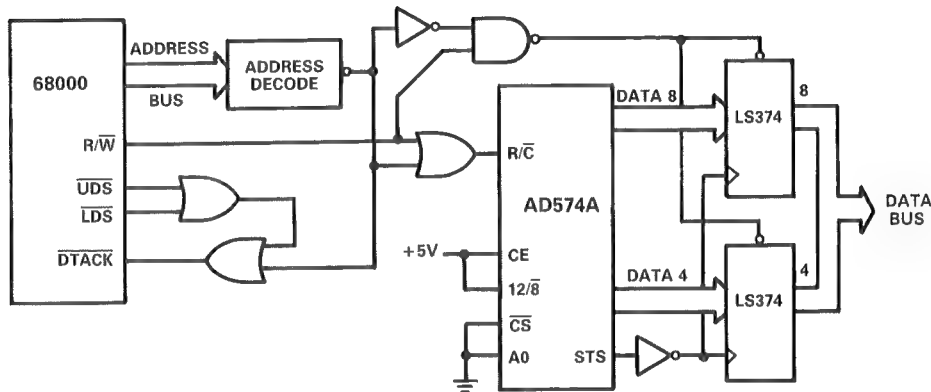
Stand-alone operation of the AD574A often allows the user to interface to high speed processors. In this mode, a single LOW going pulse to the  $\text{R}/\overline{\text{C}}$  control line is all that is necessary to start conversion. The converter's STS line will go HIGH and remain high for the duration of conversion. Prior to the falling edge of STS, data becomes valid and can be conveniently latched into a three-state latch such as a 74ALS374. The data is now read by enabling the latch's output enable. This method eliminates problems with bus access and bus float delay that are often encountered with higher speed processors.

### 8086 – STAND-ALONE CONFIGURATION



Stand-Alone operation is also possible with the 68000 microprocessor. The 68000  $R/\overline{W}$  signal combined with a low address decode initiates conversion. The  $\overline{UDS}$  and  $\overline{LDS}$  signals with the decoded address generates the  $\overline{DTACK}$  input to the processor. A read cycle then reads data from the three-state latches.

### 68000 – AD574A INTERFACE



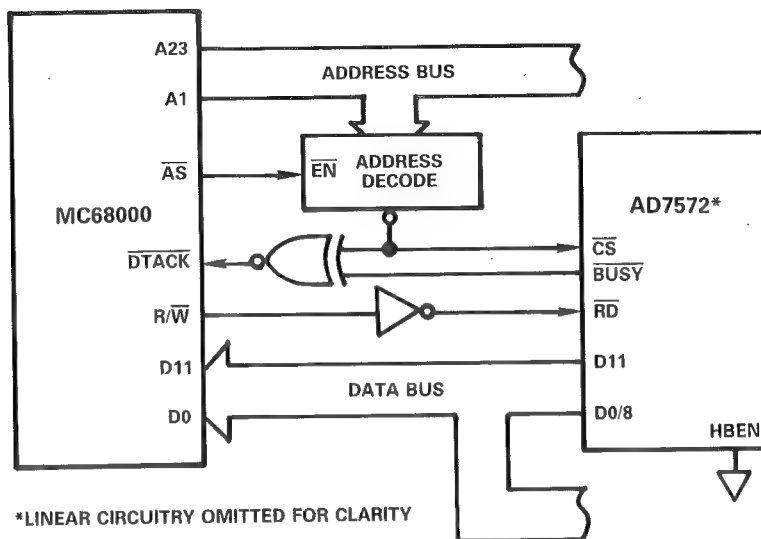
### AD7572 5 $\mu$ s A/D Converter

A typical interface for the 68000 is shown below. The AD7572 is operating in the Slow Memory Mode. Assuming the AD7572 is located at address B000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion results.

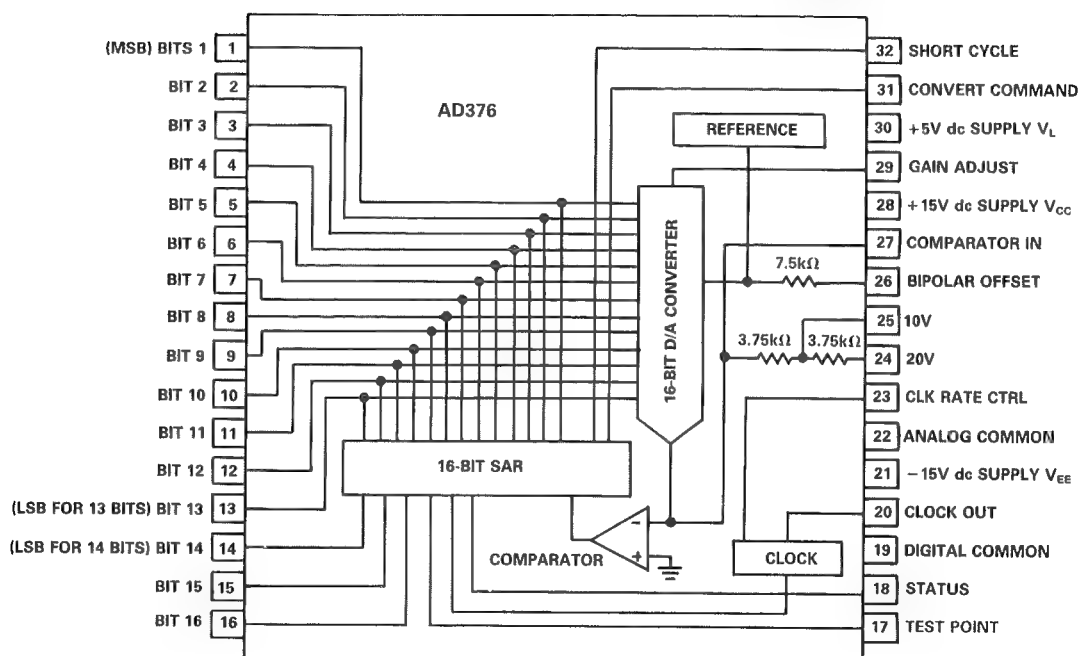
Move.W \$B000,D0

At the beginning of the instruction cycle when the A/D address is selected,  $\overline{BUSY}$  and  $\overline{CS}$  assert  $\overline{DTACK}$  forcing the 68000 into a WAIT state. At the end of conversion  $\overline{BUSY}$  returns HIGH and the conversion result is placed in the D0 register of the processor.

### AD7572 – MC68000 INTERFACE



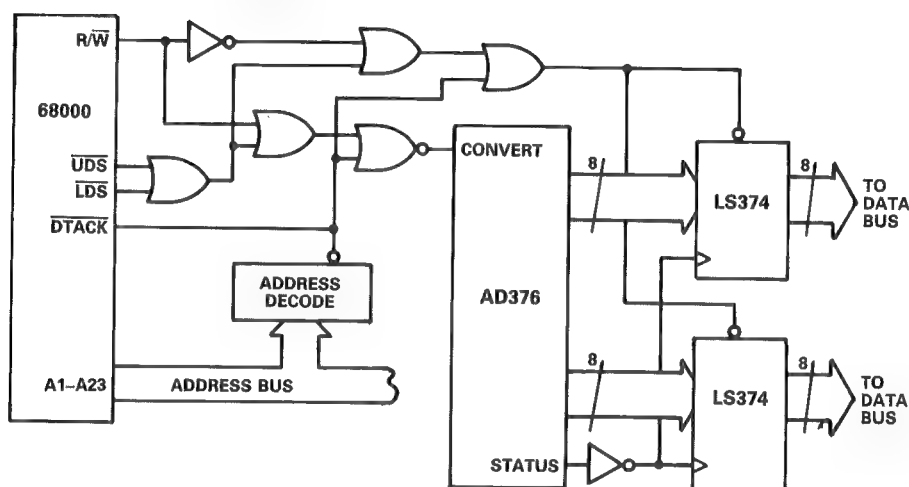
## AD376 FUNCTIONAL BLOCK DIAGRAM



The simple control logic of the AD376 makes it an ideal candidate for interfacing to high speed processors. A 50ns high convert start pulse drives the STATUS line HIGH, removes the gated clock inhibit, and starts the 16-bit successive approximation process. One clock cycle after the falling edge of CONVERT START the MSB bit decision is made and data becomes valid on the rising edge of the internal clock. This negative true data (Logic "1" = 0.4V max and Logic "0" = 2.4V min) remains latched during the entire conversion process. The subsequent bit decisions are made and STATUS goes LOW to indicate end of conversion.

Interfacing the AD376 to a 68000 microprocessor requires minimal hardware. A LOW decoded address gated with the processor's  $\overline{WR}$  generates a pulse. Two 74ALS244 octal bus buffers isolate the AD376 from the data bus and offer fast bus access and float delay necessary for operation with high speed processors.

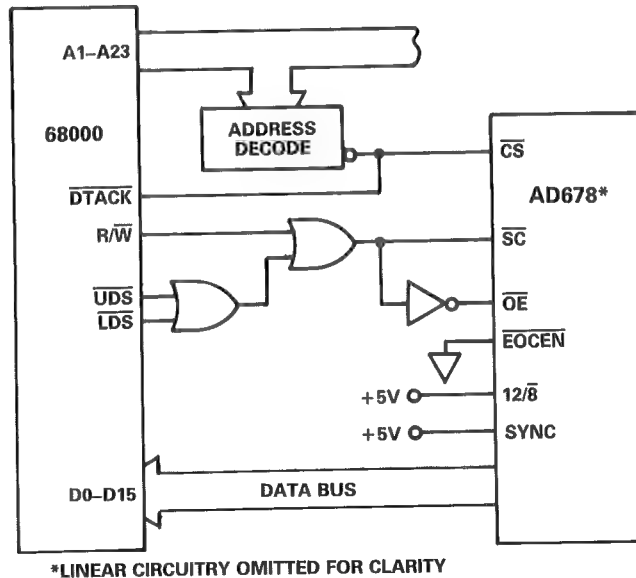
## 68000 – AD376 INTERFACE



### AD678 12-Bit Sampling A/D Converter

The high speed bus interface of the AD678 12-bit sampling A/D converter supports a direct bus interface to a 12.5MHz 68000 system. A LOW address decode asserts the AD678  $\overline{CS}$  and  $\overline{DTACK}$  allowing the processor to run at full speed without the need for wait states. To start conversion, a LOW going R/W signal OR'ed with the OR gate output of  $\overline{UDS}$  and  $\overline{LDS}$  produce a LOW  $\overline{SC}$  pulse. 5 $\mu$ s later, conversion is complete and the processor can now read data.

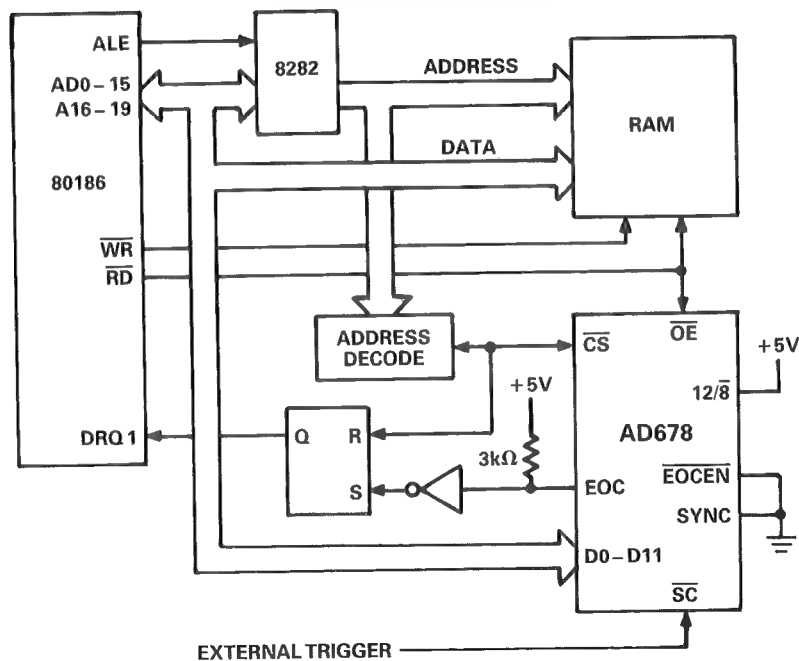
### 68000 – AD678 INTERFACE



A 6MHz or 8MHz 80186 processor is shown interfaced to the AD678 converter. This configuration allows the processor's internal DMA controller to transfer the AD678 output into a RAM-based FIFO buffer of any length with no processor intervention.

The AD678 is configured in the Asynchronous mode allowing conversions to be initiated by an external trigger source independent of the processor clock. After each conversion, the AD678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA read operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion.

### AD678 TO 80186 DMA INTERFACE (ASYNCHRONOUS)

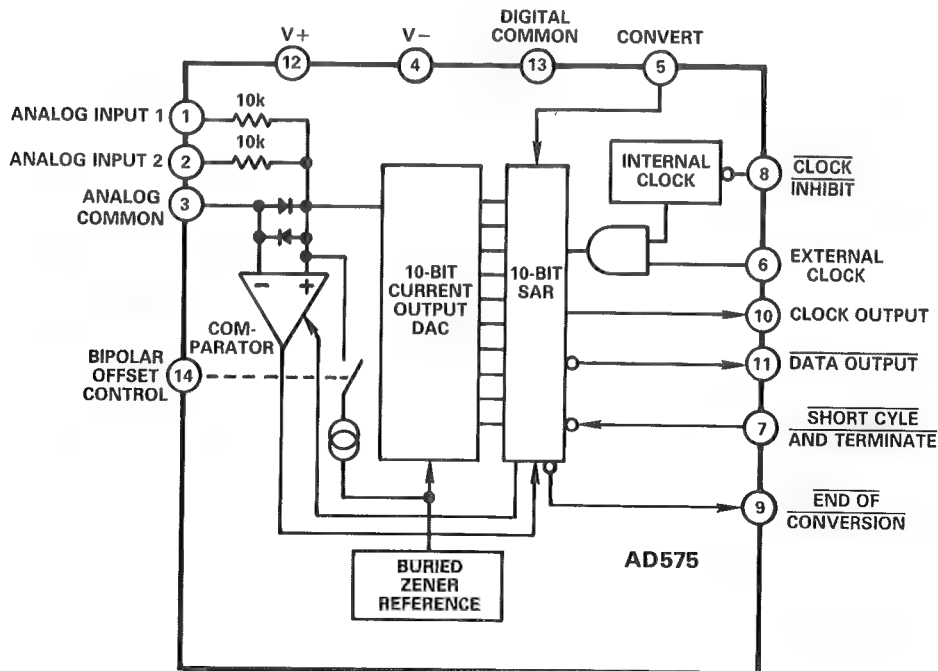


## INTERFACING CONVERTERS WITH SERIAL OUTPUT

Some microprocessors such as the 8085 and the TMS32020 can accommodate serial I/O. Generally speaking most A/D converters have parallel data formats. In order to connect these converters to a serial input port, a shift register would be required to convert to serial format. The increasing popularity however of digital signal processors in audio applications has focused attention to developing more converters with serial outputs. Let's look at some of these developments.

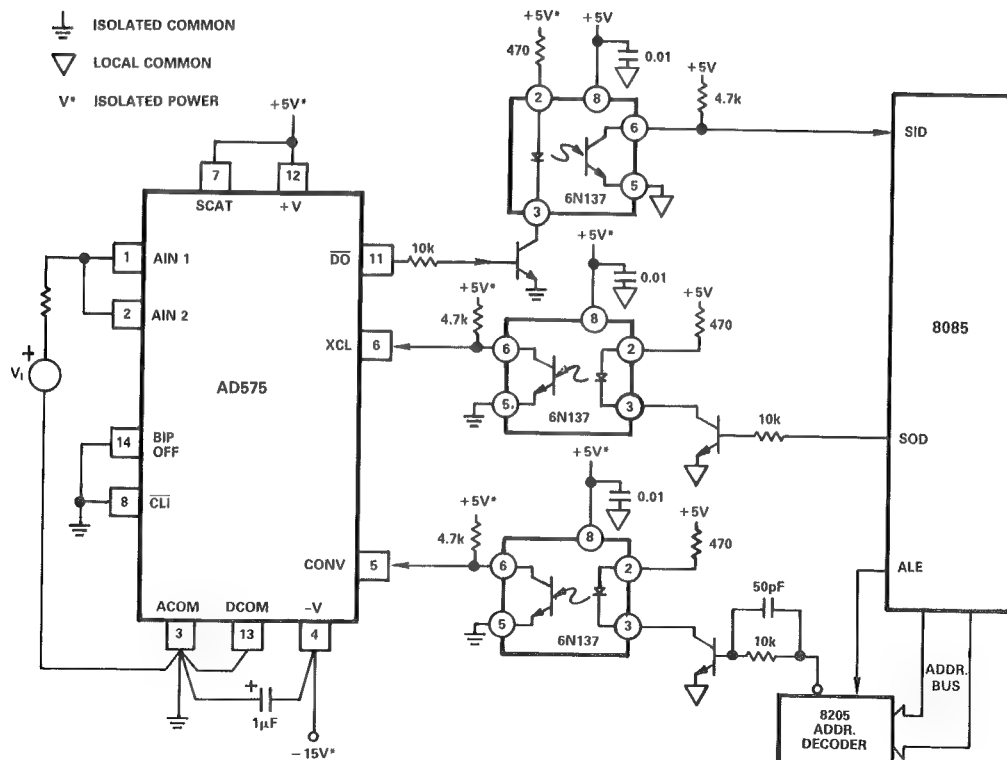
## AD575 10-Bit A/D Converter with Serial Output

## AD575 FUNCTIONAL BLOCK DIAGRAM



The 8085 has both serial output (SOD) and serial input (SID) capability. Using opto-coupling to establish galvanic isolation between processor and converter a simple three wire interface can be configured.

## AD575 TO 8085 ISOLATED INTERFACE



The software routine listed below will read a complete 10-bit data word from the AD575 in 180 $\mu$ s using a 3MHz 8085. The software generates the clock for the AD575 in order to synchronize the data output with the 8085 serial read operation.

The DATA procedure loads appropriate constants into the 8085 registers and initiates the conversion. The CONV routine assumes the AD575 clock was in the high state when the CONVERT pulse was generated. A low clock pulse is generated and the data bit is read into the MSB of the accumulator. The data bit is then shifted into the LSB of the temporary register (L), the clock is set high, and the procedure is repeated.

After the loop has executed three times, a logical AND is performed to set the first bit to zero. The result is then placed into the high byte (H) register. The loop counter is reset, and the CONV routine is executed 8 more times. Upon completion of the routine, 10 bits of right-justified data will reside in the HL register pair.

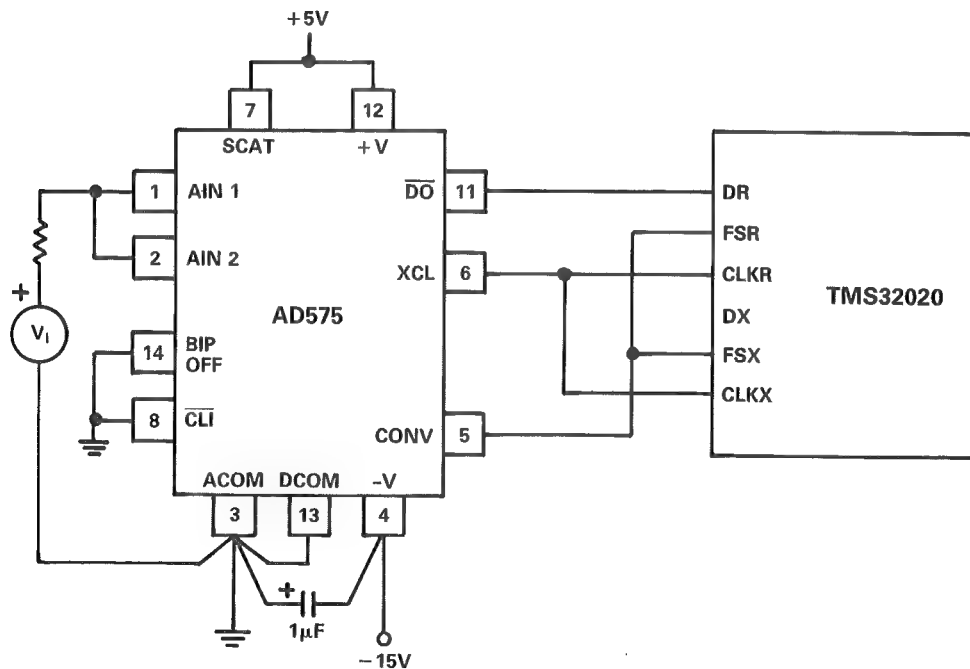
Note that the opto-isolators invert the clock and data lines. If these are not used the constants in the D and E registers must be swapped, a CMA instruction should be inserted after the RIM instruction, and an inverter should be connected between the address decoder and the CONVERT pin. In addition following power up and reset, the results of the first pass through the routine are invalid.

## SAMPLE ASSEMBLY CODE FOR AD575 to 8085 ISOLATED INTERFACE

LABEL	MNEMONIC	OPERAND	COMMENT
DATA	MVI	B,03	Set inner loop counter to 3
	MVI	C,02	Set outer loop counter to 2
	MVI	D,CO	Setup register D for clock low
	MVI	E,40	Setup register E for clock high
	MVI	H,10	AD575 address location
	MVI	L,00	Clear temp register
	MOV	M,B	Generate CONVERT pulse
CONV	MOV	A,D	Setup ACC for clock low
	SIM		Output clock low
	RIM		Read AD575 data bit into ACC
	RAL		Shift data bit into Carry
	MOV	A,L	Move temp to ACC
	RAL		Shift data bit from Carry to ACC
	MOV	L,A	Replace temp
	MOV	A,E	Setup ACC for clock high
	SIM		Output clock high
	DCR	B	Decrement inner loop counter
	JNZ	CONV	Repeat CONV until done
	DCR	C	Decrement outer loop counter
	JZ	DONE	Skip to DONE on 2nd pass
	MOV	A,L	Move temp to ACC
	ANI	03	Mask undefined bit
	MOV	H,A	Store temp in H register
	MVI	B,0B	Set inner loop counter to 8
	JMP	CONV	Repeat CONV for 8 LSBs
DONE	RET		10 bits of right-justified data now reside in HL; return

Shown below is a simple serial interface using the AD575 and the TMS32020 Digital Signal Processor. The converter is configured for external clock operation, the clock being provided by the processor's CLKR and CLKX signals. Conversion is initiated on the rising edge of FSR and FSX with the first data bit (the MSB) valid on the falling edge. Note that the data format is complementary.

### TMS32020 - AD575 SERIAL INTERFACE



### ANALOG-TO-DIGITAL CONVERSION USING VOLTAGE-TO-FREQUENCY CONVERTERS

A voltage-to-frequency converter (VFC) is a device which accepts at its input an analog voltage or current signal and provides at its output a train of pulses or square waves at a frequency which is proportional to the input value. A VFC can thus be used as a building block in an A/D conversion system by using the VFC to clock a counter for a certain period of time and reading the output digital word. This digital word will be proportional to the analog input.

There are a number of advantages to using a voltage-to-frequency converter in an A/D conversion scheme. First, unlike converters based on binary-weighted networks, monotonicity is inherent under all supply and temperature conditions. Second, the fact that the signal is converted to an easily-transmitted serial bit stream allows the analog circuitry (the VFC and analog signal conditioning) to be located close to the signal source and the digital circuitry to be located elsewhere. This is especially advantageous when a large number of channels are required; the remote VFCs can be used to provide "converter-per-channel" data acquisition. Finally, since the digital number is accumulated over a large number of cycles, integration of and reduction of unwanted signals is inherent.

The time required to convert an analog signal into a digital word is related to the maximum full-scale frequency of the VFC and the required resolution of the measurement. For example, the Analog Devices AD650 VFC has a full-scale frequency of 1MHz. If this device is used in an application where a resolution of 16 bits, or 1 part in 65,536 is desired, then the time required to convert the analog signal into a 16-bit digital word will be 65.536ms. Resolution of 18 bits, or 1 part in 262,144 will require a count time slightly greater than 0.262 seconds. In general, the required count time for an A/D conversion using a VFC is:

$$T_{\text{COUNT}} = N/FS_{\text{OUT}}$$

where N is the number of codes for a given resolution and  $FS_{\text{OUT}}$  is the VFC full-scale output frequency.

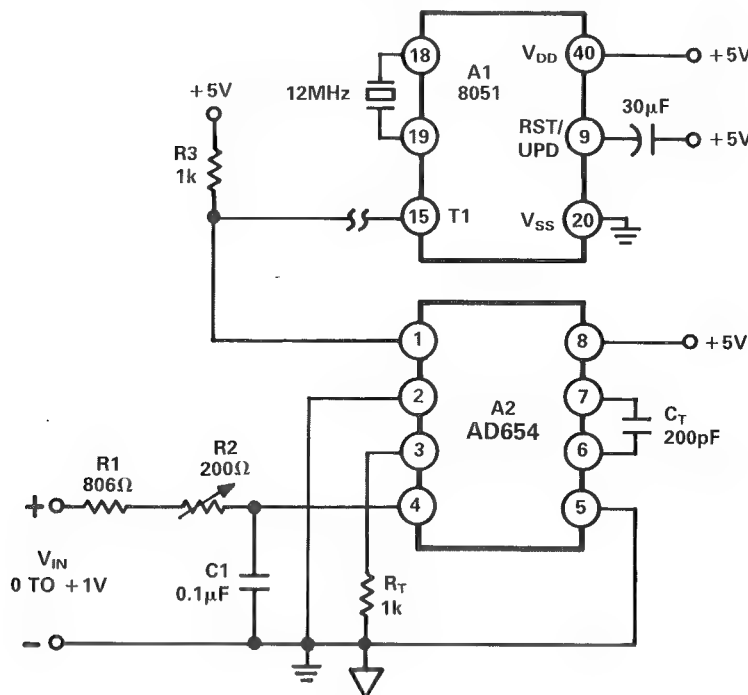
Although VFC-based A/D converters are slower than successive-approximation and flash converters, they are comparable in speed to integrating A/D's. VFC-based A/D converters are thus well suited for low frequency applications such as temperature and strain-gage measurements. The resolution that the VFC can provide in these types of applications offsets the relatively long count time required to acquire the digital word corresponding to the analog input value.

## PULSE COUNTING

One way to perform an analog-to-digital conversion using a VFC is to have a single-chip microcomputer count the number of pulses that occur in a fixed time period. The total number of pulses counted during this period is then proportional to the input voltage of the VFC. For example, if a 1V full-scale input produces a 100kHz signal from the VFC and the count period is 100ms, then the total full-scale count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5V.

The figure below shows the AD654 VFC output connected to the counter input, T1, of the Intel 8051 microcomputer. The AD654 is a low-cost, single-supply, monolithic VFC with a full-scale frequency of up to 500kHz. The 8051 is a member of the Intel MCS-51 family of 8-bit microcomputers whose family members differ mainly in their internal memory capabilities. In the following text, the term "8051" is used to generically refer to all members of the MCS-51 family.

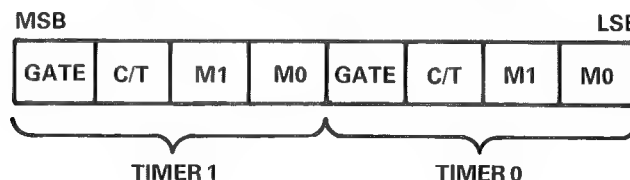
### AD654 PULSE COUNTER



The analog input of the AD654 is a 0 to +1V signal. The timing resistor and capacitor,  $R_t$  and  $C_t$ , are selected such that this 0 to +1V signal seen at Pin 4 results in a 0 to 500kHz output frequency. The pull-up resistor,  $R_3$ , ensures that the AD654 output meets the logic levels required at T1 of the 8051.

The 8051 has two 16-bit timer/event counters on-chip. These counters, Timer 0 and Timer 1, can be programmed independently to operate as 16-bit time-interval or event counters. The use of Timer 0 and Timer 1 is determined by two 8-bit registers, TMOD (timer mode) and TCON (timer control). The TMOD register is shown below:

### 8051 TMOD REGISTER





M1 and M0 are used to select the mode of each timer. Mode 01 configures the timer as a 16-bit time-interval or event counter. C/T is the timer or counter selector and is cleared for timer operation. In this application, Timer 0 was configured as the timer to provide the fixed time interval and Timer 1 was configured as the counter to count the pulses. Hereafter, the two timers will be referred to as Timer 0 and Counter 1. When running, Timer 0 increments at a rate equal to the external clock divided by twelve. Using a 12MHz crystal, this corresponds to once every microsecond. GATE is the gating control. When this bit is clear, timer/counter X is enabled whenever the TRx control bit found in the TCON register is set. The TRx bit is controlled via software. When the GATE bit is set, timer/counter X is enabled whenever the TRx bit is set and the signal level appearing at the INTx pin is high. Thus, when a GATE bit is clear that timer is controlled by software only, and when it is set that timer is controlled by a combination of software and hardware. In this application, the GATE bits are clear; however, in the next application they will be set.

Table 1 lists the software routine PLSECNT, which counts the number of falling edges that appear at T1 (the Counter 1 input) in a 50ms window. After Counter 1 is cleared, the value 15539 is loaded into Timer 0. Since Timer 0 is a 16-bit timer, the maximum possible count is 65535. With the Timer 0 interrupt enabled, a count of 65536 will cause a jump to the starting address (0BH) of the Timer 0 interrupt service program. With Timer 0 starting at 15539 and incrementing once every microsecond (based on a 12MHz clock), there will be 49997 counts or 49.997 ms before jumping to the service program. The 3 microsecond difference from 50ms is made up in the speed of the interrupt response. The interrupt response latency ranges from 3 to 7 microseconds when using a 12MHz. crystal. During this 50ms count period, control resides with the main program. Thus, the 8051 is not tied up while Counter 1 is counting for 50ms. After the interrupt service is reached, Counter 1 and Timer 0 are stopped and the contents of Counter 1 are moved into RAM, where it may be accessed at the user's convenience. Control is then returned to the main program for which the subroutine was written. With a maximum frequency of 500kHz and a count window of 50ms, the maximum value of Counter 1 will be 25,000. This provides resolution greater than 14 bits. Appropriate scaling from this 1V full-scale reference point may then be performed in software.

## 8051 PULSE COUNT ROUTINE

```

                                ORG    00H
                                AJMP   MAIN
PLSECNT  ORG    60H                ;PULSE COUNT SUBROUTINE
                                MOV     TMOD, #51H    ;Put Time 0 and Count 1 in Mode 01
                                MOV     TL1, #00H     ;Initialize Counter 1 Register
                                MOV     TH1, #00H
                                MOV     TL0, #0B3H    ;Load Time 0 With 15536 + 3.Will
                                MOV     TH0, #3CH     ;Ovflw After 50ms + 3μs Delay
                                SETB    PT0           ;Prioritize Time 0 Interrupt
                                SETB    ET0           ;Enable Time 0 Interrupt
                                SETB    EA           ;Enable Global Interrupt
                                SETB    TR0           ;Start Timer
                                SETB    TR1           ;Start Counter
                                RET                ;Return to Main Program

                                ORG    0BH            ;TIME 0 INTERRUPT SUBROUTINE
                                CLR     TR1           ;Stop Counter
                                CLR     TR0           ;Stop Timer
                                AJMP   COUNT

                                ORG    40H
COUNT   MOV     50H, TL1        ;Move Counter Contents Into RAM
                                MOV     51H, TH1
                                RETI                ;Return from Interrupt

                                ORG    100H
MAIN     -           -           ;Main Program for Which PLSECNT
                                ;Subroutine Was Written

```

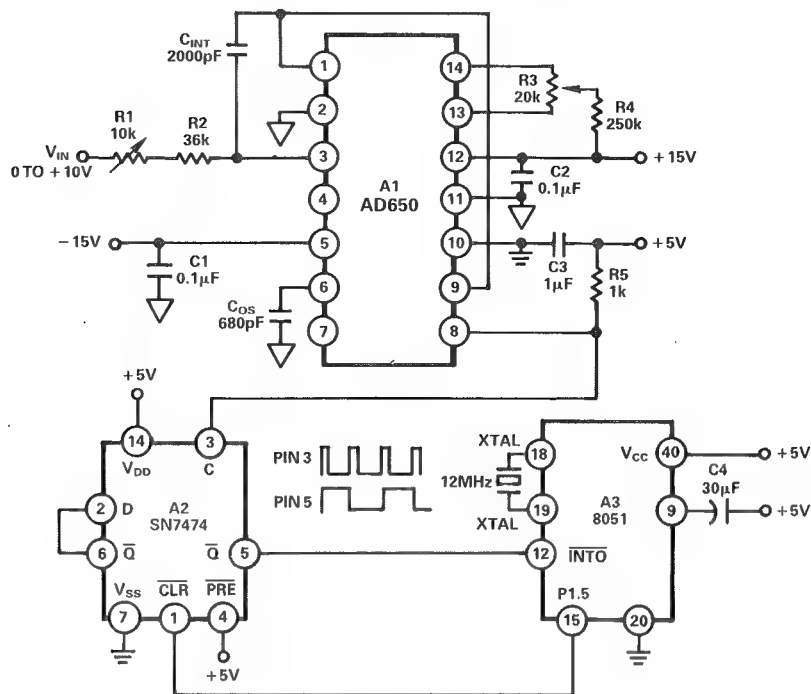
## PERIOD TIMING

Another method of performing analog-to-digital conversion using a VFC and a microcomputer is to have the computer time the period of the VFC output frequency. For example, an output frequency of 20kHz has a period of 40 microseconds. If a timer that is incremented once per microsecond is gated to this signal, a total count of 40 will result. An output frequency of 250Hz has a period of 4ms. The same timer gated to this periodic signal will then produce a total count of 4000.

One of the advantages of period timing over pulse counting is that the count window is dependent upon the output frequency of the VFC; in many cases the count window will be shorter for period timing than for pulse counting. This will be especially important in systems where a number of channels are being converted. Recall that in the Pulse Counter application, the count window was 50ms whether the output frequency was 50kHz or 50Hz. With Period Timing, the count window is the inverse of the output frequency. Thus, a 50kHz signal will have a count window of 20 microseconds while a 50Hz signal will have a count window of 20ms. In fact, it's not until the output frequency reaches 20Hz that the Period Timing count window is equal to the 50ms Pulse Counter count window.

The figure below illustrates the circuitry necessary to perform an A/D conversion via period timing using the AD650 VFC. The AD650 has a maximum full-scale frequency of 1MHz with a nonlinearity error of 0.1%. The AD650 is configured such that a 0 to +10V input will result in a 0 to 50kHz output. Because the AD650 output is made up of pulses, the 7474 flip-flop is used to convert these pulses into a square wave. The 7474 Pin 3 and Pin 5 waveforms sketched in the figure show that the width of either the high-level or low-level output appearing at Pin 5 is the same as one period of the AD650 output frequency. Note also that when Pin 1 on the 7474 is held low, Pin 5 is also held low.

### AD650 PERIOD TIMING



Recall that the INTO pin on the 8051 is the Timer 0 gate pin. When the GATE bit is set in the TMOD register, Timer 0 will run only when INTO is high and the TR0 bit in the TCON register has been set via software. Thus, connecting the Q output of the 7474 to the INTO pin on the 8051 will ensure the timer runs for one period of the AD650 frequency.

One problem that could arise is the TRO bit in software being set in the middle of a high-level edge at the INTO pin. In this case, Timer 0 would run for a fraction of a period rather than one full period. This is countered by tying the 8051 Port 1 Bit 5 (P1.5) pin to the 7474 CLR pin. When CLR is low and PRE is high, Q is low. When CLR and PRE are both high, Q changes state on every positive edge appearing at the clock pin. Setting P1.5 low, setting TRO (in software) and then setting P1.5 high will thus ensure that Timer 0 runs for one full period.

The software subroutine PCNT increments Timer 0 once per microsecond for one AD650 output frequency period. Note that there are two interrupt service programs, one for INTO and one for Timer 0. The INTO service program is accessed after a negative edge appears at the INTO pin (Pin 12) signifying the end of one period. The timer is then stopped and its contents are loaded into RAM to be later accessed.

## PERIOD TIMING ROUTINE

```

PCNT  ORG  00H
      AJMP  MAIN

      ORG  90H      ;PERIOD COUNTER SUBROUTINE
      MOV  TMOD, #05H ;Put Time 0 in Mode 1, Enable  $\overline{\text{INT0}}$  Pin
      CLR  P1.5      ;Initially Set  $\overline{\text{INT0}}$  Pin Low
      SETB IT0        ;Specify Edge Triggered Interrupt
      MOV  TLO, #00H  ;Initialize Timer
      MOV  TH0, #00H
      SETB EX0        ;Enable  $\overline{\text{INT0}}$  Interrupt
      SETB ET0        ;Enable Timer 0 Interrupt
      SETB EA        ;Enable All Interrupts
      SETB TR0        ;Start Timer
      SETB P1.5      ;Enable Gate  $\overline{\text{INT0}}$  Pin
      RET            ;Return to Main Program

      ORG  03H      ; $\overline{\text{INT0}}$  Subroutine Service Program
      CLR  TR0      ;Stop Timer
      CLR  EA        ;Disable Interrupts
      AJMP COUNT    ;Jump to Count

      ORG  0BH      ;TIMER 0 SUBROUTINE
                  SERVICE PROGRAM
      CLR  TR0      ;Stop Timer
      CLR  EA        ;Disable Interrupts
      AJMP OFLW     ;Jump to OFLW

OFLW  ORG  40H
      MOV  60H, #FF  ;Load RAM With Overflow
      MOV  61H, #FF  ;Value
      CLR  P1.5      ;Set  $\overline{\text{INT0}}$  Pin Low
      RETI          ;Return From Subroutine

COUNT ORG  50H
      MOV  60H, TH0  ;Load RAM with Counter Contents
      MOV  61H, TLO
      CLR  P1.5      ;Set  $\overline{\text{INT0}}$  Pin Low
      RETI          ;Return From Subroutine

MAIN  ORG  100H
      -      -      ;Main Program for Which
                  ;Subroutine Was Written

```

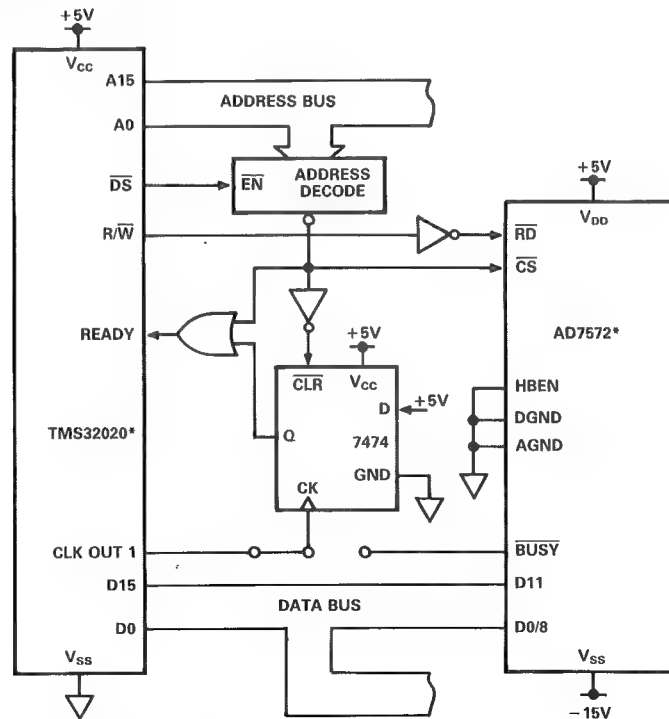
The Timer 0 service program serves to limit the count window to approximately 65.5ms. It is accessed when the contents of Timer 0 reach 65536. This will occur when the AD650 input voltage is approximately 3.05mV or the output frequency is approximately 15.26Hz. This service program then loads the overflow value 65535 into RAM. After both interrupt subroutines, and after initialization of the PCNT subroutine, control returns to the main program for which the subroutine was written. Thus the 8051 is not tied up while the period timing is occurring.

One possible source of error in this application is jitter, which is the range of variation in the period of the output frequency. This variation in period would result in a variation in the number of pulses counted from one period to the next. The magnitude of this error can be greatly reduced in software by taking the average of a number of period counts and using this average value for calculations.

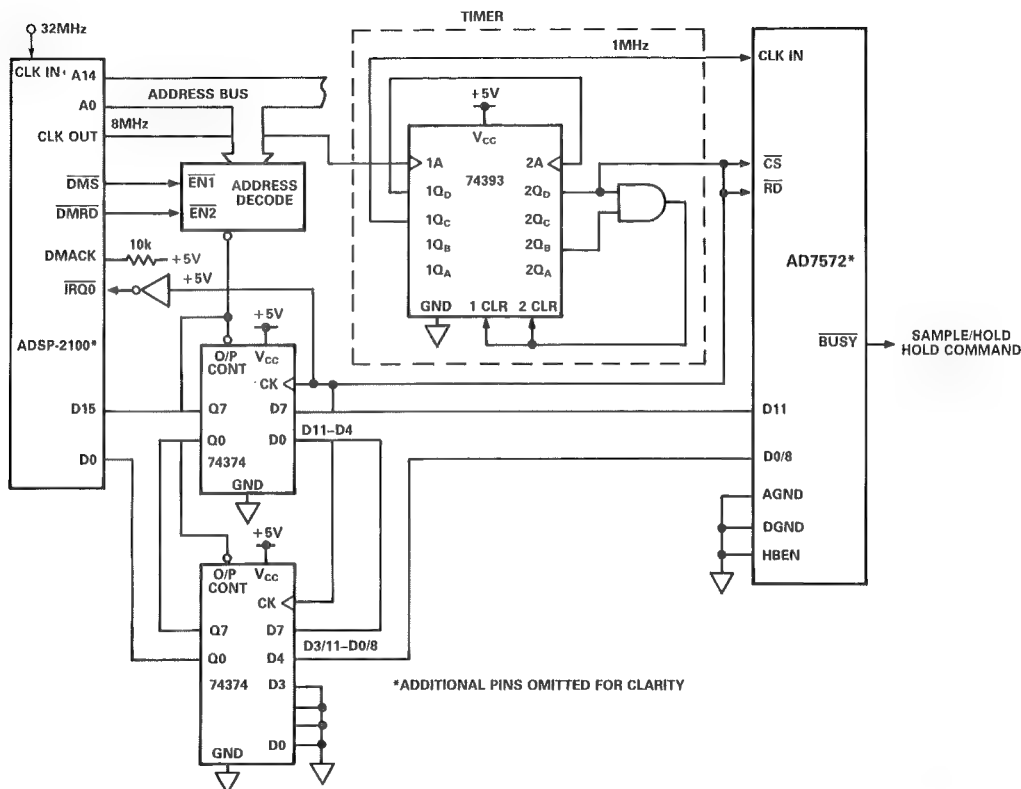
## INTERFACING TO HIGH-SPEED DSP PROCESSORS

More and more designers have discovered the tremendous power of digital signal processing on "real world" phenomena. Today, DSP techniques are used in a variety of applications such as telecommunications, secure communications, digital audio, and automotive. Most of these applications involve A/D and D/A converters whereby a signal is digitized, digital filtered, and then reconstructed with the D/A. The maximum input frequency to the A/D and the sampling interval (normally twice the maximum input frequency) will determine the conversion speed of the A/D. But what about the digital interface??? Many of the popular DSP processors such as the TMS320 series from Texas Instruments and the ADSP-2100 from Analog Devices require an extremely fast interface. Older converters are often too slow getting on or off the bus or have minimum pulse widths of several hundred nanoseconds. In these situations, placing the processor in a wait state extends read and write pulse widths as well as increases the time allotment for bus access and float delay.

IN A,PA (PA = PORT ADDRESS)

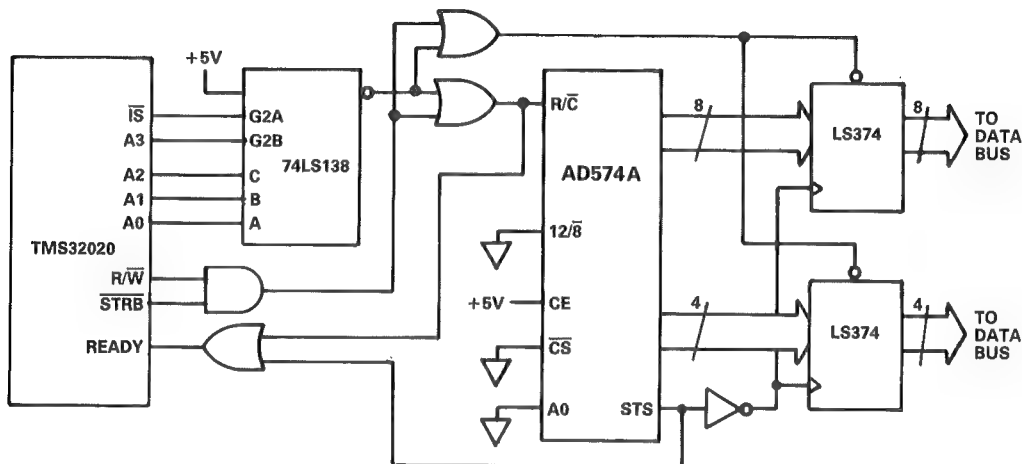


## AD7572/ADSP-2100 INTERFACE



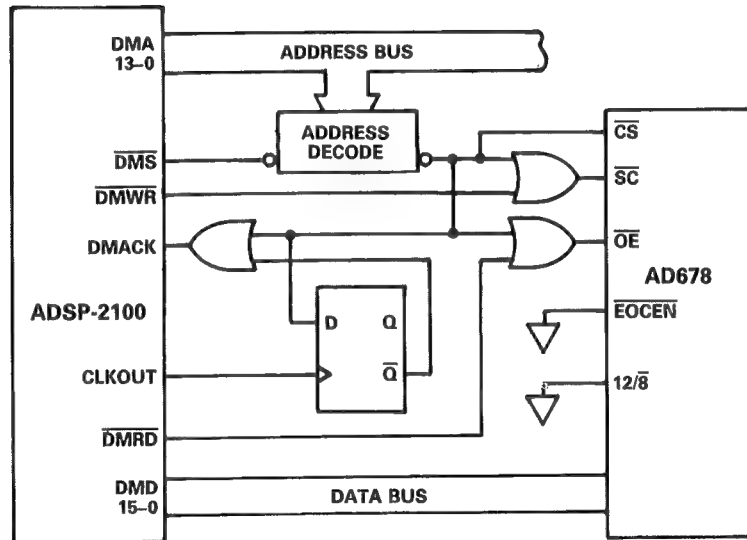
The industry standard AD574A 12-bit A/D converter can be used with the TMS32020. Using the Stand-Alone configuration previously described, this converter will interface to the processor with minimal hardware. The processor's  $\overline{\text{IS}}$  signal distinguishes the I/O space from the local program/data memory space and is used to enable a 74LS138 address decoder. The decoded port address is then gated with the  $\text{R}/\overline{\text{W}}$  and  $\overline{\text{STRB}}$  signals to provide the low-going R/C pulse to start conversion. Data is latched on the falling edge of STS and can be read by enabling the three states during a read operation.

## TMS32020 – AD574A INTERFACE



The AD678 12-bit Sampling A/D is shown interfaced to an ADSP-2100. With a clock frequency of 8MHz, and instruction execution in one 125ns cycle, the processor will support the AD678 data memory interface with a single wait state.

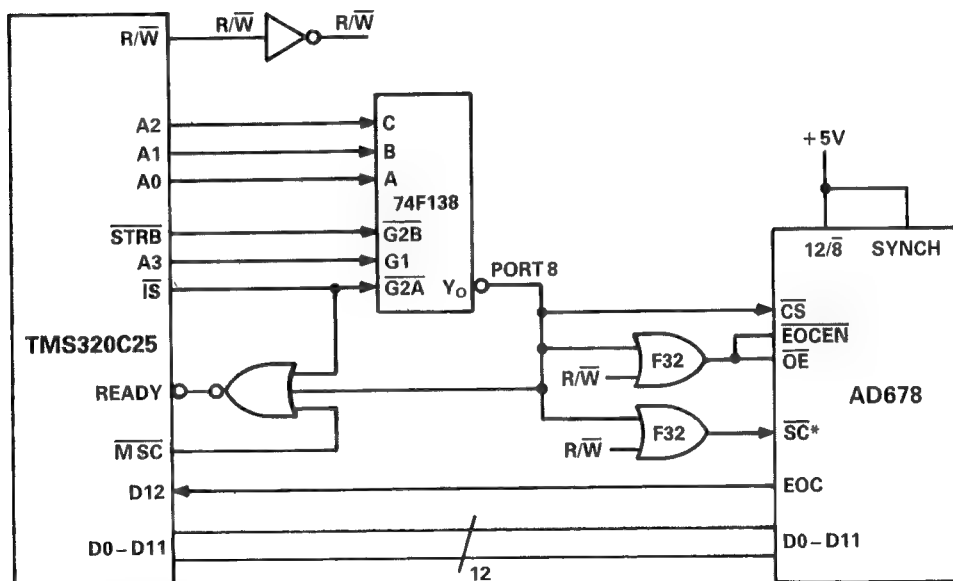
### ADSP-2100 – AD678 INTERFACE



At the beginning of the data memory access cycle, the processor provides a 14-bit address on the DMA bus. The  $\overline{\text{DMS}}$  signal is then asserted enabling a LOW address decode and the AD678  $\overline{\text{CS}}$ . The processor issues  $\overline{\text{DMWR}}$  which is gated with the decoded address to start conversion. The LOW decoded address is also OR'ed with the  $\overline{\text{Q}}$  output of a D flop-flop to pull DMACK LOW. This forces the ADSP-2100 into a wait state for 1 clock cycle. The rising edge of CLKOUT latches  $\overline{\text{Q}}$  HIGH bringing DMACK HIGH. 5 $\mu\text{s}$  later, the conversion is complete. The processor can now start a data memory access cycle to read data. For this cycle the  $\overline{\text{DMRD}}$  and LOW decoded address are OR'ed to generate  $\overline{\text{OE}}$  for the converter. Once again, a single wait state is inserted allowing data to be read from the bus.

In the following figure, the AD678 is mapped into the TMS320C25 I/O space. An OUT instruction to Port 8 initiates the conversion. EOC status and the conversion result are read with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from  $\overline{\text{IS}}$ , Port 8, and  $\overline{\text{MSC}}$ . This configuration supports processor clock speeds of 20MHz and is capable of supporting 40MHz operation if a NOP instruction follows each AD678 read.

### AD678 TO TMS320C25 INTERFACE



\*FOR ASYNCHRONOUS OPERATION, CONNECT SYNCH TO GROUND AND APPLY EXTERNAL TRIGGER TO SC.



# **SWITCHES & MUXES**





## ANALOG SWITCHES AND MULTIPLEXERS

1. Types of Switches
2. Analog Switch Technologies/Processes
3. Switch Design and Protection
4. Switch Specifications
5. Applications of CMOS Switches

### TYPES OF SWITCHES

The switching of analog signals is an essential function in a wide range of applications. There are a variety of switch types available to choose from.

The simplest of these is the mechanical switch. This offers the good electrical characteristics of low on-resistance and high off-isolation but cannot be controlled remotely.

The relay is an electro-mechanical device which offers the desirable electrical features of the mechanical switch plus remote control. It is used in different forms for both power control and analog signal switching. However the relay suffers from a number of problems which precludes its use in many applications. Principal among these are poor reliability, limited number of switch operations, deterioration of switch specifications with time, large size and weight, high power consumption and logic incompatibility.

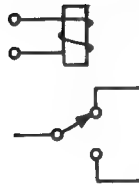
### SWITCH TYPES

#### MECHANICAL



TOGGLE, PUSH BUTTON, SLIDE, Etc.

#### ELECTRO-MECHANICAL



RELAYS (REED, MERCURY WETTED, Etc.)

#### SEMICONDUCTOR

SOLID STATE RELAYS – (HIGH CURRENT, HIGH VOLTAGE)

**ANALOG SWITCHES**

– (LOW CURRENT, LIMITED VOLTAGE, SIGNAL SWITCHING)

Semiconductor switches avoid most of these problems at the cost of higher on-resistance and lower off-isolation than relays. The main types of semiconductor switch are 'Solid State Relays' and 'ANALOG SWITCHES'. By common usage within the electronics industry the term 'Analog Switch' has largely assumed the meaning '(semiconductor) analog switch', although relays are often still used to switch analog signals in specific applications. The solid state relay exhibits low on-resistance but poor isolation and is used mainly for power control applications.

## SWITCH TYPES – ADVANTAGES AND DISADVANTAGES

TYPE	ADVANTAGE	DISADVANTAGE
MECHANICAL	<ul style="list-style-type: none"> <li>• Low <math>R_{ON}</math> (<math>&lt;0.1\Omega</math>)</li> <li>• No control power or circuitry</li> <li>• High off isolation</li> </ul>	<ul style="list-style-type: none"> <li>• <math>R_{ON}</math> degrades with time</li> <li>• No remote control</li> <li>• Limited number of switch actions (life)</li> <li>• Very slow</li> <li>• Often large and heavy</li> </ul>
ELECTRO-MECHANICAL	<ul style="list-style-type: none"> <li>• Low <math>R_{ON}</math></li> <li>• Remote control</li> <li>• High off isolation</li> </ul>	<ul style="list-style-type: none"> <li>• <math>R_{ON}</math> degrades with time</li> <li>• Exhibits "bounce"</li> <li>• Limited number of switch actions (life)</li> <li>• Slow</li> <li>• Often large and heavy</li> <li>• Not robust</li> </ul>
SOLID-STATE RELAYS	<ul style="list-style-type: none"> <li>• Low <math>R_{ON}</math></li> <li>• High reliability</li> <li>• High voltage operation</li> </ul>	<ul style="list-style-type: none"> <li>• High leakage</li> <li>• Unsuitable for signal switching</li> </ul>
ANALOG SWITCHES	<ul style="list-style-type: none"> <li>• Unlimited life</li> <li>• Small Size</li> <li>• Low cost per channel</li> <li>• Low power consumption</li> <li>• Fast (<math>&lt;200\text{ns}</math>)</li> <li>• No "bounce"</li> </ul>	<ul style="list-style-type: none"> <li>• High <math>R_{ON}</math></li> <li>• Leakage limits dc isolation</li> <li>• Limited signal voltage</li> <li>• <math>R_{ON}</math> varies with supply and temperature</li> <li>• Parasitic capacitance limits ac isolation</li> </ul>

Analog switches exhibit relatively high on-resistances—typically  $10\Omega$  to  $500\Omega$  depending on device type. The effect on system performance of these high resistances can be reduced to acceptable levels by buffering and other design techniques (see applications section). Bipolar transistors are rarely used as the signal switching elements in analog switches because they insert a base-emitter voltage drop into the signal path which is difficult to compensate for. Bipolar transistors are also unidirectional—they pass current in one direction only.

## PROCESSES FOR SEMICONDUCTOR ANALOG SWITCHES

TECHNOLOGY	PRODUCT	COMMENTS
Hybrid JFET	N-Channel JFET and hybrid driver	<ul style="list-style-type: none"> <li>• Very fast</li> <li>• <math>R_{ON} &lt; 10\Omega</math></li> <li>• Hybrid complexity and price</li> </ul>
BIFET	P-Channel JFET and integrated driver	<ul style="list-style-type: none"> <li>• Monolithic</li> <li>• <math>R_{ON}</math> rises near supply rail</li> </ul>
CMOS	N- and P-Channel MOS FETs and integrated driver	<ul style="list-style-type: none"> <li>• Lower power</li> <li>• Low cost</li> <li>• Wide signal range</li> <li>• Available junction isolated (JI) and diffusion isolated (DI)</li> </ul>

### ANALOG SWITCH TECHNOLOGIES & PROCESSES

The two principal types of analog switches are CMOS and JFET with CMOS being by far the most popular. Both types are bidirectional and can thus handle bipolar input signals. JFET switches exhibit constant on-resistance over the useable signal range. However this signal range is less than the power supply range by an amount equal to the pinch-off voltage of the FETs.

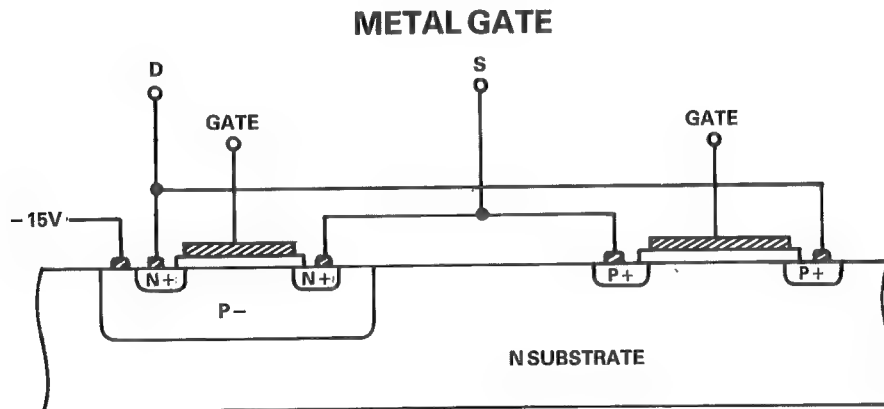
CMOS switches have a useable signal range which extends to the supply rails of the switch. They also use very little quiescent current. All the important parts of a fully integrated analog switch—fast logic interface, flexible level shifting and low leakage signal switches can easily be fabricated in CMOS. The problems associated with latch-up of first generation CMOS switches have been overcome and CMOS is now the technology of choice for analog switches.

CMOS wafer fabrication processes can be divided conveniently into two classes—Junction Isolated (JI) and Dielectrically Isolated (DI).

## JUNCTION ISOLATED (JI) CMOS

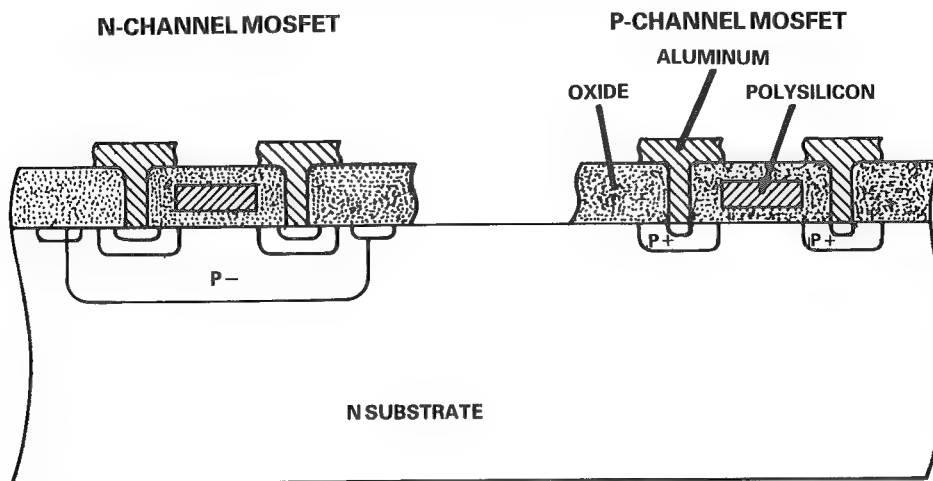
Junction Isolation relies on reverse biased p-n junctions to maintain isolation between individual elements of the switch circuit. The early problems with JI associated with latch-up caused by parasitic SCR action have been eliminated by careful layout and other design techniques.

### JUNCTION-ISOLATED (JI) CMOS SWITCHES



### JUNCTION-ISOLATED (JI) CMOS SWITCHES

#### POLYSILICON GATE (SELF ALIGNED)



The latest JI processes include poly-silicon gates in place of previous metal gates for fabricating the individual MOSFETs. These poly-gates have the distinct advantage that their position can be accurately self-aligned relative to the source and drain regions. This inherent self alignment allows the minimum feature size of the process to be reduced considerably, thus cutting chip area, and it also significantly reduces the gate-source and gate-drain capacitances. These reductions in capacitance allow smaller propagation delays and better isolation performance to be achieved.

## DIELECTRIC ISOLATION (DI) CMOS

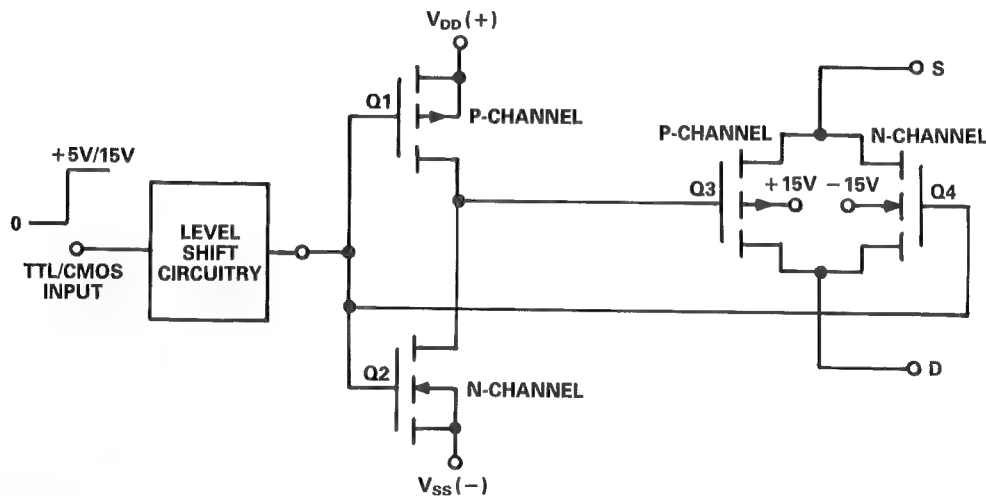
DI CMOS uses thin barriers of dielectric (usually silicon dioxide) to isolate the various chip elements. Forming of these dielectric barriers is expensive and pushes up the cost of the DI process. However DI can accommodate circuitry such as resistors and diodes which may be needed to protect the switch from excessive input overvoltages. These protection components often have to be added externally when using JI type switches.

The reverse biased junctions of JI, which have associated junction capacitances, contribute to the overall parasitic capacitance of the process. DI eliminates these contributions and thus exhibits lower parasitic capacitance.

## SWITCH DESIGN AND PROTECTION

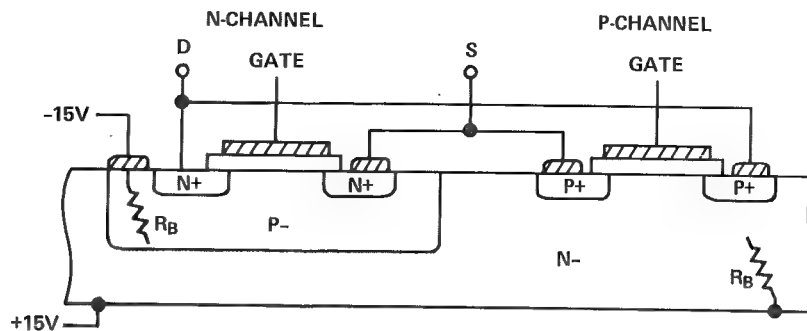
A typical CMOS analog switch IC design consists of a P-channel and an N-channel MOSFET connected in parallel to form a composite signal carrying switch. The gates of the P- and N-channel devices are driven in anti-phase by a push-pull CMOS stage which is in turn driven via level shifting circuitry from the input logic control voltage.

### BASIC CMOS SWITCH



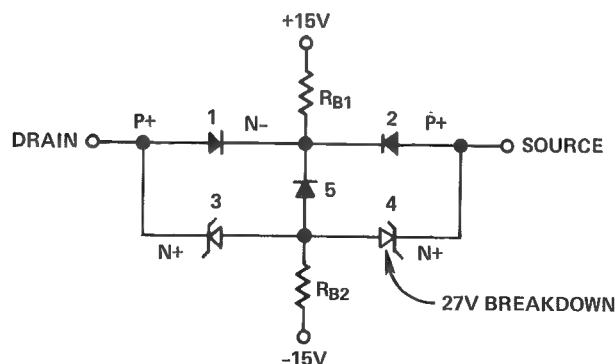
As previously mentioned, early JI CMOS switches suffered from one major drawback—they were prone to latch-up if a signal exceeded the supply voltage or if two signals applied to different switches on a single chip were greatly separated. The drawing below shows a cross section of a junction isolated CMOS switch.

### CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



Note that the sources of both the N- and the P-channel devices, as well as the drains of both devices, are tied together. The substrate of the P-channel device (n-region) is tied to V+ while the substrate of the resistances RB are the bulk resistance from substrate to the supply voltages. An equivalent circuit can now be drawn, as shown below.

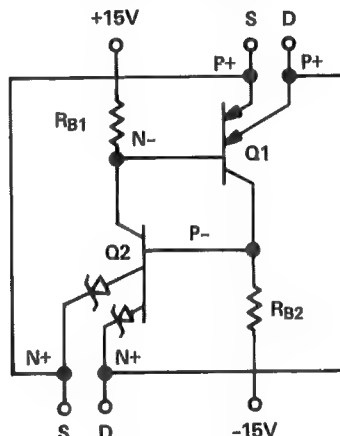
### DIODE EQUIVALENT CIRCUIT OF CMOS SWITCHING ELEMENT



If the analog voltage at either the S or the D terminals exceeds the power supply voltages, the parasitic transistors formed by the various diode junctions shown above are placed into a forward bias mode. These parasitic NPN and PNP transistors form the SCR circuit shown below.

## PARASITIC TRANSISTOR ACTION IN CMOS SWITCH

200%



For example, consider the case of a **SMALL** transient positive overvoltage applied to the drain terminal of a CMOS switch. Since the base of Q1 is normally at  $V_{DD}$ , it will conduct when its emitter voltage exceeds  $V_{DD}$  by a  $V_{BE}$  drop. The collector current of Q1 will increase to a level limited only by the  $V_{SS}$  and  $V_{DD}$  current limitations. Since the metal interconnection to the power supply terminal is normally designed to handle only small currents, the high currents flowing in the SCR can cause device failure.

This analysis is also valid for S and D terminals between and two switches. Thus, due to the latching nature of the parasitic SCR, a small transient overvoltage causes permanent 'latch-up'.

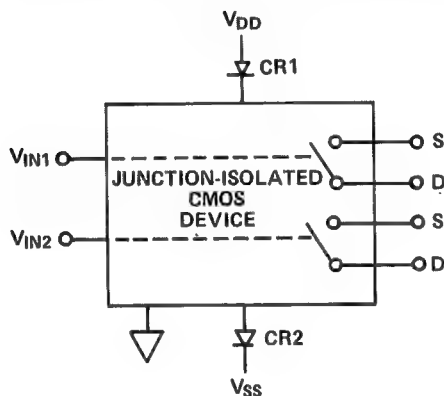
Modern junction isolated CMOS switch designs avoid the latch-up problem by reducing the values of  $R_{B1}$  and  $R_{B2}$  by means of low substrate contact resistances and optimization of IC layout such that transistors Q1 and Q2 of the parasitic SCR cannot turn on, thus preventing latch-up.

Precautions external to the switch may need to be taken to protect junction isolated CMOS switches from long periods or high levels of signal overvoltage in excess of the supply voltage. The two methods most commonly used, supply line protection and input current limiting protection, are described below.

Normally, the outputs of operational amplifiers are used as the voltage sources feeding the S and D terminals so the currents cannot exceed their output current limitations. The op amps may even be powered from the same supply as the CMOS device, but it is still possible, though much less likely with modern JI switch designs, for transient induced currents to destroy the CMOS switch.

## SUPPLY LINE PROTECTION

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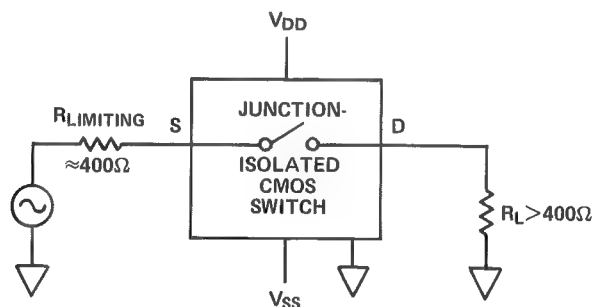


The above drawing illustrates a method of preventing the initial turn-on of the parasitic transistors. The diodes CR1 and CR2 are placed in series with the supply lines. If any S or D terminal exceeds either supply voltage CR1 or CR2 is reverse-biased and therefore no base drive is available to cause transistor turn-on. When this method is employed it is advised that each CMOS chip have its own protection diodes since if two switches use common protection diodes it is possible for the power supply current of one switch to furnish the required base current for parasitic transistors action on another device, even though the protection diode is reverse biased. The diodes used may be any general purpose device such as the 1N4148.

Even the diode protection scheme is not infallible. The internal diodes 3 and 4 in the equivalent circuit have a 27-30V reverse breakdown while diodes 1 and 2 have a 40-50V breakdown. This means that if one of the terminals, say "S", has a potential above +12V (assuming  $V_{SS} = -15V$ ), an avalanche current will run through the diode and  $R_{B2}$  to the -15V supply. Therefore the potential of the base of Q2 can be raised above the -15V line, turning on Q2, if the other terminal (emitter) is sufficiently negative. If +15V is applied to the terminal "S" (instead of +12V) then the potential on the base of Q2 will be -12V (because of the 27V zener), limiting potential on the other terminal to approximately -12.5V before Q2 turns on. The only way to protect against this condition is to have a 300-400 $\Omega$  resistor in series with terminals "S" and "D" as shown below. This will prevent burn-out.

## INPUT OVERVOLTAGE PROTECTION

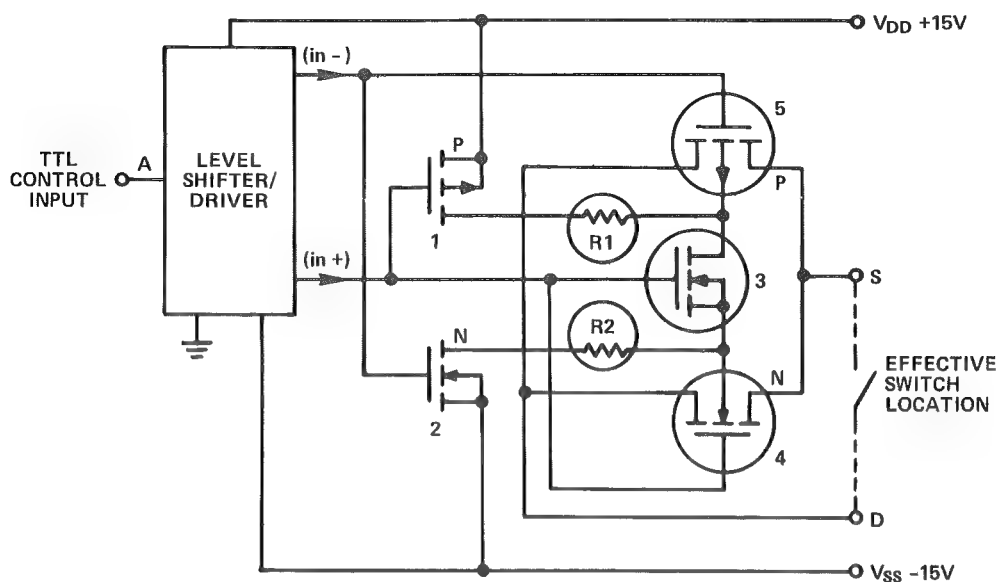
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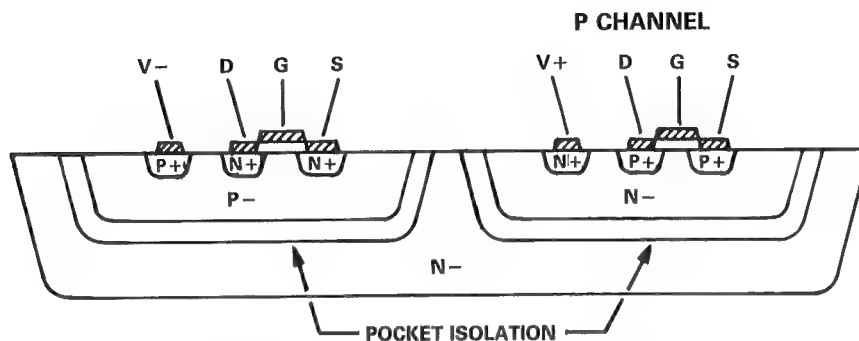
Unfortunately, the addition of this resistor increases the effective on-resistance of the switch.

DI CMOS processing allows the switch designer to eliminate problems of latch-up. Internally protected against over-voltage DI CMOS switches retain, or improve on, all the features of the JI CMOS switch.

## SCHEMATIC OF DI CMOS SWITCH



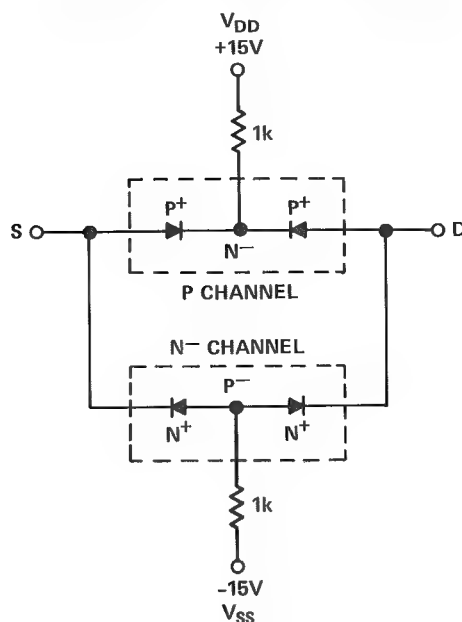
## DIELECTRICALLY-ISOLATED CMOS SWITCHES ELIMINATES LATCH-UP PROBLEMS



**DIELECTRIC-ISOLATION ELIMINATES THE  
HIGH BETA VERTICAL NPN AND THE LATERAL PNP.  
THIS ELIMINATES THE SCR PROBLEM.**

Note from the above schematic that the signal-carrying FETs are located in isolated pockets, eliminating parasitic junctions. Also the protection resistors (R1 and R2) are NOT in series with the signal path. This novel protection arrangement provides protection for signals up to  $\pm 25V$  past the supply rails with no increase in resistance.

## AD7590DI SERIES DIODE-EQUIVALENT CIRCUIT



### SWITCH SPECIFICATIONS

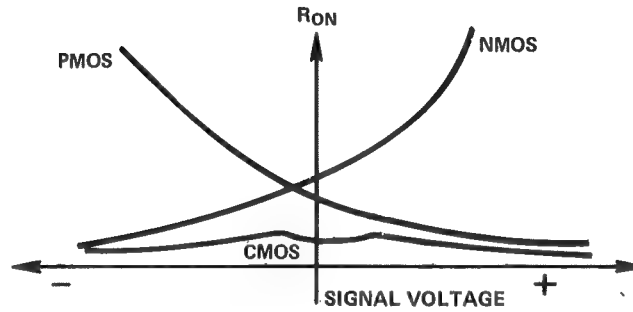
On resistance  $R_{DS(on)}$  is a prime specification of an analog switch. Its presence can insert attenuation, distortion, gain error and noise into the signal path. Techniques for minimizing some of the effects of excessive on-resistance are discussed in the applications section which follows. The on-resistance of CMOS switches is modulated by signal level, and also by supply voltage, as a result of the characteristics of its internal components.

For a fixed applied gate voltage the PMOS transistor exhibits a decreasing on-resistance for an increase in signal voltage. Conversely the NMOS transistor exhibits an increasing on-resistance for an increase in signal voltage. By connecting a PMOS transistor in parallel with an NMOS transistor of suitable relative size, a combination is formed which exhibits a relatively small change in on-resistance for different values of signal voltage.



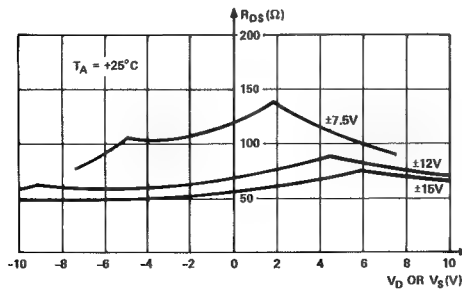
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## CMOS SWITCH $R_{ON}$ CHARACTERISTICS

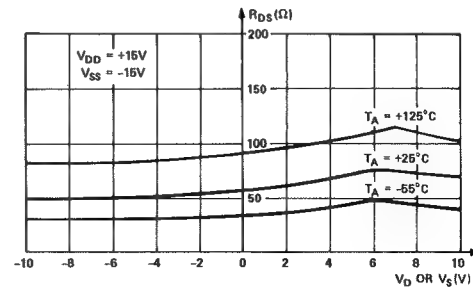


A drop in supply voltage causes a reduction in the enhancement of the two signal carrying transistors which increases their individual channel impedances. The on-resistance also has a positive temperature coefficient of approximately  $0.5\%/^{\circ}\text{C}$ .

## $R_{DS}$ AS A FUNCTION OF SWITCH VOLTAGE $V_D$ ( $V_S$ )



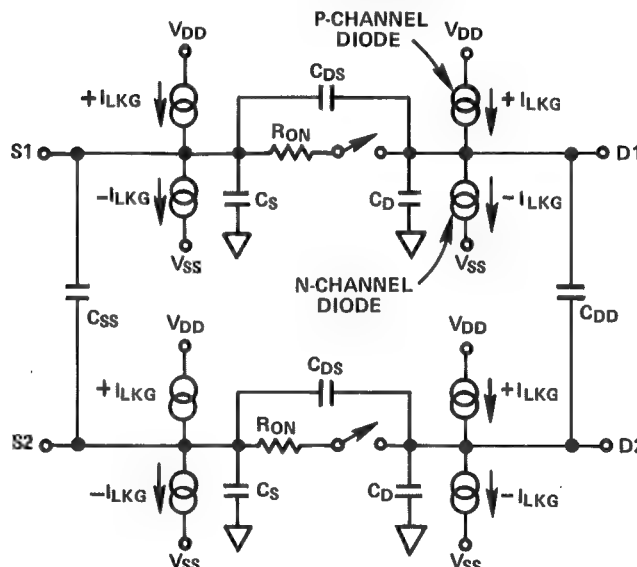
AT DIFFERENT POWER SUPPLIES



AT DIFFERENT TEMPERATURES

So far in this section we have only discussed switch on-resistance. Another dc specification which can introduce unacceptable errors into the user's system is leakage—which rises sharply with increase in temperature (silicon diode leakage doubles for every  $10^{\circ}\text{C}$  temperature increase)—and the high frequency performance of the switch is limited to a large extent by the effects of its parasitic capacitances. Both these error contributions are illustrated in the model below:

## EQUIVALENT CIRCUIT OF TWO ADJACENT SWITCHES



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Typical values for some of these specs are as follows:

## TYPICAL SWITCH SPECIFICATIONS (AD7590DI)

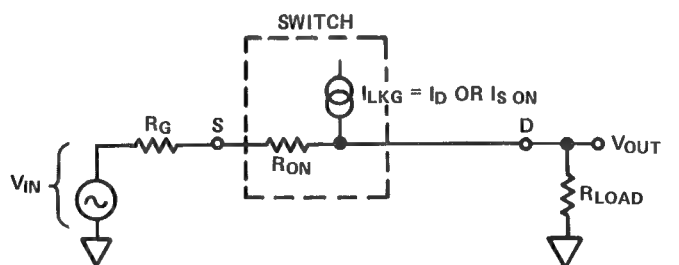
$R_{ON}$ :	60Ω typ, 90Ω max
$I_{LKG}$ :	0.5nA typ, 5nA max
$C_{DS}$ :	1pF typ
$C_D, C_S$ :	10pF typ (Off) 30pF typ (On)
$C_{DD}, C_{SS}$ :	0.5pF typ
$t_{ON}, t_{OFF}$ :	170ns, 340ns

The on-resistance and leakage current specs determine low frequency signal transmission accuracy. Their effects can only be properly analyzed if the external source and load impedances are known.

A low frequency model of a switch in the “ON” condition is shown below. It is obviously desirable to have a very high value of  $R_{LOAD}$  to minimize voltage divider effects with  $R_{ON}$ . Furthermore, low values of  $R_G$  are desirable, since switch leakage current will flow through this resistance, causing another error.

## MODEL OF SWITCH IN “ON” CONDITION

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$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[ \frac{R_{LOAD} (R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}} \right]$$

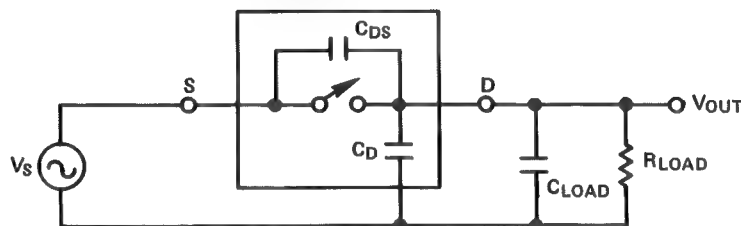
If  $R_G \rightarrow 0$ ,

$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] + I_{LKG} \left[ \frac{R_{LOAD} R_{ON}}{R_{LOAD} + R_{ON}} \right]$$

The primary concerns in using analog switches in ac applications are bandwidth and off isolation. These are not often specified on switch data sheets—with good reason. It is impossible for a manufacturer to test a switch for ac parameters without first knowing the load resistance and capacitance of the planned application circuit. The load resistance and capacitance directly affect the off-isolation of a switch, as is shown in the diagram below.

200%

## CIRCUIT MODEL FOR OFF ISOLATION



As an illustration of the effect of load impedance on isolation it is instructive to calculate the isolation, at 1MHz, or a fairly typical analog switch (having 0.5pF  $C_{DS}$  and 10pF  $C_{DOFF}$ ) with two different loads.

## LOAD AFFECTS OFF ISOLATION

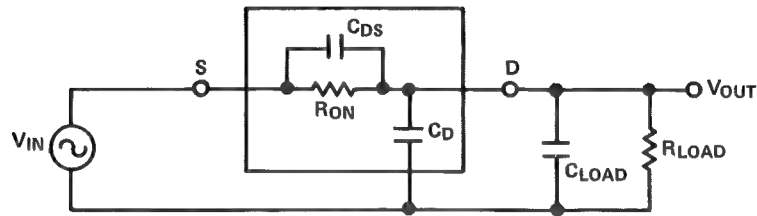
At 1MHz,  $C_{DS} = 1.0\text{pF}$ ,  $C_D = 10\text{pF}$ :

If  $R_L = 1\text{k}\Omega$       If  $R_L = 10\text{k}\Omega$   
 $C_L = 100\text{pF}$        $C_L = 10\text{pF}$

Off Isolation is -48dB      Off Isolation is -31dB

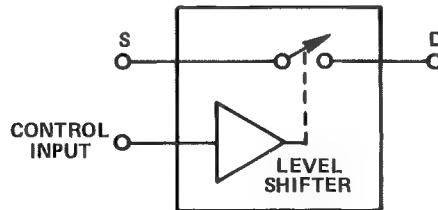
A similar analysis can be performed for the circuit model below in order to compute the available bandwidth, in the ON state, for a particular load.

## CIRCUIT MODEL FOR BANDWIDTH ANALYSIS



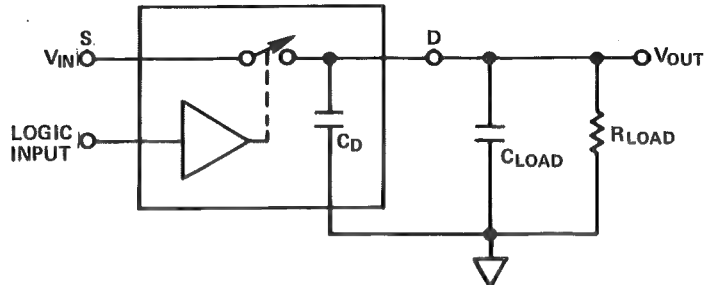
The turn-on and turn-off times are another pair of specifications which are important in analog switch applications. When a switch is commanded to change state there is a propagation delay in the level shifter/switch driver circuitry. These  $T_{ON}$  and  $T_{OFF}$  specifications are used to determine when a switch begins to operate, and whether multiple switches connected as a multiplexer will have make-before-break to break-before-make operation.

## PROPAGATION DELAY IN ANALOG SWITCH



Propagation delay should not be confused with settling time. The settling time of a switch, like its isolation and bandwidth, is a function of its load impedance (resistive and reactive). When a switch changes state the settling time for its output to settle within a given error band may be determined from the model illustrated.

## SETTLING TIME MODEL



$$\text{OFF-TO-ON: } t_{\text{SETT}} = t_{\text{ON}} + \frac{R_{\text{ON}} R_{\text{LOAD}}}{R_{\text{ON}} + R_{\text{LOAD}}} (C_{\text{LOAD}} + C_{\text{D}}) - \ln \frac{\% \text{ ERROR}}{100}$$

$$\text{ON-TO-OFF: } t_{\text{SETT}} = t_{\text{OFF}} + (R_{\text{LOAD}}) (C_{\text{LOAD}} + C_{\text{D}}) - \ln \frac{\% \text{ ERROR}}{100}$$

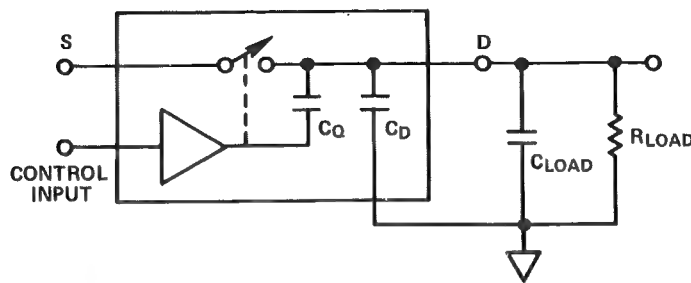
The  $\ln(\% \text{ error}/100)$  term can be recognized as the number of time constants required (with a single pole response) to reach a particular error band.

One additional specification related to transitions in analog switches is charge injection. Charge injection is the result of capacitive coupling through the gates of FET switches. Its effect is to create a voltage step on any output capacitance according to the formula:

$$\Delta V = Q_{\text{INJ}}/C_{\text{OUT}}$$

This is particularly annoying in sample-and-hold amplifiers (SHAs) since it introduces an error between the sample-and-hold modes.

## CHARGE INJECTION MODEL

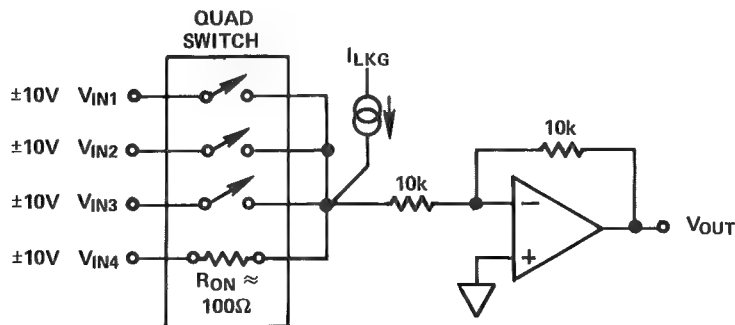


The resulting voltage pedestal error can be reduced, at the expense of settling time, by increasing the load capacitance. The AD7590DI switches feature typical charge injection of 40pF—which translates to a peak transient of 40mV with a 100pF load capacitor or 4mV with a 10,000pF capacitor. The length of the pulse depends on the load resistance.

## APPLYING ANALOG SWITCHES

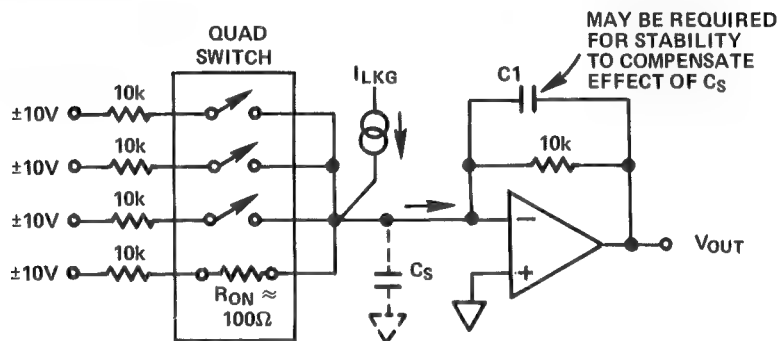
The most obvious application for an analog switch is to select one of several signals to be amplified. In the inverting amplifier shown below the resistance of the switch will obviously introduce a gain error.

## UNITY-GAIN INVERTER WITH SWITCHED INPUT



Since CMOS switches' on resistance varies somewhat with signal voltage, as well as with temperature and supply variations, it is evident that this circuit will introduce nonlinearity. By placing the switch at the summing junction the voltage variation at the switch, and hence the nonlinearity, can be reduced—at the cost of an extra input resistor per channel.

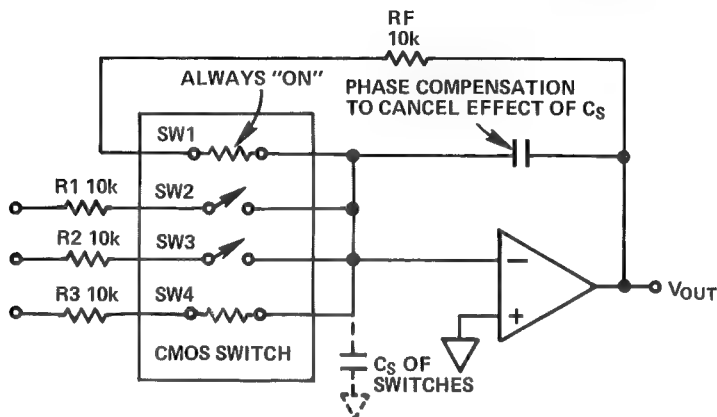
## CONNECTING SWITCH AT THE SUMMING POINT



A disadvantage of this circuit is that the switch capacitance appears at the summing junction and may destabilize the amplifier. The feedback capacitor necessary to prevent this will limit overall bandwidth.

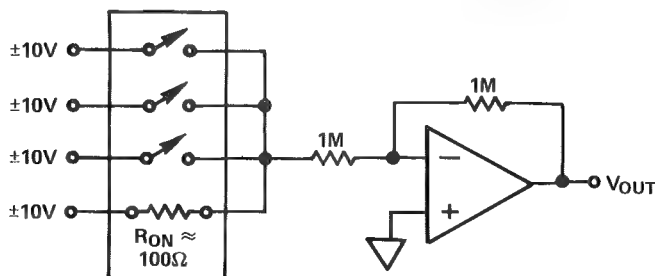
Variations of  $R_{ON}$  with temperature and supply may be compensated by connecting a closed analog switch, of the same type as is used in the multiplexer, in the feedback path. This will track the resistance of the multiplexer and reduce errors from these causes, but, of course, uses up one of the multiplexer channels and the problems of summing-point capacitance will remain.

## SWITCH IN SERIES WITH FEEDBACK RESISTOR COMPENSATES GAIN



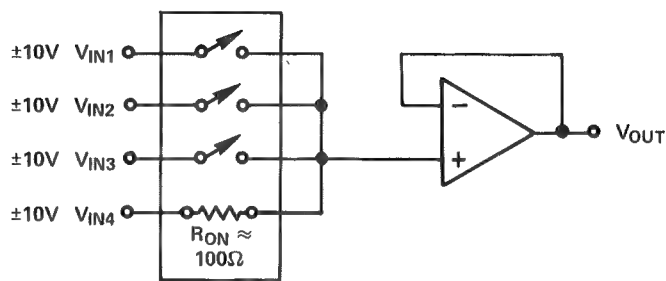
Of course the effect of switch resistance can be reduced by making the circuit resistances larger—at the cost of increased noise and of increased dc offsets due to switch leakage and amplifier bias current flowing in the extra resistance.

## USING LARGER VALUES OF RESISTANCE



It is much better to follow a switch with a noninverting amplifier which raises the load impedance to a very high level. If an inverted output is required a separate inverter may follow it.

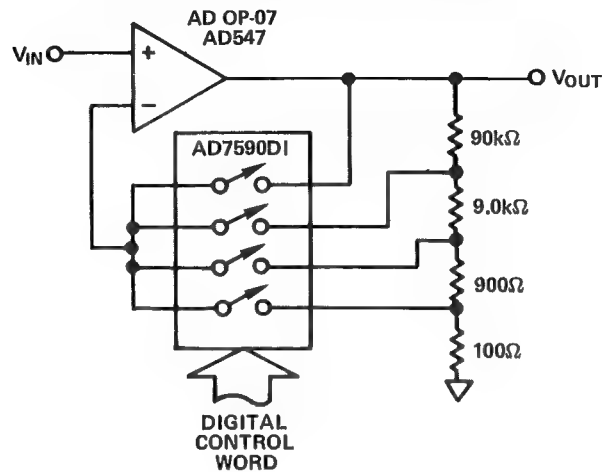
## NONINVERTING SOLUTION



With CMOS switches all are open if the switch power is off, but with JFET (and this includes BIFET switches) they are all on—which can cause problems both for the switch and the signal sources connected to it.

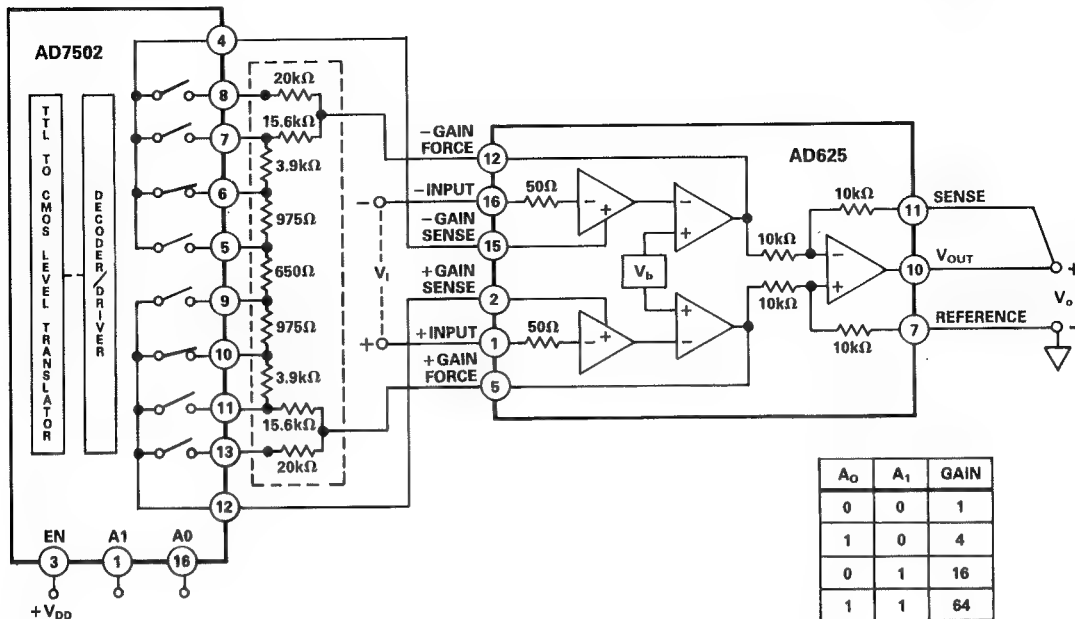
An analog switch may be used to switch the gain of an amplifier by selecting voltage taps on a resistive attenuator in the feedback path. This circuit is capable of high accuracy since only the amplifier bias current flows in the analog switch. The AD7590 is a good choice for such an application since it has make-before-break action, which prevents the amplifier from running open-loop during gain switching.

## SWITCHED-GAIN AMPLIFIER



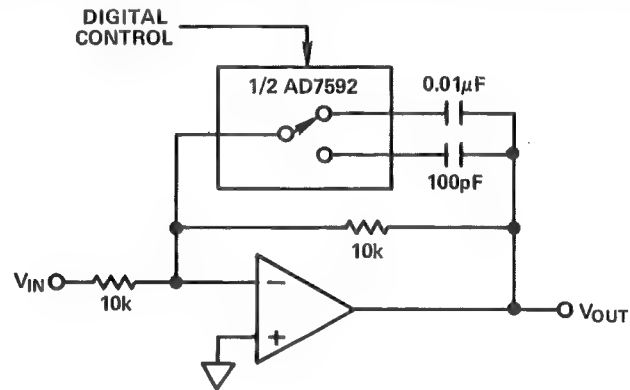
Early monolithic instrumentation amplifiers, such as the AD524 and AD624, were configured so that accurate gain switching required switches with  $R_{ON}$  of no more than a few milliohms. This is, of course, impossible to achieve with semiconductor analog switches. The AD625, however, was specifically designed so that its gain could be programmed with such switches and uses the principle shown in the diagram above—the feedback goes to a very high impedance and so the switch  $R_{ON}$  is unimportant.

## THE AD625 INSTRUMENTATION AMPLIFIER, UNLIKE EARLIER TYPES, HAS BEEN DESIGNED TO ALLOW GAIN PROGRAMMING WITH ANALOG SWITCHES.



Filter time constants can also be controlled by analog switches. In the circuit shown the low pass cutoff frequency is changed by selecting one of two capacitors. The circuit is useful in applications where a coarse reading is to be taken, and high-frequency noise can be tolerated, and a higher resolution reading must also be taken, where noise cannot be allowed. The technique is not limited to low-pass filters—any filter function may be adapted to this basic idea of switching capacitors to alter frequency response.

### DIGITALLY CONTROLLED LOW-PASS FILTER



**NO NOISE IS GOOD NOISE**





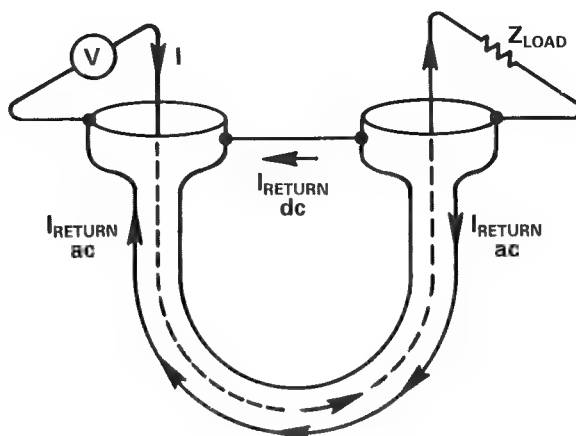
## NO NOISE IS GOOD NOISE : A DOWN TO EARTH DISCUSSION OF GROUND AND NOISE MANAGEMENT

In precision analog circuits, noise management and ground management techniques must be rationally applied to obtain the desired signal to noise ratio. Problems arising from improper grounding or shielding become more critical at higher resolutions and wider bandwidths. When analyzing interference of this type, the designer must carefully consider where noise signals originate and what is the best return path for them.

...Principle: Think—Where will the currents flow?

This may seem fairly obvious, but all of us tend to think of the currents we're interested in as flowing "out" of some place, and "through" some other place, but often neglect to worry about how the current will find its way back to its original source.

Current will return to its source via the path of least impedance. Wiring impedance is a combination of resistance and inductance. As frequencies move away from dc, the inductance becomes the dominating factor. Minimum inductance means minimum area enclosed by current flow. For example, consider the cable shown below.



If  $V$  is a dc source, then the current will flow through the load and return to the source through the short wire connecting the two ends. This is the least resistive path. However, as  $V$  increases in frequency, more and more current will flow through the load and return via the outer conductor of the coaxial cable to the source. This is the least inductive path because the current encloses less area than if it had flowed from one cable end to the other.

Noise will continue to find its way into our circuits unless we understand the characteristics of both the noise and the circuit that it is invading. For a complete analysis, we could solve the loop and node equations of the circuit, including wire resistance, stray capacitance and mutual coupling. However, since this level of detail is either impractical or impossible for many circuits, we will examine some common situations to develop a few guidelines that will be useful in most applications.

## SOURCES OF NOISE

- Transmitted Noise
- Intrinsic Noise
- Interference Noise

Any electronic system contains many sources of noise. Three basic forms in which it appears are: transmitted noise—received with the original signal and indistinguishable from it, intrinsic noise—such as thermal noise, shot noise, and popcorn noise (intrinsic noise is covered in section three under op amp specifications), and interference noise—picked up from outside the circuit. This last type of noise may be coupled in from other electrical systems such as switching power supplies, nearby digital circuits or even another segment of the same analog signal path. In this section we will concentrate on eliminating interference noise, since it is the only type that can be influenced by choices of wiring, layout and shielding.

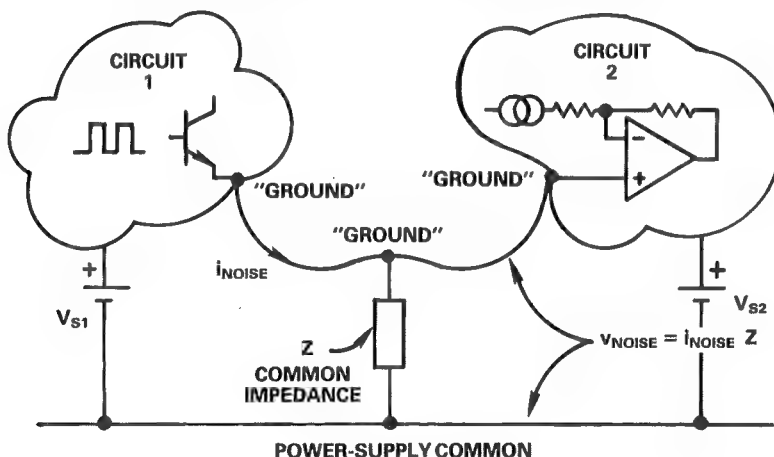
## INTERFERENCE NOISE CAN BE COUPLED INTO A CIRCUIT IN SEVERAL DIFFERENT WAYS:

- Conductive Coupling (Direct Contact)
- Capacitive Coupling (Electric)
- Inductive Coupling (Magnetic)
- Radiative Coupling (Electromagnetic)

### CONDUCTIVE COUPLING

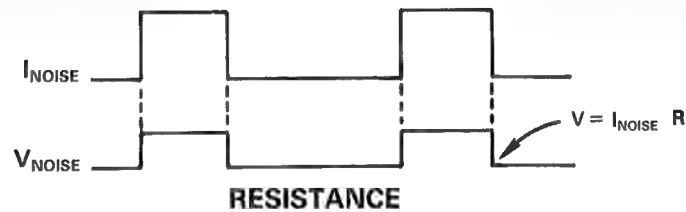
Conductively coupled noise occurs when a direct electrical contact, or leakage path, to an interference source is present. The diagram below shows the basic configuration which might occur when a digital logic circuit and an op amp's reference terminal are both connected to a "ground" point having tangible impedance to the power supply return terminal. The return current of circuit 1 will develop a voltage,  $V_{noise}$ , across impedance  $Z$  which will appear as a noise signal to circuit 2.

### HOW NOISE IS DEVELOPED BY A COMMON CIRCUIT IMPEDANCE



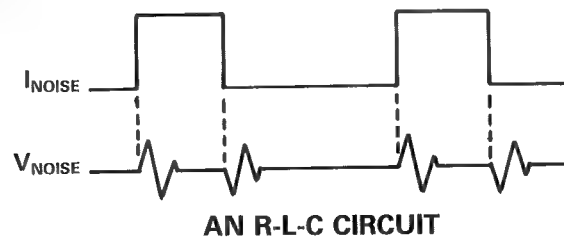
The characteristics of the noise are determined by both the noise source and the impedance of the return path  $Z$ . For example, if  $Z$  is purely resistive, the noise voltage will be proportional to the noise current and of similar shape.

## NOISE EFFECTS IN A COMMON IMPEDANCE



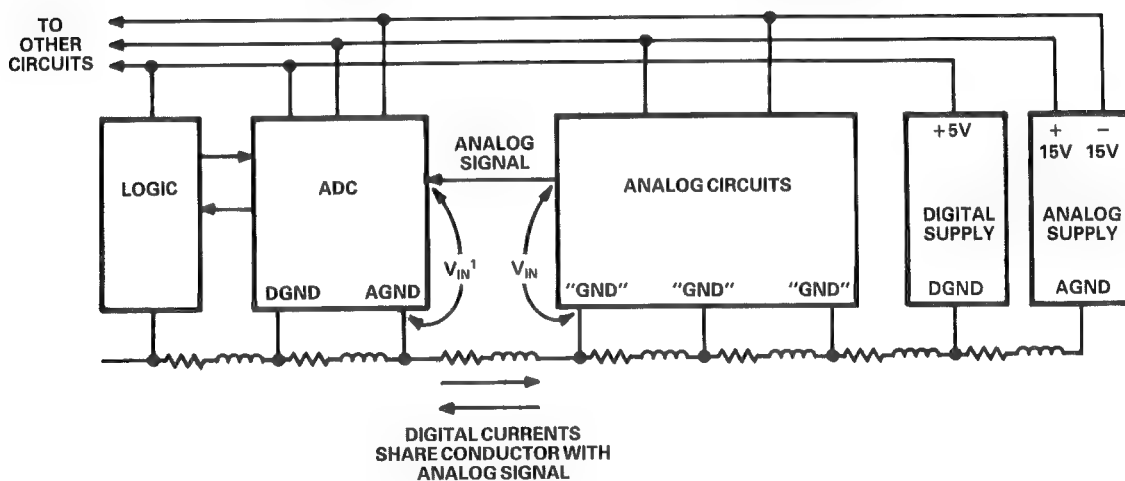
If  $Z$  is inductive and capacitive as well as resistive, the response is that of a damped second order system. That is, an impulse of current causes an exponentially decaying sinusoid of characteristic (resonant) frequency. An identifying characteristic of conductive, or common impedance, coupling is a non-zero average value for the noise waveform.

## NOISE EFFECTS IN A COMMON IMPEDANCE

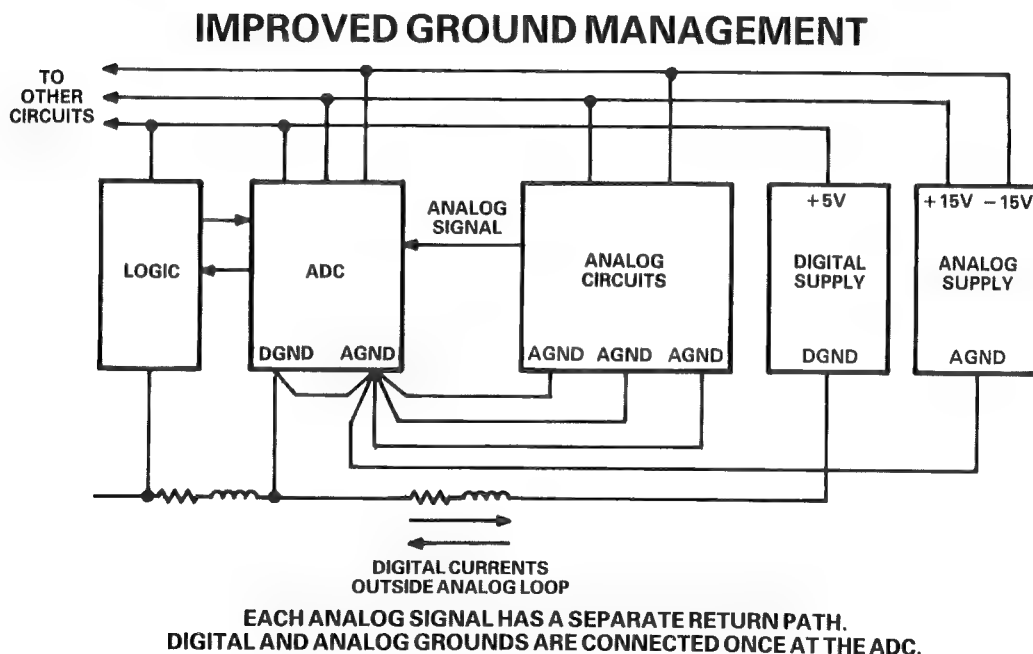


The example above is a simplified representation of the class of grounding problems that often occur in high resolution data acquisition systems. The figure below shows a typical arrangement of components in a single channel data acquisition system. The power and ground distribution systems are shown with their equivalent resistive and inductive components. This representation emphasises the complexity of the ground distribution network and its implications with respect to noise. Digital or other rapidly changing signals impressed on this "daisychain" ground will clearly affect the instantaneous potential of the separate ground nodes, and this causes errors.

## A COMMON GROUND ARRANGEMENT

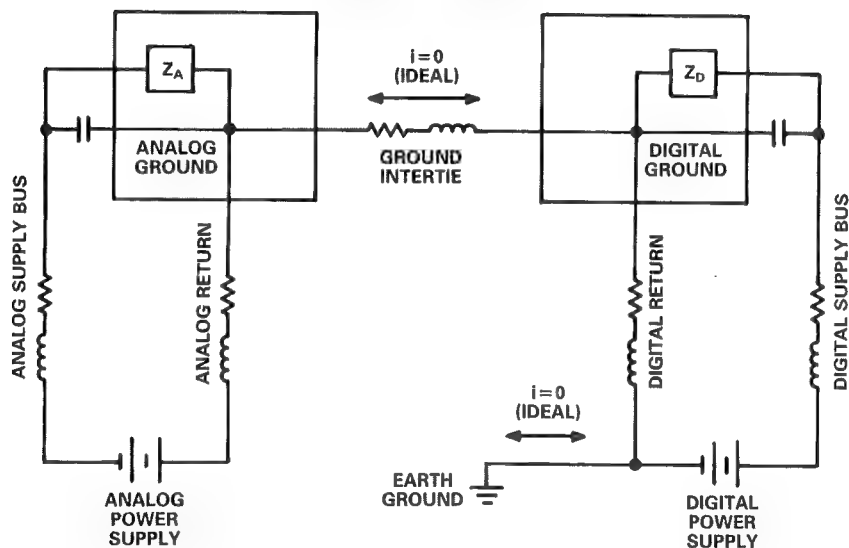


You can improve the situation greatly if a single analog reference is established. This arrangement is often called a star ground system. All analog signals should return to the ground reference via separate pc board tracks or wires. In small systems using only one converter, it is usually desirable to arrange circuit topology so that the analog ground reference point and the analog ground connection of the ADC are one and the same.



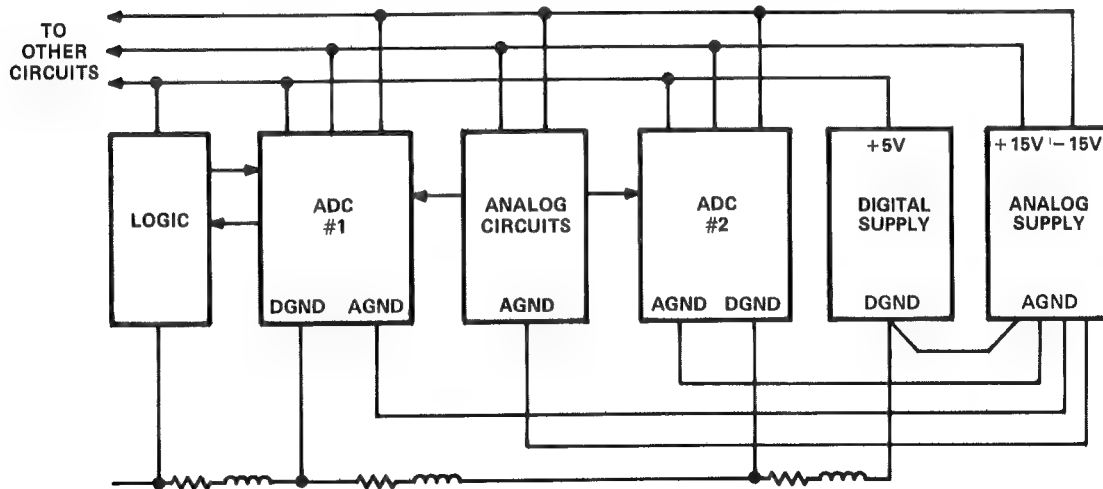
The most effective way to minimize conductive interference is to separate the analog signal return from the digital signal return. The figure below shows a system that has only one analog ground star point and one digital ground point. These two grounds are connected together via one heavy gauge connection that we shall refer to as a ground intertie. This limits the voltage difference between the two. The analog and digital supplies are NOT tied together at a common point in the supply rack. The only direct connection between the two grounds is the intertie. An additional connection would create a ground loop that would allow the noisy digital ground currents to flow through the analog system. Ideally, the analog and digital signal currents will flow through their returns to the appropriate source and no current will flow in the intertie or earth ground.

### ISOLATED SUPPLIES ELIMINATE GROUND LOOPS



For a single converter system, the tie between analog and digital ground should occur right at the chip. In multiple converter systems, it is more difficult to arrange a single point ground. In such applications, the tie between analog and digital ground should occur once at the power supply common, not at each individual chip. If the power supply is located at an inconvenient or distant location, then another point may be chosen at which to connect the analog and digital grounds. The most important design rules to follow are: provide a separate return for each analog signal through the common analog ground; provide a return for each digital signal through the digital ground; connect the analog ground to the digital ground at only one point and reference everything to that point.

## GROUND MANAGEMENT FOR MULTI-CONVERTER SYSTEMS

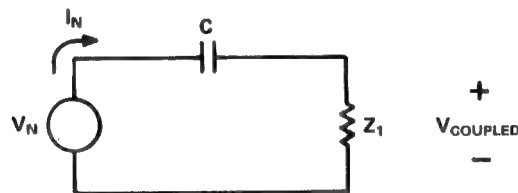


EACH ANALOG SIGNAL HAS A SEPARATE RETURN TO THE SUPPLY. DIGITAL AND ANALOG GROUNDS ARE CONNECTED ONCE AT THE SUPPLIES.

## CAPACITIVE COUPLING

Capacitive coupling of noise occurs when an electric field couples a noise source to the desired signal. All capacitive coupling may be represented by a voltage noise source, a coupling capacitor, and a circuit impedance.

## CAPACITIVE COUPLING EQUIVALENT CIRCUIT

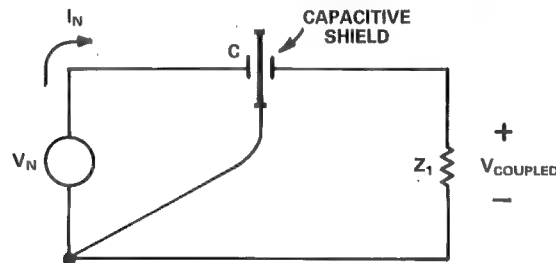


$Z_1 = \text{CIRCUIT IMPEDANCE}$   
 $Z_2 = 1/j\omega C$

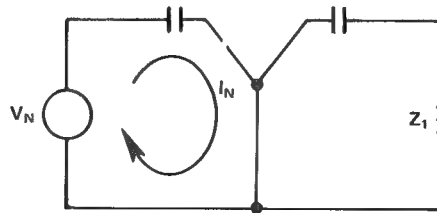
$$V_{\text{COUPLED}} = V_N \left( \frac{Z_1}{Z_1 + Z_2} \right)$$

Several steps may be taken to reduce the coupled voltage. Reducing the capacitance ( $C$ ), the noise voltage ( $V_N$ ), the frequency of the noise ( $F_N$ ), or the circuit impedance ( $Z_1$ ) will all result in a smaller coupled voltage. Unfortunately, some of these options may not be possible. Another possibility is to filter the noise at the load. This is only practical if the frequency of the noise is substantially different than that of the signal. Possibly the best solution is to use a capacitive shield.

### CAPACITIVE SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD

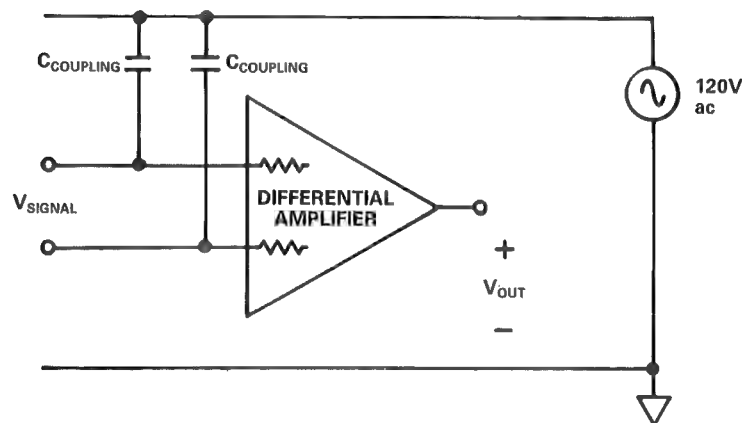


### EQUIVALENT CIRCUIT ILLUSTRATES HOW A CAPACITIVE SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH $Z_1$



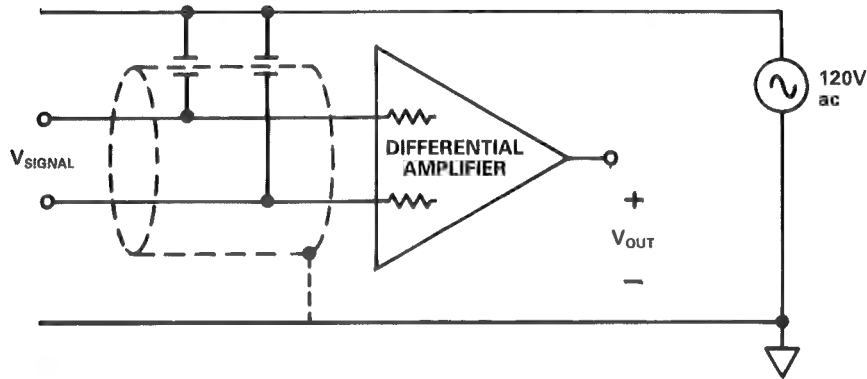
For a capacitive shield to be effective, the shield must be placed in the proper location and be connected correctly. Shields should be located between the two coupled surfaces so as to interrupt the coupling electric field. They should be connected at only one point to allow the noise currents to bypass the signal circuit as they return to their source. Capacitive shields should never be connected to more than one node, nor should they ever be left floating. An incorrectly implemented shield can be worse than no shield at all.

### CAPACITIVE COUPLING



One example of capacitive coupling is crosstalk. If the signal cable is twisted pair, then the two coupling capacitances should be equivalent. Balanced capacitance makes the interference common mode. Unbalanced capacitance results in both normal and common mode interference. Using twisted pair will greatly improve the situation by taking advantage of the differential amplifier's common mode rejection.

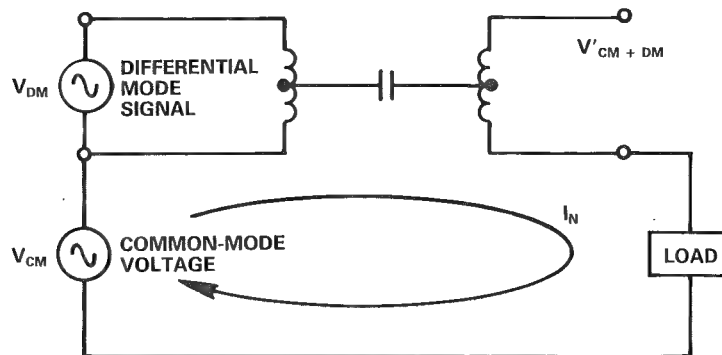
### CAPACITIVE SHIELD INTERCEPTS NOISE CURRENTS AND RETURNS THEM TO THEIR SOURCE



Further improvement is obtained by using a shield. Note that the shield doesn't eliminate the noise current, it simply re-routes it so as not to interfere with the signal.

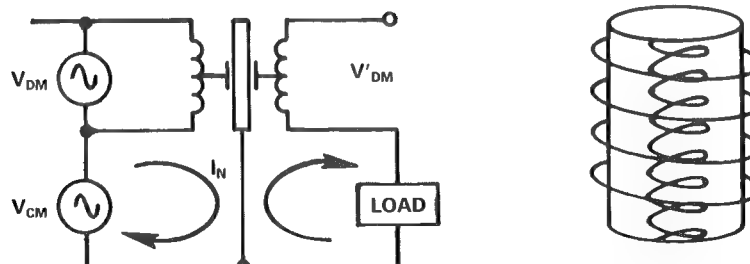
Effective shielding may be further illustrated by considering a typical transformer. Capacitive coupling may occur between the coils unless the exposed metal between primary and secondary is shielded.

### CAPACITIVE COUPLING OF TRANSFORMERS



The desired differential signal is magnetically coupled by the transformer. However, the parasitic capacitance allows the common mode signal to pass from the primary to the secondary. Consider an isolation amplifier that uses transformers to isolate a patient from a potentially dangerous voltage. Coupling of this voltage could result in serious consequences. Note how a shield may be used effectively to intercept the coupled signal and return it to its source.

### TRANSFORMER CAPACITIVE SHIELDING





# UNDESIED, CAPACITIVELY COUPLED SIGNALS ARE ONE OF THE MOST COMMON SOURCES OF INTERFERENCE.

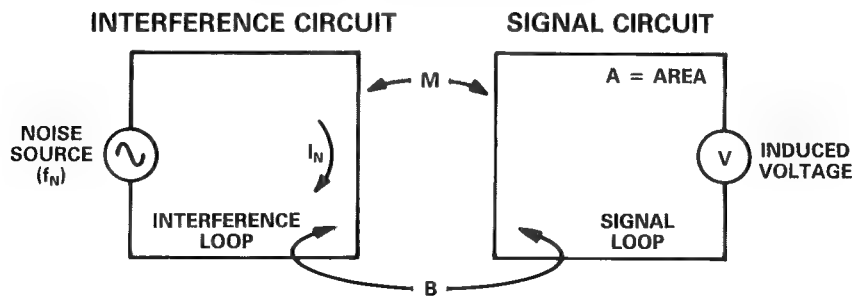
SOME IDENTIFYING CHARACTERISTICS TO LOOK FOR ARE:

- Metal surfaces which are unshielded or electrically floating.
- High noise voltage relative to signal voltage
- High impedance signal circuit
- If the noise is affected by the location of nonmagnetic materials such as cable or people, then it is more than likely capacitively coupled.

## INDUCTIVE COUPLING

Magnetic flux can couple between a signal circuit and an interference circuit and cause an undesired voltage to be induced in the signal circuit. This is inductive coupling. The figure below illustrates the basic principles.

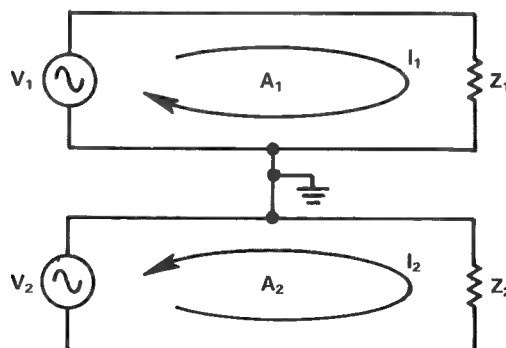
### BASIC PRINCIPLES OF INDUCTIVE COUPLING



$M$  = MUTUAL INDUCTANCE  
 $B$  = MAGNETIC FLUX DENSITY  
 $A$  = AREA OF SIGNAL LOOP  
 $\omega_N = 2\pi f_N$  = FREQUENCY OF NOISE SOURCE  
 $V$  = INDUCED VOLTAGE =  $\omega_N M I_N = \omega_N A B$

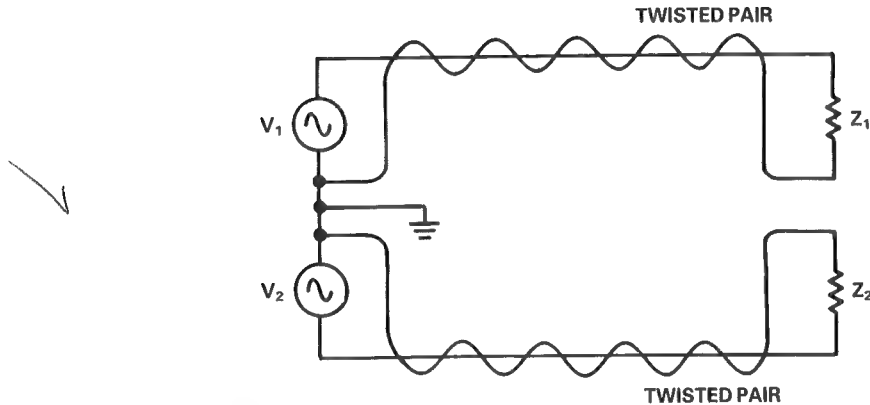
The induced voltage may be decreased by reducing any of the terms in the above equations, namely:  $f_N$ ,  $M$ ,  $B$ ,  $I$ , or  $A$ . As with any coupling, minimizing ALL of the contributing factors is not possible. In some cases the noise frequency can be reduced. For example, if the interference is digital, increasing the pulse rise time will decrease the noise bandwidth. If this is not practical, another alternative is to decrease the magnetic flux density or mutual inductance. This may be accomplished by increasing the separation between the two loops or by using magnetic shielding. Running the loops perpendicular to each other will also help eliminate magnetic coupling. One of the best, and often easiest to implement, solutions is to reduce the loop areas.

### SINGLE POINT GROUND AND POOR LAYOUT RESULTS IN EXCESSIVE LOOP AREAS



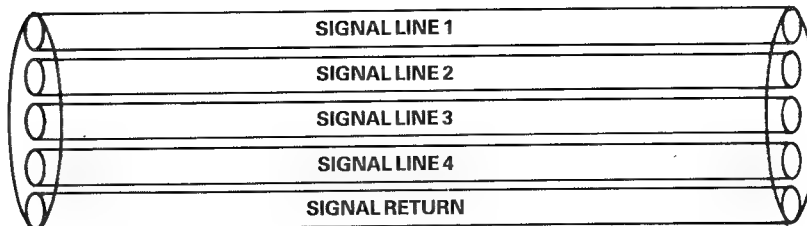
This simple circuit illustrates a poorly designed, single point grounding scheme. Note the two loop areas enclosed by the current flow. These large areas cause an excessive amount of inductive coupling between the circuits.

### PROPER SIGNAL ROUTING REDUCES LOOP AREA



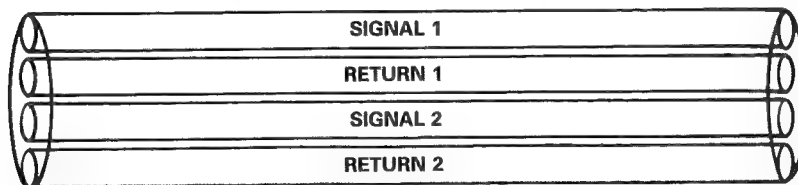
By properly routing the signal, the areas are greatly reduced, as is any inductively coupled interference. Twisting the signal and return leads will also help significantly. The equal and opposite currents produce magnetic fields that tend to cancel each other and the benefits can be significant. In comparison to running the two leads side by side, two twists per foot will reduce the voltage induced by approximately 15dB. Three twists in a foot will reduce it by 23dB and twelve twists per foot will reduce the coupled noise by about 43dB. This is an easy way to enhance the signal to noise ratio of your system.

### FLAT RIBBON CABLE WITH A SINGLE RETURN RESULTS IN UNEQUAL LOOP AREAS

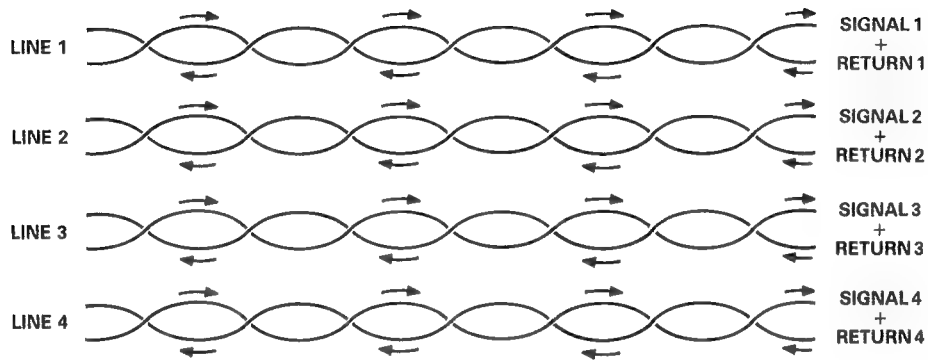


The ribbon cable shown above does not equally minimize signal loop areas. The signal through line one encloses the largest loop area, through line 4 the smallest. If this was a digital data bus which line should be assigned to the LSB? Since the LSB changes state most frequently, one could argue that it should be assigned to line 4. But what about the MSB? If it is assigned to line 1, then it is the most susceptible to noise. This could result in a half scale error if it is toggled by loop noise.

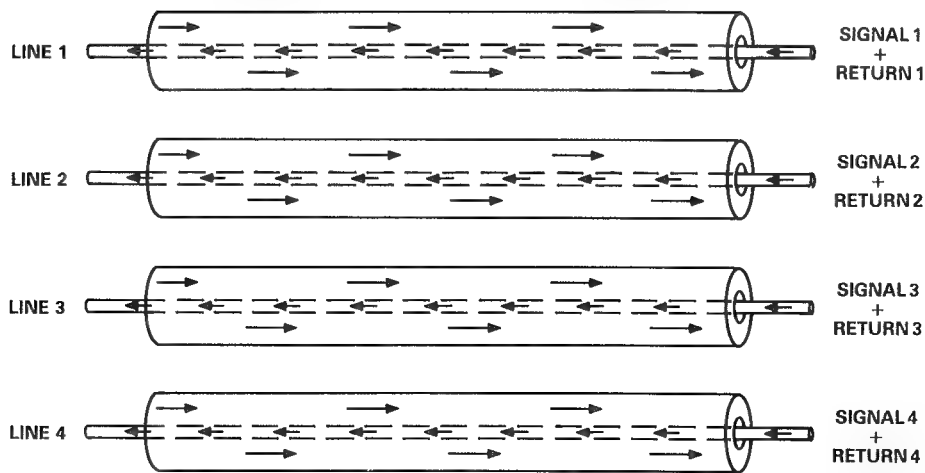
### ALTERNATE SIGNAL AND RETURN LINES IMPROVE SIGNAL INTEGRITY



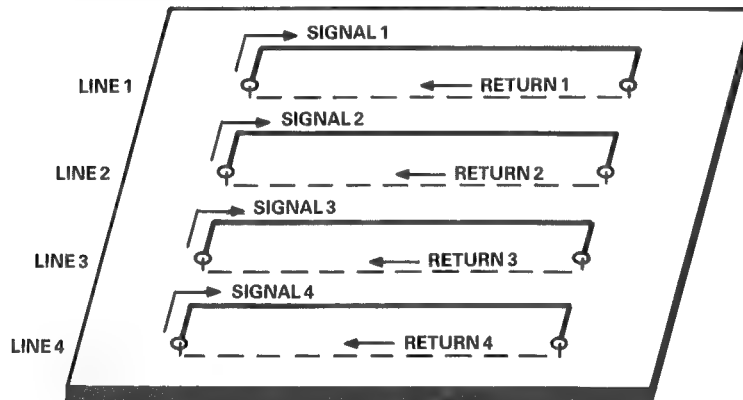
## TWISTED PAIR PROVIDES A SIGNAL AND RETURN PATH FOR ALL LINES



## COAXIAL CABLE PROVIDES INDIVIDUAL SIGNAL AND RETURN LINES



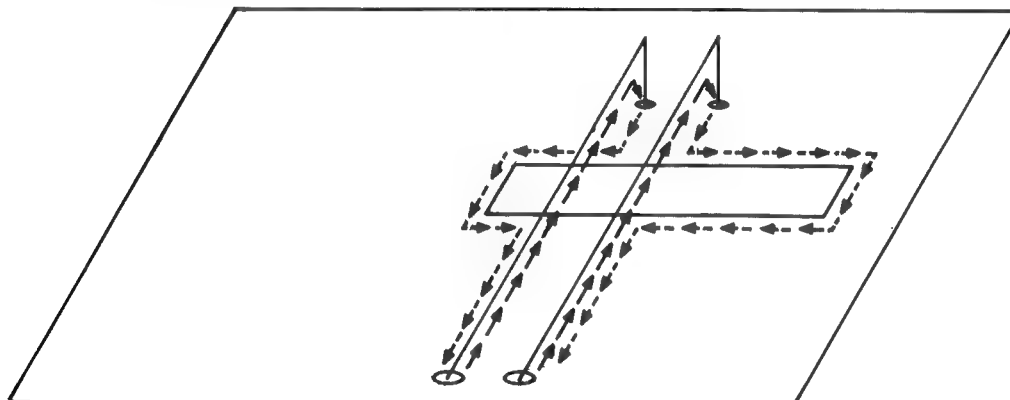
## TWO LAYER PRINTED CIRCUIT BOARD PROVIDES A TRACE FOR EACH SIGNAL AND A GROUND PLANE FOR THE RETURN PATHS



A preferred solution is to provide multiple return paths, ideally one return for each signal. This may be accomplished by dedicating every other line of the ribbon cable as a signal return. Another option is to use twisted pair. Each pair should be composed of a signal path and a return for that signal. Coaxial cable could accomplish the same result. An alternative approach is to use a ground plane. Each signal will automatically return via a minimum area (minimum inductance) path through the plane.

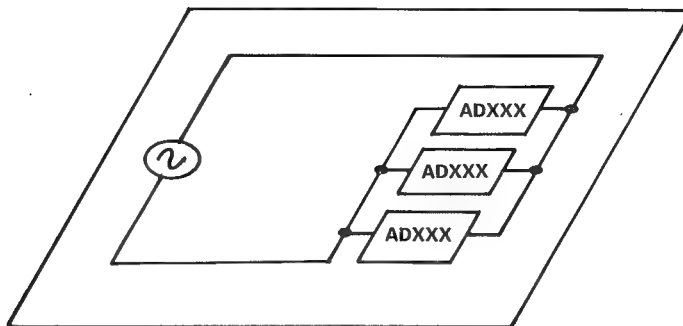
This leads to the subject of current flow patterns and associated noise problems on printed circuit boards. When laying out a PC board, it is very important to consider where the currents will flow. Again, the same argument applies: current will choose the path of least impedance. This generally means least area. Unfortunately, we sometimes prevent this from happening by the way we lay out our board.

### OPENING IN 2 LAYER PC BOARD CAN RESULT IN CURRENTS TAKING A NONOPTIMUM PATH

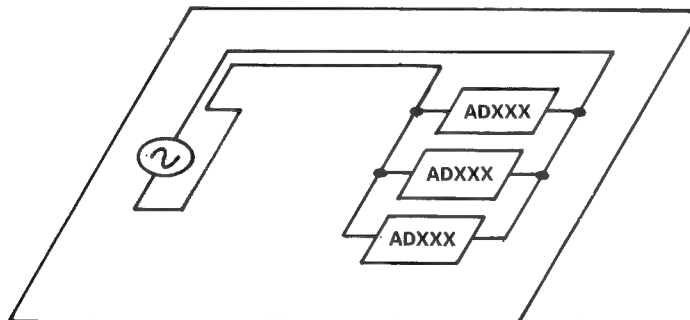


Often on a two layer PC board, an opening is cut around a device. This opening can get in the way of current selecting the least inductive path. In the figure above, the signal follows its path on the top layer, goes through the board, and tries to return to its source through the metal plane below. If the opening weren't there, the current would flow directly underneath its original path, minimizing the loop area. With the opening cut away in the plane, this path is impossible and another one is chosen which results in a larger enclosed area. This, of course, increases the magnetic coupling between the traces.

### NONIDEAL SIGNAL TRACE ROUTING



### IMPROVED TRACE ROUTING



We not only prevent current from selecting the best path in a ground plane, but we may also force it to take an excessively inductive path by routing it that way. The figure above illustrates this point. Proper trace routing to minimize the area enclosed by the signal path significantly reduces inductive coupling of noise. This principle should be followed as much as possible when designing PC boards, or any boards for that matter. It is important for low level analog signals, power supply busses, digital signals—all signals.

Another means of decreasing magnetic coupling is through shielding. The capacitive shield discussed previously intercepts the electric field and reroutes the noise currents back to their source. A magnetic shield redirects the magnetic flux by providing a path of higher permeability.

Permeability is a measure of how easily magnetic flux can be established in a material. For non-magnetic materials such as copper, aluminum, wood, or glass the permeability is, practically speaking, the same as that for air. For magnetic materials, the permeability is a hundred or a thousand times that of air.

## PERMEABILITY ( $\mu$ ) IS A MEASURE OF HOW EASILY MAGNETIC FLUX CAN BE ESTABLISHED IN A MATERIAL

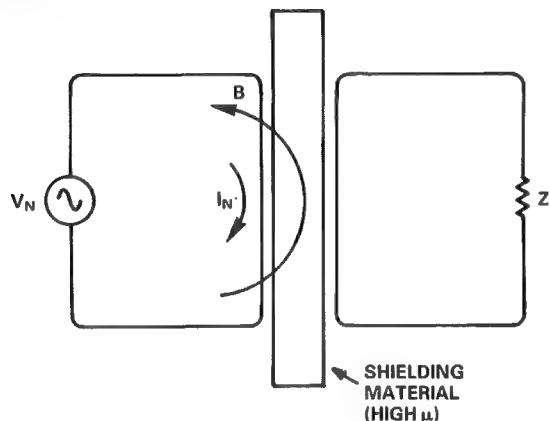
$$\text{PERMEABILITY OF FREE SPACE} = \mu_0 = 4\pi \times 10^{-7} \text{ H/M}$$

$$\text{RELATIVE PERMEABILITY OF A MATERIAL} = \mu_r = \frac{\text{PERMEABILITY OF MATERIAL}}{\text{PERMEABILITY OF FREE SPACE}} = \frac{\mu}{\mu_0}$$

MATERIAL	$\mu_r$
BISMUTH	0.9999986
PARAFFIN	0.9999942
WOOD	0.9999995
SILVER	0.9999981
ALUMINUM	1.00000065
BERYLLIUM	1.00000079
NICKEL CHLORIDE	1.00004
MAGNESIUM SULFATE	1.0001
NICKEL	50
CAST IRON	60
COBALT	60
POWDERED IRON	100
MACHINE STEEL	300
FERRITE (TYPICAL)	1,000
PERMALLOY 45	2,500
TRANSFORMER IRON	3,000
SILICON IRON	3,500
IRON (PURE)	4,000
MUMETAL	20,000
SENDUST	30,000
SUPERMALLOY	100,000

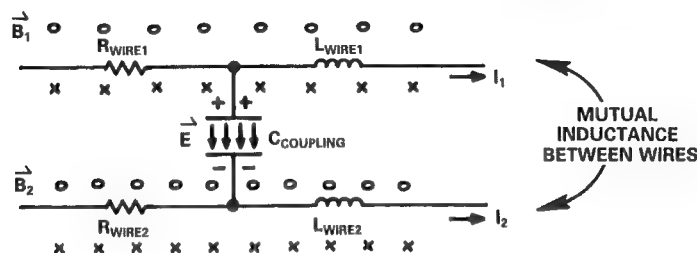
Magnetic flux will take a path of most permeability. This is the principle upon which the magnetic shield is based. The shield must be made out of a magnetic material with a high relative permeability. This shield will then contain most of the flux. The magnetic field remains the same strength as it was before the shield was added, however, the flux pattern changes.

## REDIRECTING MAGNETIC FLUX BY SHIELDING

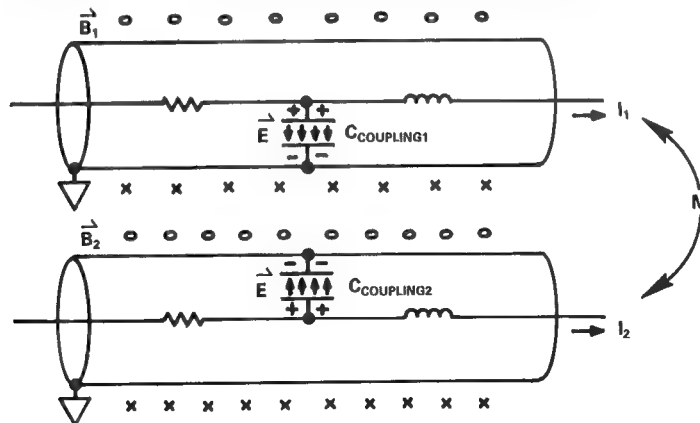


To illustrate the difference between magnetic and capacitive shields, consider current flowing in two wires. They have no shield. If we replace the exposed wire with coaxial cable, we have provided a capacitive shield. The outer conductor of the cable will intercept the electric field and a carefully chosen connection will provide a return path for the noise currents. However, the coaxial cable does not act as an effective magnetic shield. The outer conductor is not a magnetic material and therefore has a permeability practically equivalent to air. This does not help contain the flux. An additional shield made of iron, or some other highly permeable material, will provide a means to contain the magnetic flux.

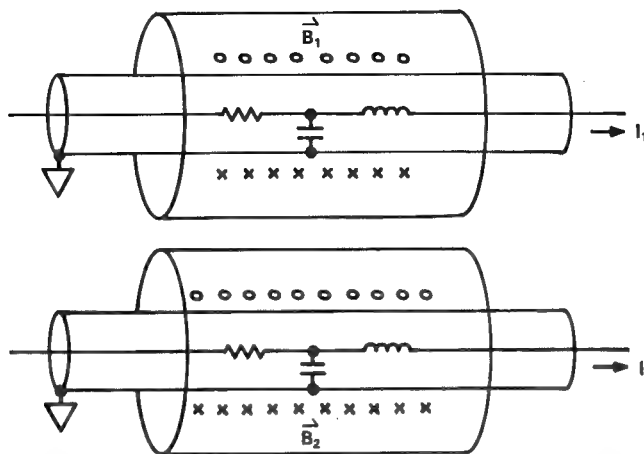
## CURRENT IN UNSHIELDED WIRE IS EXPOSED TO BOTH CAPACITIVE AND MAGNETIC COUPLING



## COAXIAL CABLE ACTS AS CAPACITIVE SHIELD BUT IS NOT EFFECTIVE AS A MAGNETIC SHIELD



## MAGNETIC SHIELDS WITH HIGH RELATIVE PERMEABILITY CONTAIN MAGNETIC FLUX, REDUCE MUTUAL INDUCTANCE AND ARE EFFECTIVE AT ELIMINATING INDUCTIVELY COUPLED INTERFERENCE



## SOME IDENTIFYING CHARACTERISTICS OF INDUCTIVELY COUPLED NOISE ARE:

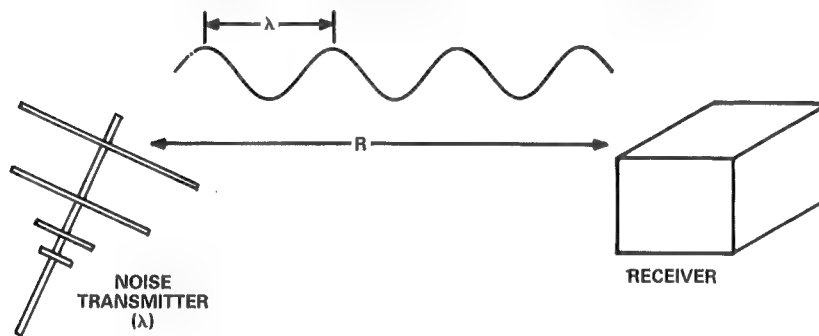
- Excessive wiring inductance due to unnecessary loop areas.
- Unaffected by materials which are nonconducting or nonmagnetic, such as people.
- The shield effectiveness is not influenced by different grounding schemes.
- High noise current.
- High frequency noise.

Logic signals are often magnetically coupled, as suggested by the last two characteristics.

## RADIATIVE COUPLING

Radiative coupling is the reception or transmission of propagating electromagnetic energy. It is a far field effect, as opposed to capacitive and inductive coupling, which are near field effects, and direct conductive coupling.

### FAR FIELD EFFECTS OCCUR AT DISTANCES GREATER THAN ONE INTERFERENCE WAVELENGTH



**FAR-FIELD DISTANCE:  $R \geq \lambda$**

The possibility that noise is electromagnetically, or radiatively, coupled can be disregarded unless the transmitter and receiver are at least one wavelength apart. A list of common interference wavelengths is given below

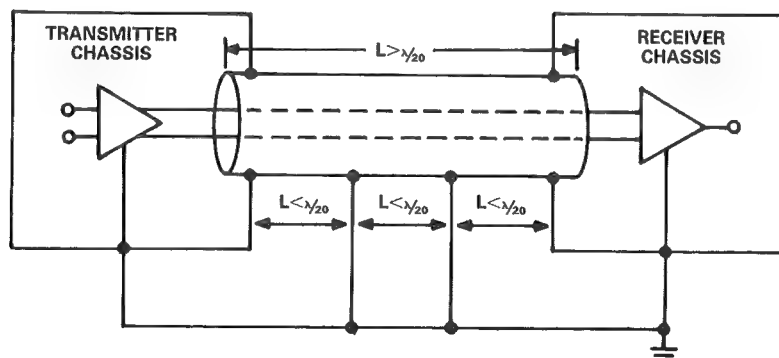
INTERFERENCE SOURCE	FREQUENCY ( $F_N$ )	WAVELENGTH ( $\lambda$ )
U.S. Power	60Hz	5,000km
European Power	50Hz	6,000km
Aircraft Power	400Hz	750km
Switching	20kHz	15km
Power Supplies	40kHz	7.5km
FM Radio	88MHz–108MHz	2.7m–3.4m
AM Radio	550kHz–1600kHz	188m–545m
Microwaves	1.5GHz–600GHz	0.5mm–200mm
X-Rays	$15 \times 10^{15}\text{Hz} - 6 \times 10^{24}\text{Hz}$	0.05fm–20nm
TV	56MHz–16Hz	300mm–5.4m
Amateur Band	3MHz–36MHz	8.3m–100m
Cellular Phones	800MHz	375mm

$$C = \text{SPEED OF LIGHT} = \lambda f_n \approx 3 \times 10^8 \text{m/s}$$

fm	$= 10^{-15}\text{m}$
pm	$= 10^{-12}\text{m}$
nm	$= 10^{-9}\text{m}$
$\mu\text{m}$	$= 10^{-6}\text{m}$
mm	$= 10^{-3}\text{m}$
km	$= 10^3\text{m}$
kHz	$= 10^3\text{Hz}$
MHz	$= 10^6\text{Hz}$
GHz	$= 10^9\text{Hz}$

The best way to reduce radiatively coupled noise is by shielding.

### USING A SHIELD TO REDUCE RADIATIVE COUPLING



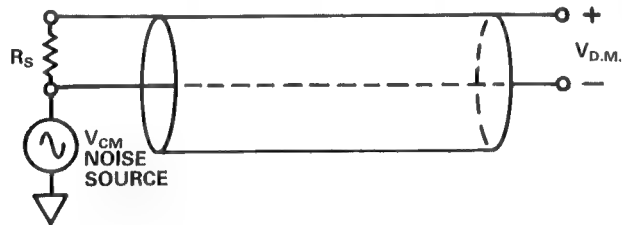
Electromagnetic shields must make a tight bond, both mechanically and electrically, at each end. They should never be terminated inside the receiver as this would provide a path via which the high frequency currents could penetrate. If the shield has a length greater than  $\lambda/20$ , then it may act as an antenna. This effect can be reduced by connecting the shield to ground along its length at distances less than  $\lambda/20$ , making it appear electrically shorter than it is.

When evaluating electromagnetic susceptibility, remember that if a system can transmit energy at a certain frequency then it can also receive at that frequency and vice-versa.

## BALANCED VS. UNBALANCED SYSTEMS

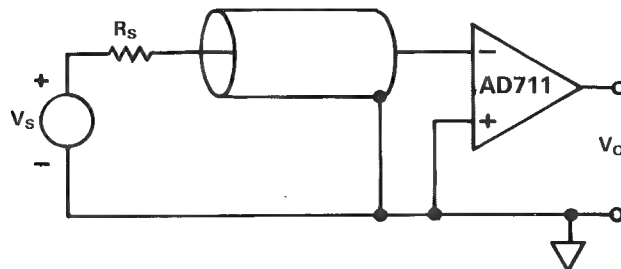
An unbalanced circuit can cause a common mode noise to become differential.

### CIRCUIT UNBALANCE CAUSES COMMON MODE TO DIFFERENTIAL MODE CONVERSION

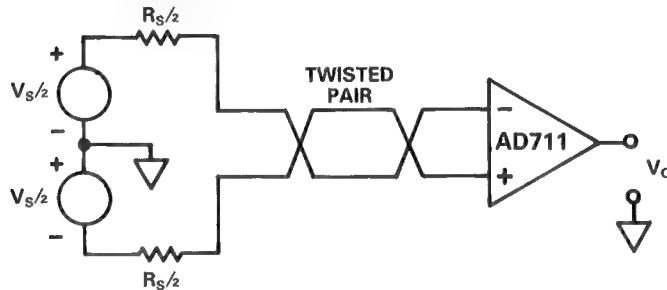


Desired signals are differential. Noise can be either differential or common mode. A conversion of common mode noise to differential will cause it to interfere with the desired signal. A balanced circuit helps to minimize this conversion.

### UNBALANCE (SINGLE ENDED) CIRCUIT



### BALANCED (DIFFERENTIAL) CIRCUIT

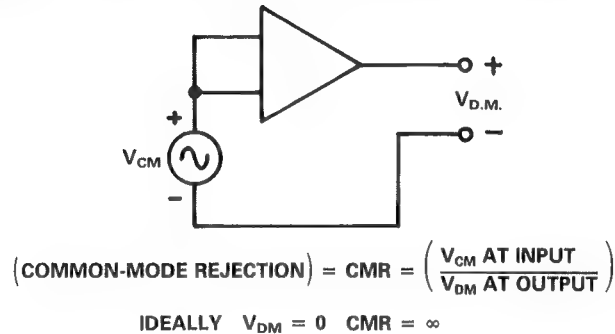


A balanced circuit is one whose current signal path is electrically identical to the current return path. For a system to be balanced, every component must be balanced, including the source, the cable, and the receiver.



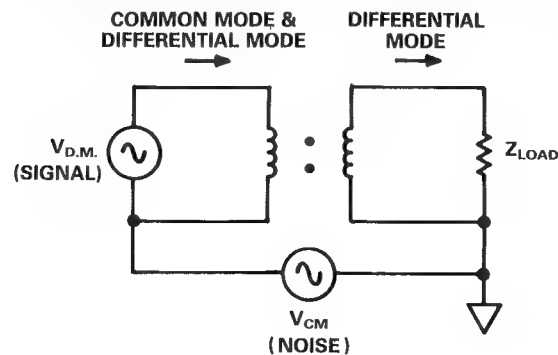
Devices with good common-mode rejection help to control noise by improving the circuit balance.

## DEFINITION OF COMMON-MODE REJECTION



Differential amplifiers, instrumentation amplifiers, and isolation amplifiers are examples of good common-mode rejection devices.

## SIMPLIFIED MODEL OF ISOLATION AMPLIFIER ILLUSTRATES COMMON-MODE REJECTION



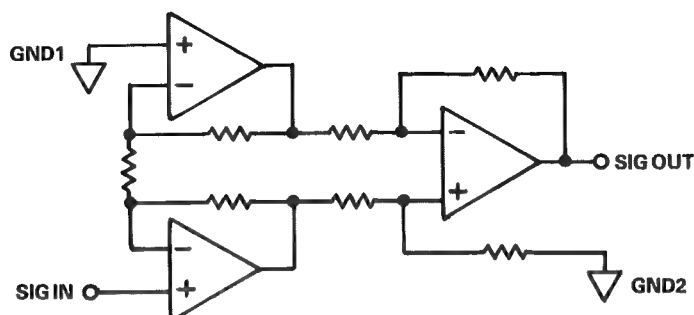
To minimize the conversion of common-mode noise to differential mode noise, electrically balance the system and use devices with high common-mode rejection.

## TRANSLATING GROUNDS

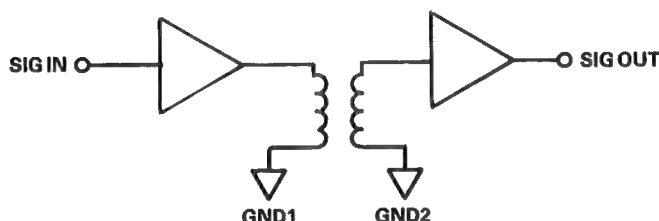
There will always be noise between different local grounds. These ground to ground noise voltages must be anticipated during system design so that an appropriate strategy can be developed to handle them. A voltage is meaningless if it is not referred to something. Therefore, when transferring signals from one ground to another, the signal must be translated from one ground reference to another.

The most common way to translate an analog signal to a board with a different ground reference is to use an electronic isolator such as an instrumentation amp, isolation amp, or differentially connected op amp.

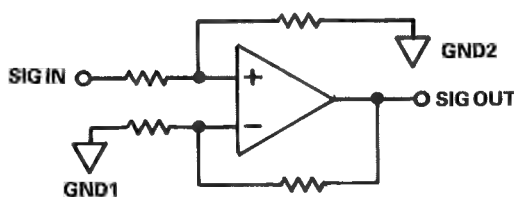
An isolation amp will cover ground differences as large as several thousand volts. They are suitable for transmitting low frequency (several kilohertz) signals between grounds that have very high levels of ground to ground noise. An inherent advantage of transformer coupling is that high frequency signals such as power supply glitches cannot readily pass through the transformer. The limited frequency response of the transformer core can be a disadvantage, however, because it limits the useable frequency of the signal being coupled through the isolation amplifier. In addition, isolation amplifiers are expensive; although modern manufacturing techniques have greatly lowered the price of some newer models.



**INSTRUMENT AMP ISOLATION**



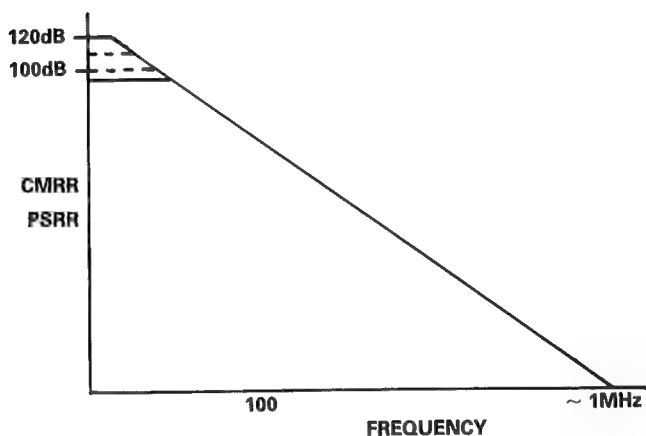
**ISOLATION AMPLIFIER**



**DIFFERENTIAL OP AMP**

Instrumentation amplifiers and differentially connected amplifiers can provide the ground translation function at a much lower cost, although they are not without pitfalls. Obviously, the signals must stay within the power supply rails, but this is not necessarily a problem. Of far more importance is the high frequency performance of in-amps and differential connected op amps. In the data sheet for any amplifier, there are two specifications that are of special interest. They are PSRR and CMRR. Usually these specs are on the order of 100 to 120dB. However, **THESE ARE DC SPECIFICATIONS**. They do not mean that the amplifier has high rejection at the frequencies associated with glitches and other types of noise.

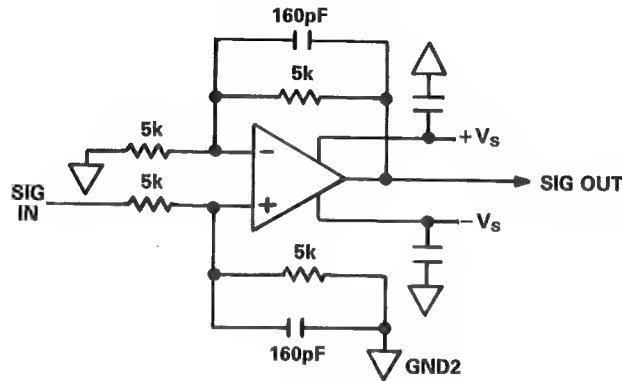
## CMRR AND PSRR VS. FREQUENCY



Most amplifiers have CMRR and PSRR specifications that follow a single pole rolloff as shown in the plot above. They are quite good at eliminating dc errors, 60Hz interference, and even audio frequency interference, but are almost useless at stopping glitches caused by digital switching or other high slew rate transients. Therefore, the high frequency transients must be filtered out by passive means before or after the instrumentation amplifier.

## GROUND NOISE ISOLATOR

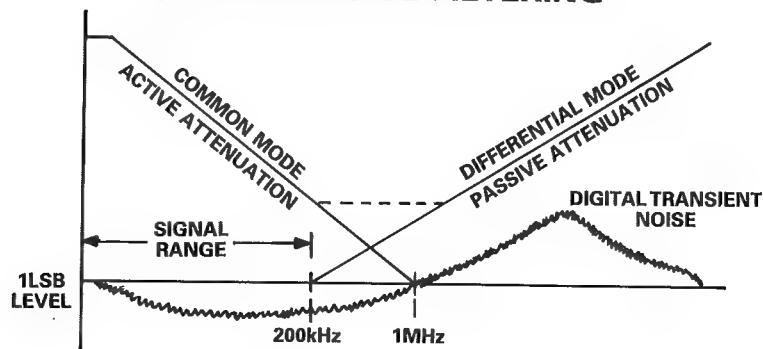
$$F_c = 200\text{kHz}$$



This figure shows a differential amplifier that has been modified by the addition of two capacitors so that it attenuates high frequency signals (glitches).

The 160pF capacitors causes attenuation of both differential and common mode signals above 200kHz. At that frequency, the common-mode noise attenuation is about a factor of five. This is shown graphically below. The power supplies in this configuration must be referred to ground 2 to avoid noise injection via the supplies.

## OVERALL NOISE FILTERING



The total noise level should be kept below 1 LSB to preserve the accuracy of the system. This may be calculated by integrating the noise over the frequency range and multiplying the result by the attenuation factors of both the active common-mode attenuation (CMRR of the in-amp) and the differential mode attenuation (due to the R-C circuit) at higher frequencies. In the example shown and in many real life situations, most of the noise is at higher frequencies where the common-mode attenuation of the amplifier will not affect it. To compound the problem, high frequency noise is often rectified by both active and passive components resulting in a dc error. In these situations, it is absolutely necessary to provide some kind of passive filtering to eliminate noise. The filtering in this example limits the useful signal frequency to under 200kHz. However, it also eliminates most of the noise that would otherwise interfere. The bandwidth of a system need not exceed the required signal bandwidth. If the signal frequency range is much wider, it may be necessary to use more expensive high frequency amplifiers to translate signals from one ground level to another. Hybrid video amplifiers might be appropriate since they have at least a decade more CMRR than inexpensive monolithic amplifiers.

## **A FEW GENERAL RULES**

**Consider all signals to be differential signals requiring a path to and from their source. With proper attention to all applicable details, "ground" may serve as a return path.**

**Use separate signal and power return conductors.**

**Keep signal paths as short as possible. This will help to minimize voltage drops through the conductors as well as to minimize magnetic interference by controlling loop areas.**

**Using twisted pair cable is an easy way to improve the noise rejection of a system.**

**Provide separate analog and digital grounds and tie the two together only once.**

**Provide one connection from the system ground to the actual earth ground.**

**Connect capacitive shields once to provide a return path to the noise source.**

**Magnetic shields must be made out of a highly permeable material to be effective.**

**Metal should not be left electrically floating.**

**Maintain the balance of a system to prevent common mode signals from becoming differential.**

**Limit the bandwidth of the system to the required signal bandwidth**

**Last but not least: KEEP LOOP AREAS SMALL AND ALWAYS THINK – WHERE WILL THE CURRENTS FLOW?**



# APPENDIX A

## SECTION I

READS AND PUTS DATA INTO MEMORY LOCATION [0500], [0502], [0504], [0506]

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0100	DF = 0 CLEAR DIR FLAG	CLD	FC	SET CLEAR DIRECTION FLAG TO "0"
0101	MOV I TO DI	MOV 500→DI	BF	MOV IMM TO DI FOR INITIAL DATA LOCATION
0102			00	MEMORY LOCATIONS FOR ANALOG INPUT SIGNALS
0103			05	
0104	MOV IMM TO AX	MOV	B8	MOV TO [AX] 0004
0105			04	
0106			00	
0107	MOV AX TO M1 0004→0300	MOV AX <sub>1</sub> [0300]	A3	MOV [AX] TO 0300
0108			00	
0109			03	
010A	MOV IMM TO AL		B0	MOV TO AL THE FOLLOWING NUMBER
010B			80	THIS DEFINES P1 AS AN AN OUTPUT PORT
010C	MOV IMM TO DX	MOV FFFF→DX	BA	MOV TO THE [DX]
010D			FF	INITIALIZE FOR OUTPUT PORT
010E			FF	PG 3-16
010F	OUT DX, AX		EE	THE [DX] REGISTER IS A POINTER FOR THE AL INSTRUCTION
0110	MOV IMM TO DX	MOV TO DX	BA	
0111			F9	LOCATION FOR DATA OUT
0112			FF	LOCATION FOR DATA OUT
0113	MOV [0300]→AX		A1	MOV [0300]→ [AX]
0114			00	
0115			03	

# SECTION I (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0116	OUT DX		EE	OUTPUT <b>AL</b> TO DIA
0117	MOV IMM TO DX		BA	LOCATION FOR DATA OUT
0118			FB	LOCATION FOR DATA OUT
0119			FF	Pg 4-8
011A	MOV IMM TO AL		B0	MOV TO <b>AL</b> FF
011B			FF	NUMBER FF TO AL
011C	OUT DX		EE	OUTPUT AL TO PIB
011D	NOT AL		F6	INVERT AL
011E			D0	
011F	OUT DX		EE	OUTPUT <b>AL</b> TO PIB
0120	NOP		90	NO OPERATION
0121	NOP		90	NO OPERATION
0122	NOP		90	NO OPERATION
0123	MOV IMM TO AX		B8	MOV IMM TO <b>AX</b>
0124			09	NUMBER INTO
0125			00	ACCUMULATOR
0126	DEC AX		48	DECREMENT <b>AX</b>
0127	JNZ		75	JUMP NOT ZERO
0128			FD	FD = FF-02
0129	MOV IMM TO AX		B8	MOV IMM TO <b>AX</b>
012A			9B	THIS WORD DEFINES P2/P1 AS AN INPUT PORT
012B			9B	
012C	MOV IMM TO DX		BA	MOV TO THE <b>DX</b> REGISTER THE FOLLOWING NUMBER
012D			FE	PORT ADDRESS PG 3-16
012E			FF	PORT ADDRESS PG 3-16
012F	OUT AX, DX		EF	THE <b>DX</b> REGISTER ACTS AS A POINTER FOR THE <b>AX</b> REGISTER
0130	MOV IMM TO DX		BA	MOV TO <b>DX</b> THE FOLLOWING NUMBER FFFC
0131			FC	THIS NUMBER DEFINES THE PORT INPUT ADDRESS
0132			FF	
0133	IN DX		ED	THE CONTENTS OF STORE DATA AT DI (0500)
0134	STDSW		AB	INDEXES THE <b>DI</b> ONE
0135			B8	MOV IMM TO <b>AX</b>
0136			00	PLACE ALL ZEROS
0137			00	INTO ACCUMULATOR

# SECTION I (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0138	MOV [0300]→AX		AX	MOV [0300] → <b>AX</b>
0139			00	THE CONTENTS OF MEMORY LOCATION [0300] ARE LOADED INTO THE ACCUMULATOR
013A			03	
013B	DEC AX		48	DECREMENT <b>AX</b> REDUCE AX BY ONE
013C	JNZ		75	JUMP NOT ZERO
013D			C9	THIS MANY BACK (FF – XX) = C9
013E	JUMP UNCONDITIONAL	EB	EB	JUMP ON ANYTHING
			90	NO OP
013F			C1	THIS MUCH
			90	NO OP
0140			F4	STOP
			90	NO OP



## SECTION II

### COMPUTES OFFSET AND STORES IN [06??]

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0141	MOV IMM TO AX		B8	MOV IMM TO <b>AX</b>
0142			00	000 – 0400 = 0800
0143			08	000 – 0400 = 0800
0144	MOV AX→[0600]		A3	MOV <b>AX</b> → [0600]
0145			00	MEMORY LOCATION
0146			06	FOR (0800)
0147			F8	CLEAR CARRY FLAG
0148			A1	MOV [0504] → <b>AX</b>
0149			04	MEMORY LOCATION FOR ANALOG GROUND
014A			05	≈0800 ± 2
014B			8B	MOV [0600] → <b>BX</b>
014C			1E	MOV [0600] → <b>BX</b>
014D			00	MEMORY LOCATION
014E			06	FOR 0800
014F			2B	
0150			C3	<b>AX</b> – <b>BX</b> = <b>AX</b>
0151			73	JUMP IF CF = 0
0152			0A	← THIS MANY
0153			A1	MOV [0504] → AX
0154			04	MEMORY LOCATION FOR ANALOG GROUND
0155			05	0800 ± 3
0156			8B	MOV [0600] = <b>BX</b>
0157			1E	
0158			00	MEMORY LOCATION [0600]
0159			06	[0600] CONTAINS NUMBER 0800
015A			93	SWAP <b>AX</b> → ← <b>BX</b>
015B			2B	<b>AX</b> – <b>BX</b> = <b>AX</b>
015C			C3	<b>AX</b> – <b>BX</b> = <b>AX</b>
015D			90	NO OP
015E			A3	MOV <b>AX</b> → [0604]
015F			04	MEMORY LOCATION
0160			06	Δ OFFSET
0161			F4	HALT
			90	NO OP

### SECTION III

**TAKES [0604] (OFFSET 1), COMPARES GROV REFERENCE AND COMPUTES AIN<sup>1</sup>**  
**AIN<sup>1</sup> = AIN ± OFFSET**

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0162			F8	CLEAR CARRY FLAG
0163			90	NO OP
0164			90	NO OP
0165			90	NO OP
0166			90	NO OP
0167			90	NO OP
0168				NO OP
0169			90	NO OP
016A			90	NO OP
016B			90	NO OP
016C			90	NO OP
016D			90	NO OP
016E			A1	MOV [0504] → <b>AX</b>
016F			04	LOCATION FOR ANALOG GROUND
0170			05	
0171			8B	MOV [0600] → <b>BX</b>
0172			1E	MOV [0600] → <b>BX</b>
0173			00	LOCATION FOR 0800
0174			06	LOCATION FOR 0800
0175			2B	<b>AX</b> - <b>BX</b> = <b>AX</b>
0176			C3	<b>AX</b> - <b>BX</b> = <b>AX</b>
0177			72	JUMP IF CF → 1
0178			10	← THIS MANY
0179			A1	MOV [0506] → <b>AX</b>
017A			06	LOCATION FOR AIN
017B			05	LOCATION FOR AIN
017C			8B	MOV [0604] → <b>BX</b>
017D			1E	[0604] → DELTA
017E			04	MEMORY LOCATION FOR DELTA OFFSET
017F			06	
0180			2B	<b>AX</b> = <b>AX</b> - <b>BX</b>
0181			C3	<b>AX</b> = <b>AX</b> - <b>BX</b>
0182			A3	MOV <b>AX</b> → [0508]
0183			08	AIN <sup>1</sup>
0184			05	AIN <sup>1</sup>
0185			90	NO OP
0186			90	NO OP
0187			EB	JUMP UNCONDITIONAL
0188			OF	THIS MANY

### SECTION III (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
0189			90	
018A			90	
018B			A1	MOV [0506] → <b>AX</b>
018C			06	MEM LOCATION FOR AIN
018D			05	
018E			8B	MOV [0604] → <b>BX</b>
018F			1E	
0190			04	MEMORY LOCATION FOR DELTA
0191			06	
0192			03	<b>AX</b> = <b>AX</b> + <b>BX</b>
0193			C3	<b>AX</b> = <b>AX</b> + <b>BX</b>
0194			A3	MOV <b>AX</b> → [0508]
0195			08	
0196			05	AIN <sup>1</sup>
0197			90	NO OP
0198			90	NO OP
0199			90	NO OP
019A			90	NO OP
019B			F4	NO OP
			90	

## Section IV

### COMPUTES THE VALUE FOR THE ANALOG INPUT BY CORRECTING SLOPE

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
019C			A1	MOV [0500] → <b>AX</b> $V_{REF+} \approx 0C00$
019D			00	MEMORY LOCATION
019E			05	MEMORY LOCATION
019F			8B	MOV [0502] → <b>BX</b> $V_{REF-} \approx 0400$
01A0			1E	
01A1			02	MEMORY LOCATION FOR $-5V_{REF} \approx 0400$
01A2			05	
01A3			2B	<b>AX</b> - <b>BX</b> = <b>AX</b>
01A4			C3	
01A5			A3	MOV <b>AX</b> → [0606] THIS IS THE LOCATION FOR $\Delta M12$
01A6			06	
01A7			06	
01A8			A1	MOV AIN <sup>1</sup> [0508] → <b>AX</b>
01A9			08	MEMORY LOCATION FOR CORRECTED ANALOG SIGNAL
01AA			05	
01AB			8B	MOV [0600] → <b>BX</b>
01AC			1E	MOV [0600] → <b>BX</b>
01AD			00	MEMORY LOCATION FOR 0800
01AE			06	
01AF			F7	MULT <b>AX</b> BY <b>BX</b>
01B0			E3	STORE RESULTS IN <b>DX</b> <b>AX</b>
01B1			8B	MOV [0606] (DM12) → <b>BX</b>
01B2			1E	MOV [0606] (DM12) → <b>BX</b>
01B3			06	
01B4			06	LOCATION FOR DM12
01B5			F7	DIVIDE <b>DX</b> <b>AX</b>
01B6			F3	BY <b>BX</b> = <b>AX</b> <b>BX</b>
01B7			A3	MOV <b>AX</b> → [0608]
01B8			08	LOCATION FOR FINAL ANSWER
01B9			06	

# Section V

## MODIFIES ANSWER TO ACCOUNT FOR ROUNDING ERRORS

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
01BA			92	SWAP $\boxed{AX}$ $\rightarrow$ $\leftarrow \boxed{DX}$
01BB			A3	MOV $\boxed{AX}$ $\rightarrow$ [0610]
01BC			10	LOCATION FOR REMAINDER
01BD			06	LOCATION FOR REMAINDER
01BE			B8	MOV IMM TO $\boxed{AX}$
01BF			02	NUMBER 2
01CO			00	NUMBER 2
01C1			A3	MOV $\boxed{AX}$ $\rightarrow$ [0612]
01C2			12	LOCATION FOR #2
01C3			06	LOCATION FOR #2
01C4			B8	MOV IMM TO $\boxed{AX}$
01C5			01	#1
01C6			00	#1
01C7			A3	MOV $\boxed{AX}$ $\rightarrow$ [0614]
01C8			14	LOCATION FOR 0001
0109			06	LOCATION FOR 0001
01CA			BA	MOV IMM $\rightarrow$ $\boxed{DX}$
01CB			00	#0000
01CC			00	#0000
01CD			A1	MOV [0606] $\rightarrow$ $\boxed{AX}$
01CE			06	MEMORY LOCATION
01CF			06	MEMORY LOCATION
01D0			8B	MOV [0612] $\rightarrow$ $\boxed{BX}$
01D1			1E	
01D2			12	MEMORY LOCATION FOR #2 (0002)
01D3			06	
01D4			F7	DIV $\boxed{DX}$ $\boxed{AX}$
01D5			F3	BY $\boxed{BX}$ = $\boxed{AX}$ $\boxed{DX}$
01D6			A3	MOV $\boxed{AX}$ $\rightarrow$ [0616]
01D7			16	$\frac{\Delta M12}{2} \approx 0400$
01D8			06	$\frac{\Delta M12}{2} \approx 0400$
01D9			8B	MOV [0610] $\rightarrow$ $\boxed{BX}$
01DA			1E	
01DB			10	LOCATION OF REMAINDER
01DC			06	LOCATION OF REMAINDER
01DD			F8	CLEAR CARRY FLAG
01DE			2B	$\boxed{AX} - \boxed{BX} = \boxed{AX}$
01DF			C3	

# SECTION V (Continued)

PROGRAM MEMORY	MNEMONIC	BINARY CODE	HEX CODE	DESCRIPTION/ COMMENTS
01E0			73	JUMP IF CF = 0
01E1			0D	← THIS MANY
01E2			8B	MOV [0608] → <b>BX</b>
01E3			1E	
01E4			08	LOCATION OF ANSWER
01E5			06	LOCATION OF ANSWER
01E6			A1	MOV [0614] → <b>AX</b>
01E7			14	NUMBER 0001 LOCATION
01E8			06	NUMBER 0001 LOCATION
01E9			03	<b>AX</b> + <b>BX</b> = <b>AX</b>
01EA			C3	
01EB			A3	MOV <b>AX</b> → 0608
01EC			08	MEMORY LOCATION FOR ANSWER
01ED			06	
01EE			90	NO OP
01EF			90	NO OP
01F0			90	NO OP
01F1			F4	HALT

# APPENDIX B

## BINARY BIT WEIGHTS OR RESOLUTION

BIT	$2^{-n}$	$1/2^n$ (Fraction)	"dB"	$1/2^n$ (Decimal)	%	ppm
FS	$2^0$	1	0	1.0	100	1,000,000
MSB	$2^{-1}$	1/2	-6	0.5	50.	500,000
2	$2^{-2}$	1/4	-12	0.25	25	250,000
3	$2^{-3}$	1/8	-18.1	0.125	12.5	125,000
4	$2^{-4}$	1/16	-24.1	0.0625	6.2	62,500
5	$2^{-5}$	1/32	-30.1	0.03125	3.1	31,250
6	$2^{-6}$	1/64	-36.1	0.015625	1.6	15,625
7	$2^{-7}$	1/128	-42.1	0.007812	0.8	7,812
8	$2^{-8}$	1/256	-48.2	0.003906	0.4	3,906
9	$2^{-9}$	1/512	-54.2	0.001953	0.2	1,953
10	$2^{-10}$	1/1,024	-60.2	0.0009766	0.1	977
11	$2^{-11}$	1/2,048	-66.2	0.00048828	0.05	488
12	$2^{-12}$	1/4,096	-72.2	0.00024414	0.024	244
13	$2^{-13}$	1/8,192	-78.3	0.00012207	0.012	122
14	$2^{-14}$	1/16,384	-84.3	0.000061035	0.006	61
15	$2^{-15}$	1/32,768	-90.3	0.0000305176	0.003	31
16	$2^{-16}$	1/65,536	-96.3	0.0000152588	0.0015	15
17	$2^{-17}$	1/131,072	-102.3	0.00000762939	0.0008	7.6
18	$2^{-18}$	1/262,144	-108.4	0.000003814697	0.0004	3.8
19	$2^{-19}$	1/524,288	-114.4	0.000001907349	0.0002	1.9
20	$2^{-20}$	1/1,048,576	-120.4	0.0000009536743	0.0001	0.95

# APPENDIX C

## STANDARD VALUE DECADE FOR 1% DECADE FOR 1% FILM RESISTORS

Ohms\*

10.0	14.7	21.5	31.6	46.4	68.1
10.2	15.0	22.1	32.4	47.5	69.8
10.5	15.4	22.6	33.2	48.7	71.5
10.7	15.8	23.2	34.0	49.9	73.2
11.0	16.2	23.7	34.8	51.1	75.0
11.3	16.5	24.3	35.7	52.3	76.8
11.5	16.9	24.9	36.5	53.6	78.7
11.8	17.4	25.5	37.4	54.9	80.6
12.1	17.8	26.1	38.3	56.2	82.5
12.4	18.2	26.7	39.2	57.6	84.5
12.7	18.7	27.4	40.2	59.0	86.6
13.0	19.1	28.0	41.2	60.4	88.7
13.3	19.6	28.7	42.2	61.9	90.9
13.7	20.0	29.4	43.2	63.4	93.1
14.0	20.5	30.1	44.2	64.9	95.3
14.3	21.0	30.9	45.2	66.5	97.6

\*Standard resistance values are obtained from the decade by multiplying by powers of 10. Ex.: 13.3 can be 13.3, 133, 1.33K, 13.3K, 133K, or 1.33MΩ.



# APPENDIX D

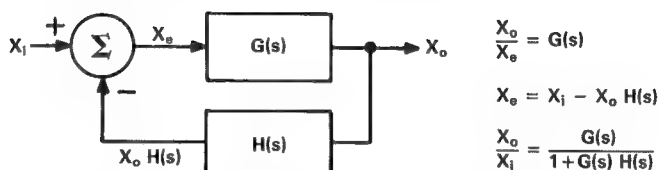
## NEGATIVE FEEDBACK TECHNIQUES

The concept of negative feedback is of considerable importance in the design of electronic systems. Negative feedback techniques allow the electronic designer to be more accurate in the prediction and control of the performance of his systems, and to achieve that control by the use of stable well-characterized passive elements such as resistors, capacitors and, sometimes, inductors.

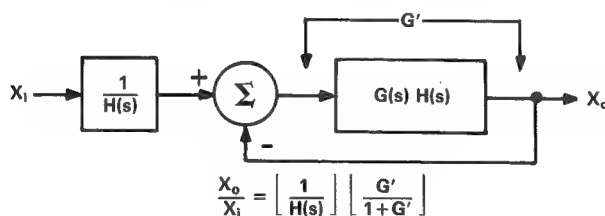
In all feedback controlled systems a signal derived from the system output is applied to a summing point where it is added to the original input signal and applied to an amplifier which drives the system output. The system is thereby stabilized. It should be clearly understood that negative feedback is a general physical concept which applies to systems of all types, not merely electronic ones, even though negative feedback in electronic systems is the only type that will be discussed in this seminar. Negative feedback techniques can be used in electronic systems to stabilize gain, bandwidth, impedance levels, velocity, position, or any physical parameter which can be converted to an electrical signal to be fed into the summing point.

A generalized diagram of a negative feedback system is shown in the diagram, as is a restructured version of the same system which has been redrawn to demonstrate more clearly how a negative feedback network works. (The feedback need not actually be negative—positive feedback systems are equally possible but are of more limited use, although the same analyses work for them.)

### GENERALIZED FEEDBACK NETWORK



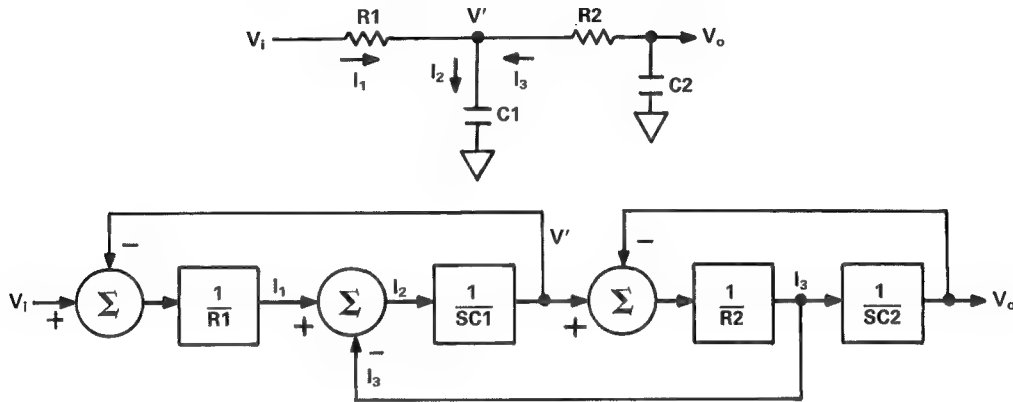
### RESTRUCTURED FORM OF GENERALIZED FEEDBACK NETWORK



Consider the diagram. For large values of the product  $G(s)H(s)$  the ratio  $X_o/X_i$  approaches a value of  $1/[H(s)]$ , indicating a distinct advantage of a negative feedback system: if the open loop gain is sufficiently large the system gain is determined by feedback and the open loop gain does not significantly affect it.

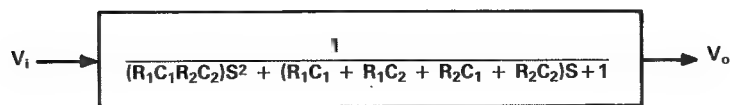
Electronic feedback systems can have voltage feedback, current feedback or both.

## RESISTOR CAPACITOR NETWORK AND EQUIVALENT FEEDBACK MODEL



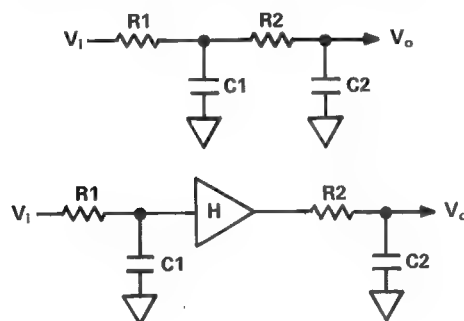
Even resistors—capacitor networks maybe modelled as a feedback network or control system. The system shown illustrates both voltage and current feedback and each element in the circuit represents a stand alone transfer function. Some simple mathematical manipulation can reduce the complex form to a simple block.

## EQUIVALENT RESISTOR CAPACITOR NETWORK REDUCED TO A SINGLE BLOCK

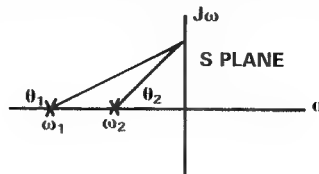


Control system analysis is a convenient means of describing many physical occurrences which we take for granted. Consider walking around with closed eyes—this represents a system with minimal negative feedback. At best one would have to move slowly and unless guided it would be quite difficult not to stumble into obstacles. Even with sight there are limitations upon the speed with which one could negotiate obstacles. This speed limitations may be regarded as the system frequency response and is directly related to the mechanics of the system. Practically speaking the frequency response is a measure of how quickly the system can respond to changes at the input.

## ISOLATION BETWEEN STAGES SIMPLIFIES ANALYSIS



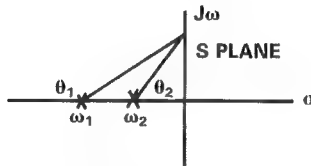
## ISOLATION/NONISOLATION COMPARISON



$$\omega_1 = \frac{-(R_1C_1 + R_1C_2 + R_2C_1 + R_2C_2) + \sqrt{(R_1C_1 + R_1C_2 + R_2C_1)^2 - 4(R_1C_1R_2C_2)}}{2(R_1C_1R_2C_2)}$$

$$\omega_2 = \frac{-(R_1C_1 + R_1C_2 + R_2C_1 + R_2C_2) - \sqrt{(R_1C_1 + R_1C_2 + R_2C_1)^2 - 4(R_1C_1R_2C_2)}}{2(R_1C_1R_2C_2)}$$

### NONISOLATED



$$\omega_1 = \frac{1}{R_1C_1}$$

$$\omega_2 = \frac{1}{R_2C_2}$$

### ISOLATED

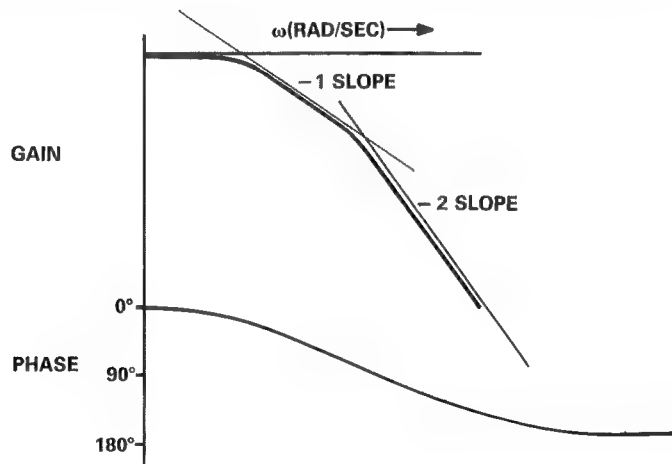
Obviously a single capacitor resistor circuit is easier to analyze than a cascaded dual capacitor resistor network for there is no interaction between the networks. But the two-resistor two-capacitor network is quite easy to analyze provided an isolation stage is placed between the circuits. Clearly each network has two poles, but in the nonisolated case repositioning one pole causes a shift in the location of the other. However, irrespective of the circuit topology the output phase is equal to the sum of  $\theta_1$  and  $\theta_2$ . The pole zero representation is a convenient method to visualize the phase response as the input frequency is varied. The pole zero diagram does not give much insight with regard to the absolute magnitude of the response, however, and Bode plot, or gain magnitude phase plot, is necessary. Consider again the resistor capacitor network resulting in two poles located at  $\omega_1$  and  $\omega_2$  whose values are 300 and 900 radians per second respectively. At low frequencies the phase shift approaches zero and at high frequencies the phase shift approaches zero and at high frequencies it approaches  $180^\circ$ . The fundamental equation for this response is:

$$\theta_T = \theta_1 + \theta_2$$

$$\theta_T = \tan^{-1} \omega/\omega_1 + \tan^{-1} \omega/\omega_2$$

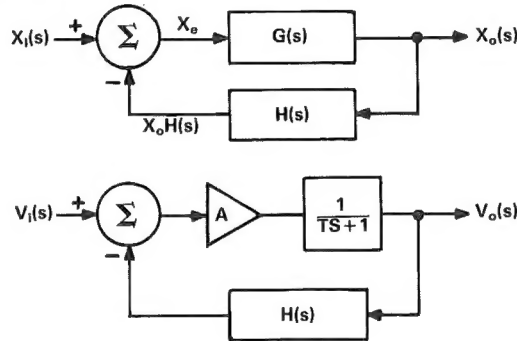
This response is consistent with the one implied by the pole zero diagram.

## GAIN MAGNITUDE/FREQUENCY & PHASE/FREQUENCY PLOTS FOR 2 RESISTOR/2 CAPACITOR LOW PASS FILTER



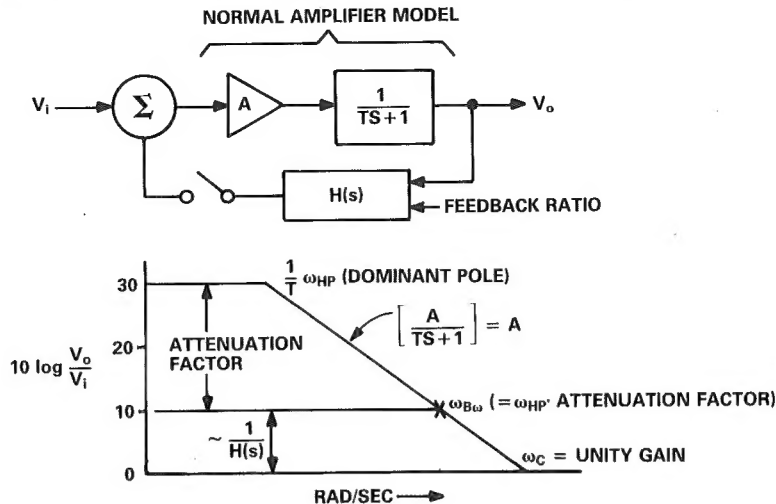
The resistor-capacitor network is referred to as a passive network because no external power is required to make it function. There is no amplification and the network is not capable of increasing power levels of its own. Any of the amplifier types that we discussed earlier may be used in a feedback system to increase power levels or provide isolation between the input and output. At present, however, we shall use a voltage amplifier in our examples since today op amps are the commonest type of amplifier to be used in such systems.

## GENERAL FORM OF FEEDBACK NETWORK AND AN AMPLIFIER CASCADED WITH A LOW PASS STRUCTURE



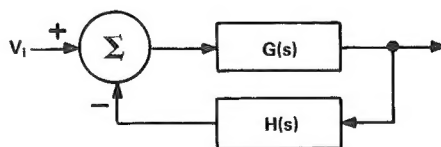
A voltage amplifier followed by a low pass filter is a reasonable first order approximation to a voltage amplifier with a dominant pole. The dominant pole is the major element in determining the frequency response of the system. The gain magnitude plot of the amplifier and low pass filter is similar to that of a low pass filter on its own except that the amplifier system has gain.

## GAIN MAGNITUDE PLOT FOR AN IDEAL VOLTAGE AMPLIFIER WITH GAIN "A" AND CASCADED LOW PASS FILTER



This type of response is typical for operational amplifiers that are internally compensated. The system is stable for all values of attenuation factor (stable for unity gain). The stability factor can be determined if the gain magnitude and feedback ratio  $H(s)$  are known. The feedback ratio is shown as  $H(s)$  for "H" and is generally frequency dependent. For the system to be stable the product  $G(s)H(s)$  should be less than unity when the phase-shift is  $180^\circ$ . If at any frequency the product  $G(s)H(s)$  is greater than unity at  $180^\circ$  phase-shift the system will be unstable and oscillate. (Don't tell marketing—they'll want to offer it as an option.)

## CONTROL SYSTEM STABILITY REQUIREMENT



FOR STABLE OPERATION  $G(s)H(s) < 1$  at  $180^\circ$  PHASE SHIFT

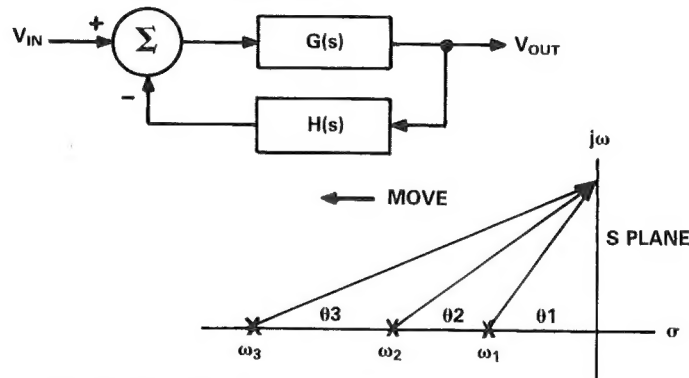
As an example consider an amplifier with a low frequency gain  $A_O = -1000$  and poles  $f_1$ ,  $f_2$  and  $f_3$  located at 50kHz, 1MHz and 2MHz respectively. Is this amplifier stable for  $H(s) = -0.005$  and  $H(s) = -0.02$ ?

### EXAMPLE 1

$$A_O = -10^3 \text{ V/V}, \omega_1 = 0.5 \times 10^6 \text{ r/s}, \omega_2 = 1.0 \times 10^6 \text{ r/s}$$

$$\omega_3 = 2.0 \times 10^6 \text{ r/s}$$

$$H(s) = -0.003, -0.02$$



FOR STABILITY  $G(s)H(s) < 1.0$   $1180^\circ$

$\therefore$  AT WHAT FREQUENCY DOES  $\theta_1 + \theta_2 + \theta_3 = 180^\circ$

$$A(f) = \frac{A_O}{\left(1 + \frac{j\omega}{\omega_1}\right) \left(1 + \frac{j\omega}{\omega_2}\right) \left(1 + \frac{j\omega}{\omega_3}\right)} =$$

$$A(f) = -\frac{10^3}{\left(1 + \frac{j\omega}{0.5 \times 10^6}\right) \left(1 + \frac{j\omega}{1 \times 10^6}\right) \left(1 + \frac{j\omega}{2 \times 10^6}\right)} =$$

A pole zero diagram will help get started on the problem by displaying the output phase variation as a function of frequency. Additionally, setting up an equation for the gain will allow us to find the frequency for which the output phase is  $180^\circ$ . For this problem it is only necessary to plot the loop gain  $G(s)H(s)$  and obtain a root locus since all that is of interest is whether or not stability exists for two values of  $H(s)$ .

### EXAMPLE 1 (CONTINUED)

$$A(f) = \frac{A_O}{(1 - 3.5f^2) + j(3.5f - f^3)}$$

FOR  $180^\circ \text{ Im}[A(f)] = 0$

$$\therefore 3.5f - f^3 = 0 = 3.5 - f^2$$

$$f^2 = 3.5, f = 1.87 \text{ MHz}$$

$$A(f) = \frac{-10^3}{[1 - (3.5)(1.87)^2]} = 88.97 \text{ V/V}$$

$\theta = 180$

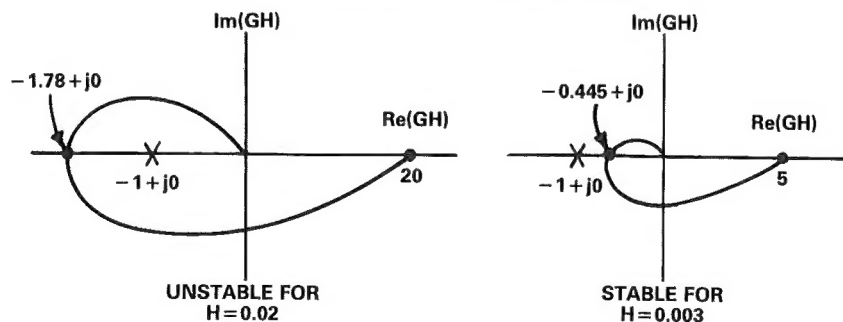
AGAIN  $GH < 1 < 180^\circ$

FOR  $H = -0.005$

$$GH = (88.97)(0.005) = -0.445 \text{ STABLE}$$

FOR  $H = -0.02$

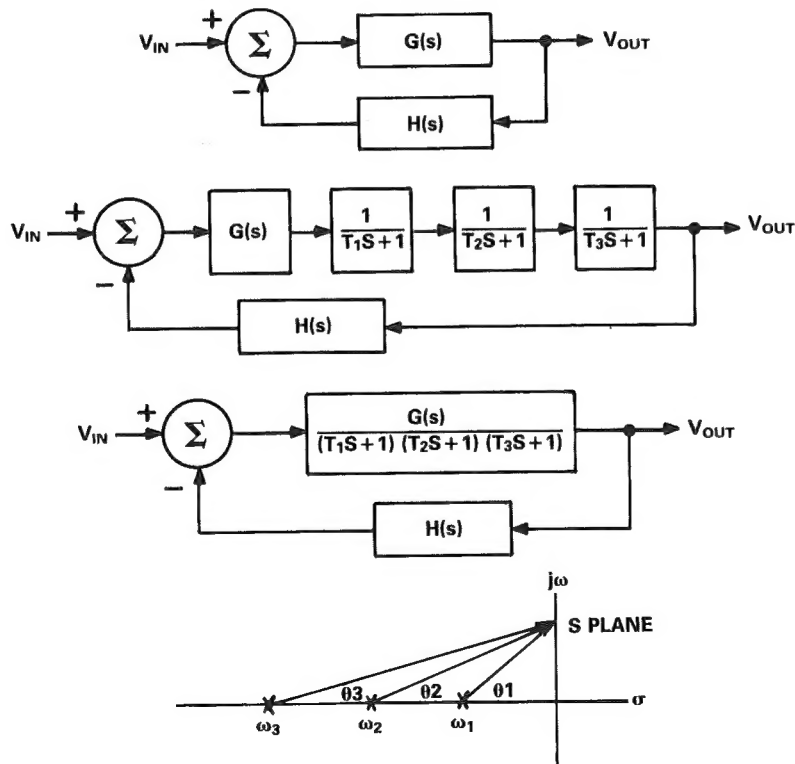
$$GH = (88.97)(0.02) = -1.78 \text{ UNSTABLE}$$



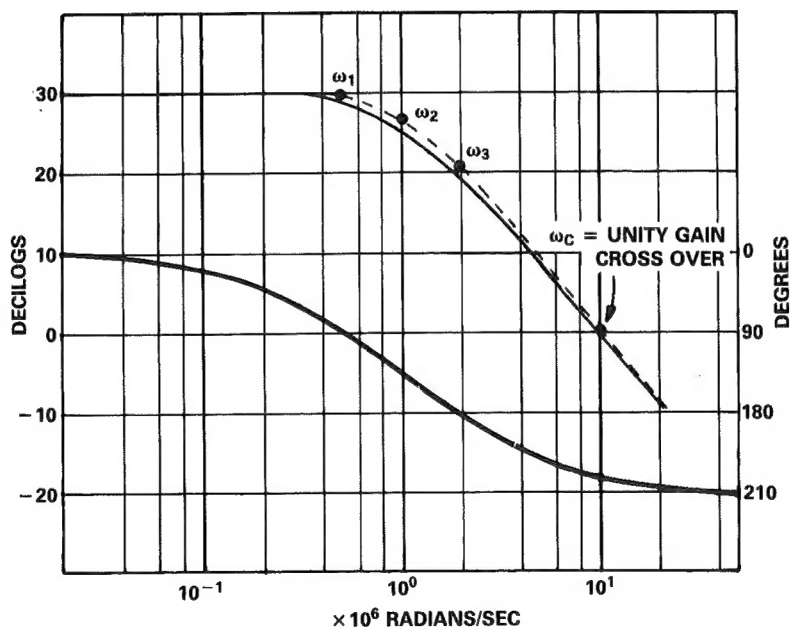
A combination of analytical and graphical techniques considerably assists the development of insight into a problem. In this case it can be seen that for an  $H(s)$  of 0.02 the amplifier is unstable and for an  $H(s)$  of 0.005 it is stable.

## EXAMPLE 2

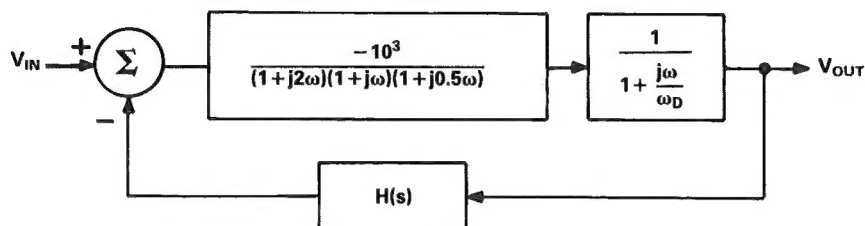
$$A_0 = -10^3 \text{ V/V}, \omega_1 = 0.5 \times 10^6 \text{ r/s}, \omega_2 = 1.0 \times 10^6 \text{ r/s}, \omega_3 = 2.0 \times 10^6 \text{ r/s}$$



The amplifier gain magnitude and phase response is plotted. The Bode plot reveals that the gain at a phase shift of  $180^\circ$  is in agreement with the computed value of 89V/V. From both the root locus plot and the Bode plot it is obvious that the amplifier cannot be used in a system where the closed loop gain is less than 89V/V. However, at a gain of 89V/V the amplifier bandwidth is approximately 318kHz. The location of the poles at  $\omega_1$ ,  $\omega_2$  and  $\omega_3$  are inherent in the design. It is possible, however, to add a dominant pole to the amplifier such that it will be stable for all closed loop gains. The disadvantage of doing this is that the bandwidth is reduced.

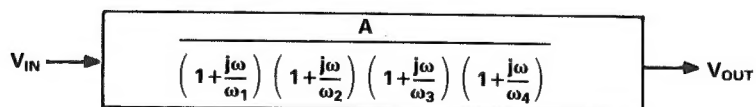


$\omega_D$  REPRESENTS A DOMINANT POLE. WHERE SHOULD IT BE FOR AN AMPLIFIER TO BE STABLE FOR ALL VALUES OF (H)?



The purpose of adding the dominant pole is to assure the stability of the amplifier for all values of the feedback ratio "H"—the largest practical value is "1" when the full output signal is fed back to the input. For stability, the product  $G(s)H(s)$  must be less than unity at  $180^\circ$ . The attenuation (negative gain) at  $180^\circ$  phase shift is known as the "gain margin" of the amplifier and is usually expressed in dB—similarly the difference between the phase shift at unity gain and  $180^\circ$  is known as the phase margin and is expressed in degrees. For practical purposes a gain margin 6dB and a phase margin of  $35^\circ$  are reasonable values which represent a compromise between excessive overshoot and mushiness in the loop response.

**SOLVING EXPLICITLY FOR  $\omega_D$  IN A SYSTEM WITH GREATER THAN THREE POLES IS CUMBERSOME AND TIME CONSUMING.**



$$\frac{V_{OUT}}{V_{IN}} = 1 \angle 180^\circ = 1 \pm j0.0$$

Using a combination of analytical and graphical techniques the dominant pole is located at approximately 0.0005 rad/sec. The phase is plotted and for an open loop gain of unity or 0dB the open loop phase shift is just about  $180^\circ$ .

